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A Symmetrical Outputs Uniplanar Out-of-Phase Power Divider without Phase Shifter

Chen Miao[1], Xuezheng Zheng[1, *], Jinping Yang[2], and Wen Wu[1]

Abstract—A new out-of-phase power divider (PD) without phase shifter at the output ports is proposed. Based on admittance matrix, a new topology of uniplanar power divider with symmetrical outputs is designed. Under conditions of good matching, perfect isolation, and 180° phase difference between two output ports, the corresponding design equations and synthesis procedures are derived and given with admittance matrix. To verify the design approach, an out-of-phase power divider operating at 2 GHz with equal power division ratio is designed, fabricated, and measured. Experimental results demonstrate that the input return loss is better than 32 dB, the insertion loss is less than 0.29 dB and the isolation is better than 33 dB. The amplitude imbalance between the output ports is 0.03 dB and the phase difference between the two output ports is 181.6° at the operation frequency. Further more, 49.9% relative bandwidth of 15 dB return loss and 39.4% relative bandwidth of 20 dB port isolation are achieved.

1. INTRODUCTION

Power dividers (PDs) are widely used in microwave and millimeter wave systems. Most of them are in-phase between the two output ports [1–8]. But in some applications such as baluns, push-pull amplifiers and antenna feeding networks, out-of-phase characteristic is respected between the two output ports. To achieve the out-of-phase characteristic, the classical method is to design an in-phase PD and add phase shifter such as microstrip delay line [9] and microstrip metamaterial lines (MML) [10] at two output ports. However, these structures suffer from large circuit size, which make them unsuitable for compact system. To design compact out-of-phase PD without phase shifter, a lot of structures have been reported [11–19]. According to the layers of the reported works, out-of-phase power dividers can be classified into two types: multilayer structures [11–17] and uniplanar structures [18, 19]. Double-side parallel striplines (DSPSL) [11–14], slotline T-junction (STJ) [15], multilayer microstrip-slotline coupling structure (MMSC) [16], and microstrip to slotline transitions (MST) [17] are applied in multilayer structures. In these works, good ports matching and wide working band are achieved. But multilayer structures increase the fabricating difficulty, and they are unsuitable for microwave and millimeter-wave integrated circuit (MMIC) implementation because the back sides of the substrates are used. Compared with the multilayer structure, uniplanar configuration is attractive because of its simplicity and easy fabrication. Out-of-phase power dividers using asymmetrical coplanar stripline (ACPS) [18], and single-section Gysel structure (SSG) [19] are developed. The structure in [18] is compact and simple, and it has achieved good amplitude and phase characteristics at two output ports, but a microstrip line to slotline converter should be used at the input port, and the output ports impedance had to be chosen as 100 Ω while impedance transformers are needed for 50 Ω ports impedance systems, which can result in an increase of system size. In [19], high power-handling capability is realized; however, the insertion losses of the two output ports are not perfectly balanced.

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* Corresponding author: Xuezheng Zheng (zxzfrot@163.com).

[1] Ministerial Key Laboratory of JGMT, Nanjing University of Science and Technology, Nanjing 210094, China. [2] Key Lab of Radio Astronomy, CAS, Nanjing 210008, China.

To the best of the authors' knowledge, the main design method for power dividers is the classical even- and odd-mode analysis. Even- and odd-mode method has been applied to many power dividers' design successfully. However, it also has two disadvantages: it doesn't consider the phase delay information in the calculation processes; and it is complicated for asymmetrical configurations or different port impedances. Using admittance matrix can resolve these two problems easily [20]. Thus admittance matrix method is introduced in this letter, based on which closed-form design equations are derived and synthesis procedures for the proposed out-of-phase power divider are given. A uniplanar out-of-phase Wilkinson power divider with isolation stubs and symmetrical output circuits is proposed. High isolation between the two output ports is obtained for the use of isolation stubs. To reduce the circuit size, traditional phase shifters are removed to the impedance transformer part. Furthermore, the output ports are symmetrical, so it can be easily integrated with other uniplanar circuits. The proposed out-of-phase power divider has been designed and fabricated. Experimental results show that the proposed structure has the characteristics of excellent input impedance matching, outputs amplitude balance, 180° phase difference at two output ports, and isolation between two output ports. That is, it can be superior to other out-of-phase power divider types in microwave circuits.

2. THE PROPOSED CIRCUIT STRUCTURE AND DESIGN EQUATIONS

It is well-known that a power divider is a three-port network with one input (port 1) and two outputs (port 2 and port 3). All ports are matched ($S_{nn} = 0$, $n = 1, 2, 3$), and two outputs are isolated ($S_{23} = 0$). For out-of-phase outputs, assuming that $\theta_1 = \theta$ is the phase delay between port 1 and port 2, and $\theta_2 = \theta + \pi$ is the phase delay between port 1 and port 3. Thus the corresponding scatter-matrix can be expressed as:

$$[S] = \begin{bmatrix} 0 & \frac{\sqrt{2}}{2}e^{-j\theta} & -\frac{\sqrt{2}}{2}e^{-j\theta} \\ \frac{\sqrt{2}}{2}e^{-j\theta} & 0 & 0 \\ -\frac{\sqrt{2}}{2}e^{-j\theta} & 0 & 0 \end{bmatrix} \tag{1}$$

The classical scatter-matrix to admittance-matrix conversion formulas with port impedance Z_0 is shown as follow:

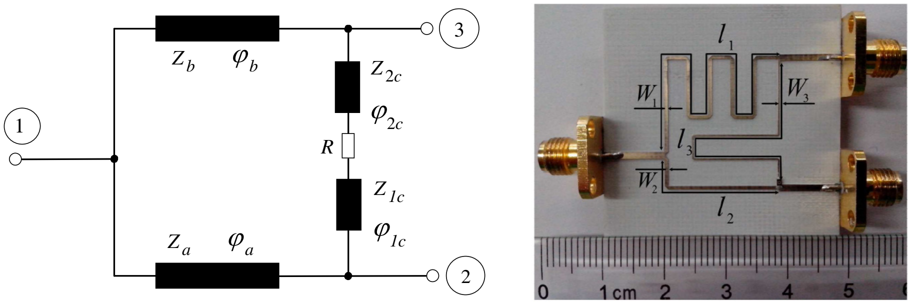
$$Y = \frac{1}{Z_0}(U - S)(U + S)^{-1} \tag{2}$$

Therefore, the expected admittance matrix of a power divider with phase shifts θ and $\theta + \pi$ at the port 2 and port 3 respectively can be obtained:

$$[Y_{ex}] = \begin{bmatrix} \dfrac{-j\cot\theta}{Z_0} & \dfrac{j\sqrt{2}}{2Z_0\sin\theta} & \dfrac{-j\sqrt{2}}{2Z_0\sin\theta} \\ \dfrac{j\sqrt{2}}{2Z_0\sin\theta} & \dfrac{1}{2Z_0} - \dfrac{j\cot\theta}{2Z_0} & \dfrac{1}{2Z_0} + \dfrac{j\cot\theta}{2Z_0} \\ \dfrac{-j\sqrt{2}}{2Z_0\sin\theta} & \dfrac{1}{2Z_0} + \dfrac{j\cot\theta}{2Z_0} & \dfrac{1}{2Z_0} - \dfrac{j\cot\theta}{2Z_0} \end{bmatrix} \tag{3}$$

The configuration of the proposed power divider is shown in Figure 1(a), where Z_a and Z_b are the characteristic impedances of the two branches, and φ_a, φ_b are the corresponding electrical lengths. Z_{1c}, Z_{2c} are characteristic impedances of the isolation stubs, and φ_{1c}, φ_{2c} are the corresponding electrical lengths. The admittance matrix of the proposed configuration can be expressed as:

$$[Y_{pr}] = \begin{bmatrix} -j\left(\dfrac{\cot\varphi_a}{Z_a} + \dfrac{\cot\varphi_b}{Z_b}\right) & \dfrac{j}{Z_a\sin\varphi_a} & \dfrac{j}{Z_b\sin\varphi_b} \\ \dfrac{j}{Z_a\sin\varphi_a} & \dfrac{-j\cot\varphi_a}{Z_a} + Y_{22}^c & Y_{12}^c \\ \dfrac{j}{Z_b\sin\varphi_b} & Y_{12}^c & \dfrac{-j\cot\varphi_b}{Z_b} + Y_{22}^c \end{bmatrix} \tag{4}$$



(a) (b)

Figure 1. (a) Configuration and (b) photograph of the proposed power divider.

where

$$\begin{aligned}
Y_{11c} &= \left(R\cos^2\varphi_{2c} + jY_{11cim}\right)/A && \text{(4a)}\\
Y_{12c} &= (-R\cos\varphi_{1c}\cos\varphi_{2c} + j(Z_{1c}\sin\varphi_{1c}\cos\varphi_{2c} + Z_{2c}\cos\varphi_{1c}\sin\varphi_{2c}))/A && \text{(4b)}\\
Y_{22c} &= (R\cos^2\varphi_{1c} + jY_{22cim})/A && \text{(4c)}\\
A &= R^2\cos^2\varphi_{1c}\cos^2\varphi_{2c} + (Z_{1c}\sin\varphi_{1c}\cos\varphi_{2c} + Z_{2c}\cos\varphi_{1c}\sin\varphi_{2c})^2 && \text{(4d)}\\
Y_{11cim} &= \sin\varphi_{1c}\cos\varphi_{1c}\left(Z_{2c}^2\sin^2\varphi_{2c}/Z_{1c} + R^2\cos^2\varphi_{2c}/Z_{1c} - Z_{1c}\cos^2\varphi_{2c}\right)\\
&\quad + Z_{2c}\sin\varphi_{2c}\cos\varphi_{2c}(\sin^2\varphi_{1c} - \cos^2\varphi_{2c}) && \text{(4e)}\\
Y_{22cim} &= \sin\varphi_{2c}\cos\varphi_{2c}\left(Z_{1c}^2\sin^2\varphi_{1c}/Z_{2c} + R^2\cos^2\varphi_{1c}/Z_{2c} - Z_{2c}\cos^2\varphi_{1c}\right)\\
&\quad + Z_{1c}\sin\varphi_{1c}\cos\varphi_{1c}(\sin^2\varphi_{2c} - \cos^2\varphi_{1c}) && \text{(4f)}
\end{aligned}$$

When the proposed admittance matrix $[Y_{pr}]$ is equal to the expected the admittance matrix $[Y_{ex}]$, the following equations can be obtained:

$$Z_a\sin\varphi_a = \sqrt{2}Z_0\sin\theta \tag{5}$$

$$Z_b\sin\varphi_b = -\sqrt{2}Z_0\sin\theta \tag{6}$$

$$\cos\varphi_{1c} = -\cos\varphi_{2c} \tag{7}$$

$$R\cos^2\varphi_{1c} = 2Z_0\sin^2\theta \tag{8}$$

$$Z_{1c}\tan\varphi_{1c} + Z_{2c}\tan\varphi_{2c} = -R\cot\theta \tag{9}$$

From (7) φ_{2c} can be obtained:

$$\varphi_{2c} = k\pi - \varphi_{1c} \quad k = \pm1, \pm3\ldots \tag{10a}$$

$$\text{or} \quad \varphi_{2c} = k\pi + \varphi_{1c} \quad k = \pm1, \pm3\ldots \tag{10b}$$

From (9) and (10), the following equations can be obtained:

$$(Z_{1c} - Z_{2c})\tan\varphi_{1c} = -R\cot\theta \tag{11a}$$

$$\text{or} \quad (Z_{1c} + Z_{2c})\tan\varphi_{1c} = -R\cot\theta \tag{11b}$$

From (5) φ_a can be expressed as:

$$\varphi_a = \arcsin\left(\sqrt{2}Z_0\sin\theta\Big/Z_0\right) \tag{12}$$

Assuming $Z_a/Z_0 = 1$, the following condition holds well:

$$\left|\sqrt{2}\sin\theta\right| \le 1 \Rightarrow \theta \in (2k\pi, \pi/4 + 2k\pi) \cup (3\pi/4 + 2k\pi, 5\pi/4 + 2k\pi) \cup (7\pi/4 + 2k\pi, 2\pi + 2k\pi) \tag{13}$$

Relations among θ, Z_a/Z_0 and φ_a are shown in Figure 2 from which it can be seen that Z_a/Z_0 should not be larger than 2 when θ is larger than 45°.

It can be obtained that when $\theta = k\pi/2$ $(k = 0, 1, 2\ldots)$, φ_{1c} should be $k\pi$ to meet Equation (12) requirement. Electrical parameters varies with different values of θ. As an instance, assuming that $\theta =$ 45° and 90°, the selecting of R, φ_{1c}, φ_{2c}, Z_{1c} and Z_{2c} for two cases (case 1 and case 2) is tabulated in Table 1. From the table it can be seen that when $\theta = 45°$ case 2 would be a good candidate.

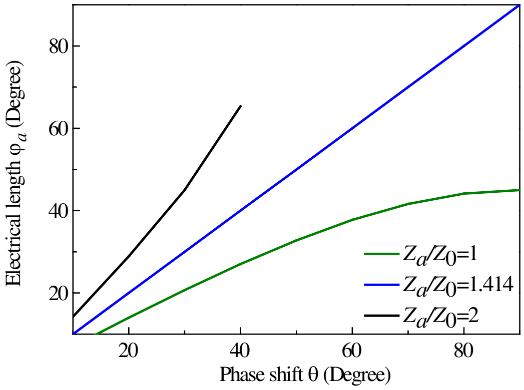


Figure 2. Relations among θ, Z_a/Z_0 and φ_a.

Table 1. Electronic parameters of R, φ_{1c}, φ_{2c}, Z_{1c} and Z_{2c}.

	φ_{1c} (°)	φ_{2c} (°)	$Z_{1c} - Z_{2c}$ (Ω)	R (Ω)		φ_{1c} (°)	φ_{2c} (°)	$Z_{1c} + Z_{2c}$ (Ω)	R (Ω)
Case 1 ($\theta = 45°$)	45	135	−100	100	Case 2 ($\theta = 45°$)	120	60	115.5	200
	120	60	115.5	200		135	45	100	100
	135	45	100	100		160	20	155.6	56.6
Case 1 ($\theta = 90°$)	180	0	*	100	Case 2 ($\theta = 90°$)	180	0	*	100
	0	180	*	100		0	180	*	100

* means arbitrary.

3. SIMULATED AND MEASURED RESULTS

To simplify the design, let $\theta = 90°$, $\varphi_a = 90°$, and φ_{1c} =180°. An out-of-phase power divider is fabricated on the Rogers 4003 substrate with the relative permittivity of 3.55 and a thickness of 0.508 mm. The operating frequency is chosen to be 2 GHz. Figure 1(b) shows a photograph of the fabricated power divider, and the corresponding physical parameters are shown in Table 2.

Table 2. The physical parameters of fabricated power divider.

Parameters	w_1	w_2	w_3	l_1	l_2	l_3
Values	0.61 mm	0.61 mm	0.3 mm	66.76 mm	22.5 mm	46.81 mm

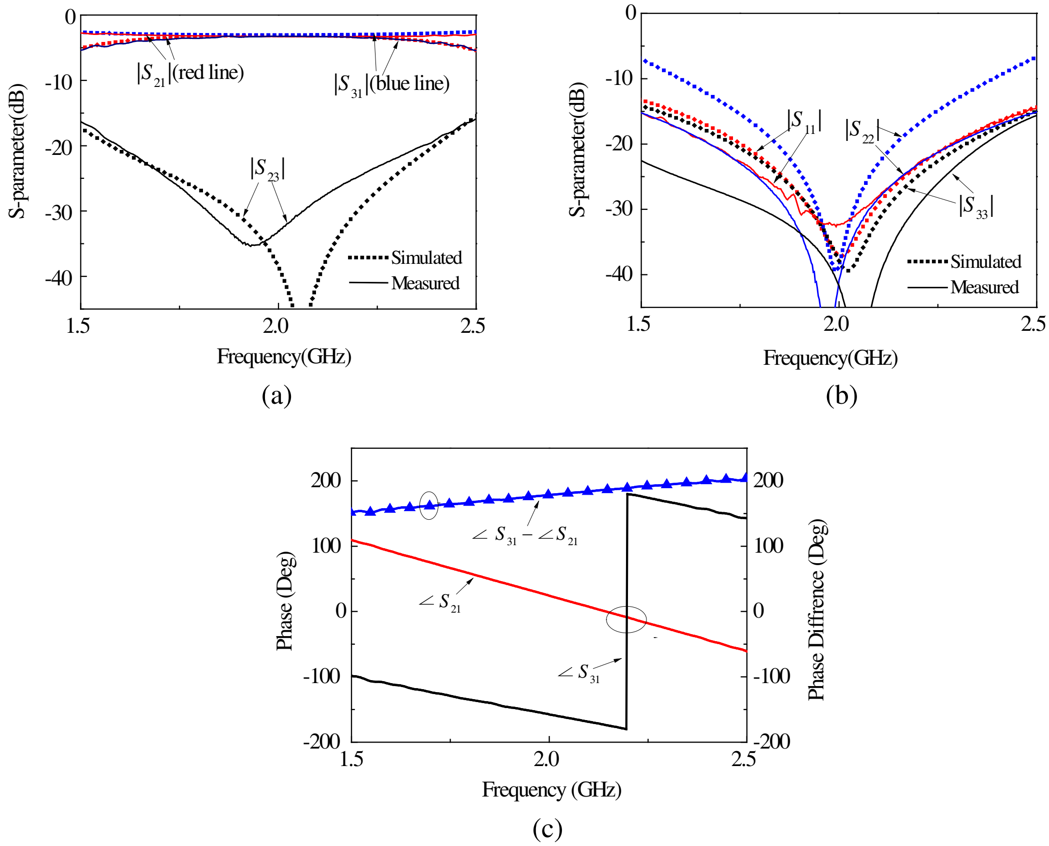
The simulated and measured results are shown in Figure 3. At the center frequency of 2 GHz, the insertion losses are: $|S_{21}| = -3.29$ dB and $|S_{31}| = -3.26$ dB; the return losses are: $|S_{11}| = -32.32$ dB, $|S_{22}| = -42.05$ dB and $|S_{33}| = -41.42$ dB; the isolation is: $|S_{23}| = -33.43$ dB; the phase difference between the two output ports is 181.6°. The 15 dB return loss bandwidth is better than 49.9%, and the 20 dB port isolation bandwidth is better than 39.4%. The measured phase difference between the two output ports is in the range of 180°±6° from 1.91 GHz to 2.15 GHz.

A performance comparison between the proposed structure and the reference works is made in Table 3. It can be found that the most listed works with out-of-phase outputs are multilayer types, while the proposed uniplanar structure in this paper is relatively simple and can be mounted in compact system easily. A modest area of the power divider is obtained compared with other structures. The device exhibits excellent ports matching and outputs amplitude balance, in addition, a phase error of 1.6° may be found sufficient in many applications. It is noted that the proposed method realized a wide isolation bandwidth, which is important for out-of-phase output signal.

Table 3. Performance comparison between the proposed structure and the reference works.

Reference	Dimension	Isolation BW	RL BW	PD (°)	AD (dB)	Approach	Circuit Layer
[10]	$> 0.35\lambda \times 0.30\lambda$	34.5%	30.5%	Good	Good	MML	Uniplanar
[11]	$0.25\lambda \times 0.05\lambda$	$< 5.4\%$	47.6%	Good	Good	DSPSL	Multilayer
[12]	$> 0.40\lambda \times 0.29\lambda$	25.6%	27.1%	Good	Good	DSPSL	Multilayer
[13]	$0.57\lambda \times 0.03\lambda$	12.5%/6.3%	10%/2.1%	Good	Good	DSPSL	Multilayer
[14]	$1.44\lambda \times 1.31\lambda$	-	17.1%	Good	Good	DSPSL	Multilayer
[15]	$0.27\lambda \times 0.28\lambda$	10.7%	71%	Good	-	STJ	Multilayer
[16]	$> 1.0\lambda \times 0.5\lambda$	-	92.2%	Good	-	MMLSC	Multilayer
[17]	$1.09\lambda \times 1.36\lambda$	3%	$< 1\%$	Good	-	MST	Multilayer
[18]	$0.16\lambda \times 0.16\lambda$	13.8%	6.7%	Good	Good	ACPS	Uniplanar
[19]	$0.25\lambda \times 0.5\lambda$	10.8%	16.7%	Good	Poor	SSG	Uniplanar
Our work	$0.20\lambda \times 0.21\lambda$	39.4%	49.9%	1.6°	0.03	ACML	Uniplanar

BW means Bandwidth. — means not mentioned. Isolation bandwidth is measured when $|S_{23}| < -20\,\text{dB}$. RL bandwidth is measured when $|S_{ii}| < -15\,\text{dB}$. λ is the wavelength in the dielectric at the center frequency. AD $= |\,\text{dB}(S_{21}) - \text{dB}(S_{31})|$. PD $= ||\angle S_{31} - \angle S_{21}| - 180°|$. ACML means asymmetrical coplanar microstrip lines.



(a) (b)

(c)

Figure 3. Simulated and measured (a) $|S_{21}|$ (red line), $|S_{31}|$ (blue line), $|S_{23}|$, (b) $|S_{11}|$, $|S_{22}|$, $|S_{33}|$ and (c) measured $\angle S_{21}$, $\angle S_{31}$, $\angle S_{21} - \angle S_{31}$.

4. CONCLUSION

Admittance matrix has been used to synthesize the out-of-phase power divider in this paper, and analytical equations have been derived. The proposed power divider employs uniplanar and symmetrical output structure for coplanar systems. Good isolation characteristic has been achieved because isolation stubs at the output ports are used. The area of the proposed power divider is reduced since no delay shift at the output ports is introduced. In Section 3, an experimental power divider, operating a bandwidth of 990 MHz (49.9%) with better than 15 dB return loss and a bandwidth of 780 MHz (39.4%) with better than 20 dB port isolation is implemented, meanwhile, good amplitude balance and small phase error are achieved, which demonstrates good agreement between simulated and measured results. The main features of the proposed power divider include: 1) no delay units at the output ports; 2) uniplanar and symmetrical outputs structure; 3) good matching and isolation characteristic are realized; 4) closed-form design equations are deduced. The method proposed in this paper simplified the design of out-of-phase power divider.

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