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High Frequency Electrical Characterization of 3D Signal/Ground through Silicon Vias

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Abstract—3D integration using through-silicon-vias (TSVs) is gaining considerable attention due to its superior packaging efficiency resulting in higher functionality, improved performance and a reduction in power consumption. In order to implement 3D chip designs with TSV technology, robust TSV electrical models are required. Specifically, due to the increase of signal speeds into the gigahertz (GHz) spectrum, a high frequency electrical characterization best describes TSV behavior. In this letter, $5 \times 50\,\mu$m TSVs are manufactured using a via-mid integration scheme and characterized using S-parameters up to 65 GHz. At 50 GHz, the measured attenuation constant is 0.35 dB/via with a time delay of 0.7 ps/via.

1. INTRODUCTION

Three-dimensional integration (3Di) is an emerging "More than Moore," concept to increase chip functionality and packaging efficiency beyond traditional scaling methods [1, 2]. Through-Silicon-Vias (TSVs) provide a vertical electrical connection between multiple 3D die stacks. Recently, Samsung and IBM have demonstrated homogeneous stacked Dynamic Random Access Memory (DRAM) packages utilizing 3Di technology [3, 4]. Additionally, several authors [5–7] have proposed heterogeneous chip stacking to integrate several chips of different functionality to form system in a package (SiP) technology. The advantages of SiP packaging using 3Di TSV technology are higher functionality, improved performance and reduction in power consumption [1]. Therefore, to implement 3Di chip architectures with TSVs, comprehensive electrical models are required to maximize performance. However, as signal speeds continue to increase into the 20+ GHz regime, simple resistance-capacitance (RC) models are no longer sufficient to predict TSV electrical behavior [8]. Further high frequency characterization is required to account for the inductance of the structure to accurately model TSV behavior in both analog and digital design.

Current state of the art TSVs consist of a $5 \times 50\,\mu$m copper vias insulated from the silicon substrate with a $0.1\,\mu$m silicon dioxide liner. Both a signal and ground (S/G) TSV are required to achieve high-speed signal propagation. Utilizing Ansoft's High Frequency Structure Simulator (HFSS), the electromagnetic (E/M) fields propagate between S/G TSV system as shown in Figure 1.

The S/G TSV geometry and silicon substrate electrical properties greatly affect the electrical parameters such as resistance, inductance, conductance and capacitance ($RLGC$). Due to the nature of high frequency signals, these parameters are not directly measureable. S-parameters are the standard metric for characterizing high frequency circuits. To the best of our knowledge, this letter is the first publication of S-parameter measurements used to characterize S/G TSV electrical behavior up to 65 GHz.

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2. DESIGN OF EXPERIMENT

Fabrication of the TSV structures utilizes a standard via middle process [9–11]. Reactive ion etching (RIE) patterns the TSV structures to a depth of 50 µm. The TSV isolation oxide liner utilizes a sub atmosphere chemical vapor deposition (SACVD) process to deposit a conformal oxide spanning the surface area of the etched TSV. Next standard copper barrier seed materials are sputtered into the via, where the TSV is then filled with copper by electroplating. Chemical mechanical polishing (CMP) removes the excess surface materials. At this point, the remaining front-side metal levels are formed using standard dual damascene metal processing. After the front-side metal wiring levels are complete, the wafers are bonded to a handle wafer, where the device wafer is thinned and the TSV structures are revealed from the backside of the wafer. Then the backside metal wiring layers are formed using standard dual damascene processing techniques to complete wafer processing. Thus, the thin device wafer can be de-bonded from the handle wafer where it can be used to form multiple die stacks for a given application. Figure 2 illustrates a completed thin TSV wafer via chain demonstrating both front and backside metal interconnects required for electrical measurements.

Due to the inability to probe, the vertical TSV interconnects directly; a symmetrical S/G TSV pair via chain is employed as shown in Figure 3. Previous work by [12] describes a mathematical method for extracting the singular TSV S-parameters as long as the full via chain and backside interconnect S-parameters, thus requiring two test sites. Additionally, both the TSV via chain and backside interconnect are embedded within a padset for measurement probes to contact the wafer. Due to the physical length of the test site from pad 1 to pad 2 being much shorter than the physical

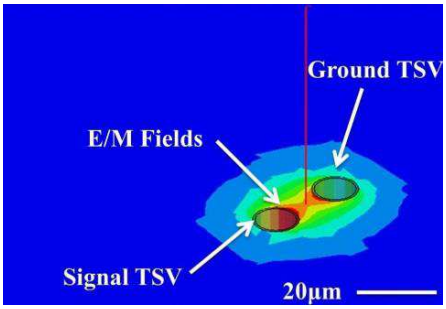

Figure 1. Top down view of electromagnetic (EM) field propagation for S/G TSV configuration solved at 25 GHz with HFSS.

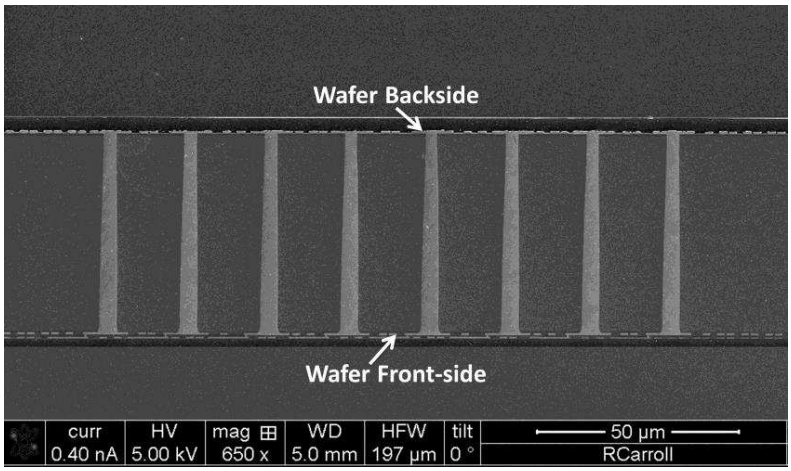

Figure 2. Polished cross-section of thin TSV device wafer illustrating manufactured TSV devices with both front and backside metal interconnect wiring.

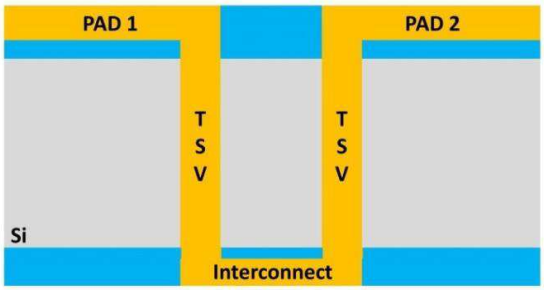

Figure 3. Cross sectional view of DUT test structure used for S/G TSV electrical characterization.

wavelength of the highest frequency of interest, the open/short de-embedding technique is valid to remove probe pad parasitics [13]. Next S-parameter measurements are made using a vector network analyzer (VNA). The current industry standard employs a two-step calibration/de-embedding method for measurement accuracy [14]. The first step is to calibrate the VNA utilizing a commercial impedance standard substrate (ISS) to move the measurement reference plane from the VNA to the probe tips. The line reflect reflect match (LRRM) technique is employed to calibrate the VNA. Specifically, the Cascade Microtech 101–190 ISS features a 1 ps thru line standard, two reflects standards featuring an open and short and lastly a 50 Ω match standard. The advantage of using the ISS substrate is the match standard is precision load trimmed to a tolerance of 0.3% compared to on wafer resistors having tolerances in the range of 6–8% leading to inaccurate calibration [14]. To verify calibration, the ISS features passive elements such as capacitors of known value that are used to validate calibrations. For these specific measurements performed, the VNA calibration produces results that are within 2% of the nominal value of the validation capacitor. Next, the dummy open and short structures remove the probe pad parasitic capacitance/conductance and inductance/resistance respectively from the DUT to yield the S-parameters of both the full via chain and the backside interconnect. Both the calibration ISS and dummy/DUT structures utilize a ground signal ground (GSG) pad scheme to correspond to the 150 µm GSG probes.

3. RESULTS

Upon calibrating the VNA, the device under test (DUT), interconnect line and dummy open/short structures are measured on the thin silicon die. Figure 4 illustrates the reflection and transmission coefficient results of both the TSV via chain and interconnect upon parasitic pad removal normalized to a reference impedance of 50 Ω.

Utilizing the t-parameter matrix extraction equation from [13], the single S/G TSV pair S-parameters are extrapolated from the measured TSV via chain and interconnect S-parameters. By utilizing the physical dimensions of the S/G TSV structures along with defining the material parameters

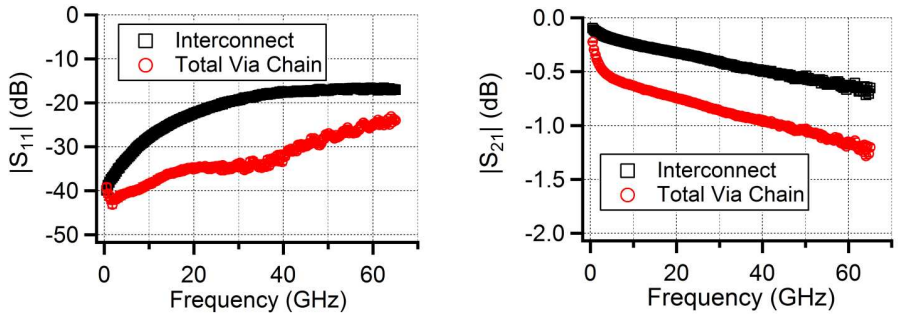

Figure 4. Reflection and transmission coefficient of the TSV via chain and interconnect after parasitic pad.

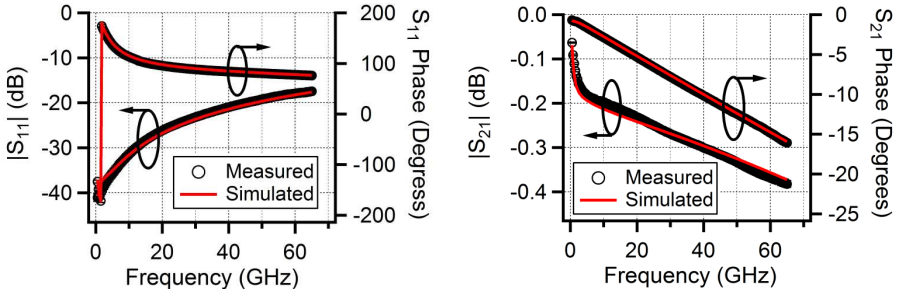

Figure 5. Transmission coefficient comparison of the measured and simulated S/G TSV pair.

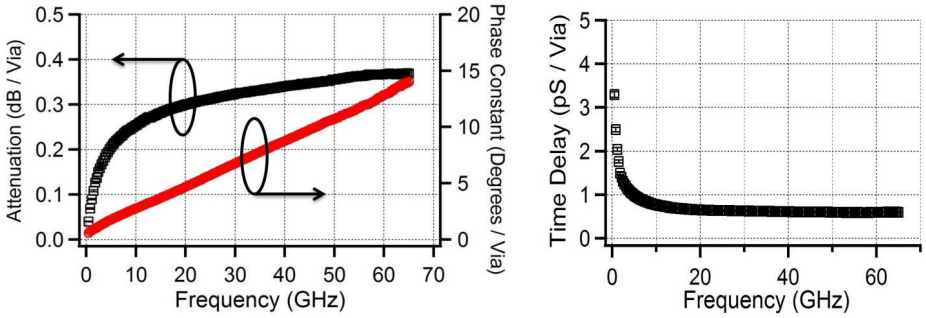

Figure 6. The extracted attenuation and phase constant of the S/G TSV structure with time delay per via transition.

such as the 10 Ω-cm substrate resistivity, the HFSS software enables a finite element full wave electromagnetic simulation to help validate S-parameter results. The HFSS simulation software features an adaptive tetrahedron finite element method to elicit fast convergence times while maintaining accurate solutions [15]. Figure 5 displays the comparison between the measured and simulated S/G TSV reflection and transmission coefficient.

As Figure 5 displays, there is excellent agreement between the reflection and transmission coefficient magnitude and phase of the S/G TSV pair. The S-parameters are now used to extrapolate key transmission line parameters such as attenuation and phase constant. By employing the methods described by Xu [16], the S/G TSV S-parameters are converted to $RLGC$ parameters. With the $RLGC$ parameters known, the transmission line propagation constant is computed in accordance with Equation (1).

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{1}$$

where the real part of the propagation constant is the attenuation constant and the imaginary component is the phase constant. The attenuation constant is a representation of the power lost in the TSV transition, while the phase constant can be used to estimate the time delay caused by the transition. Figure 6 displays both the attenuation and phase constant along with the time delay of the S/G TSV.

The S/G TSV exhibits 0.35 dB of attenuation and 0.7 ps of delay per via at a frequency of 50 GHz. The primary parameters that contribute to the attenuation loss are the copper resistance and resistivity of the silicon substrate. Therefore as expected the substrate resistivity will play a critical role in the signal integrity performance of these interconnects. Additionally, the time delay is a primary function of the capacitance and inductance of the vias, which is largely attributed to the proximity of the ground via and proximity to neighboring interconnects.

4. CONCLUSION

In this letter, S/G TSV S-parameter measurements were performed and validated with full wave EM simulations. From the S-parameters, transmission line characteristics such as attenuation and time delay were extracted. The measurements illustrate the S/G TSV signal integrity performance is dependent on not only the properties of the silicon substrate but the physical layout as well. Additionally, as these interconnects are not shielded from the substrate or adjacent interconnects, there exists a potential for unintentional signal propagation resulting in crosstalk. Therefore, designers will need to account these variables to maximize performance utilizing 3D integration.

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REFERENCES

1. Greig, W. J., *Integrated Circuit Packaging, Assembly and Interconnections,* Springer, New York, 2007.
2. Arden, W., M. Brillouët, P. Cogez, M. Graef, B. Huizing, and R. Mahnkopf, "More-than-Moore" White Paper, Version 2, 14, 2010.
3. I-Micronews, "Samsung presents new 3D TSV Packaging Roadmap," *Advanced Packaging*, Retrieved Feb. 23, 2014, from http://www.i-micronews.com/news/Samsung-3D-TSV-Packaging-Roadmap,4047.html.
4. Batra, P., et al., "Three-dimensional wafer stacking using Cu TSV integrated with 45 nm high performance SOI-CMOS embedded DRAM technology," *2013 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Vol. 43, 1–2, 2013, Doi: 10.1109/S3S.2013.6716515.
5. Beyne, E., "3D system integration technologies," *2006 International Symposium on VLSI Technology, Systems, and Applications*, 1–9, Apr. 2006.
6. Dong, X. and Y. Xie, "System-level cost analysis and design exploration for three-dimensional integrated circuits (3D ICs)," *Asia and South Pacific Design Automation Conference, ASP-DAC 2009*, 234–241, Jan. 2009.
7. Knickerbocker, J. U., et al., "3D silicon integration," *58th Electronic Components and Technology Conference, ECTC 2008*, 538–543, May 2008.
8. Johnson, H. W. and M. Graham, *High-speed Signal Propagation: Advanced Black Magic*, Prentice Hall/PTR, Upper Saddle River, NJ, 2003.
9. Yu, C. L., et al., "TSV process optimization for reduced device impact on 28 nm CMOS," *2011 Symposium on VLSI Technology (VLSIT)*, 138–139, Jun. 14–16, 2011.
10. Kawano, M., et al., "A 3D packaging technology for 4 Gbit stacked DRAM with 3 Gbps data transfer," *International Electron Devices Meeting, IEDM' 06*, 1–4, Dec. 11–13, 2006.
11. Arkalgud, S., "Via mid through silicon vias — The manufacturability outlook," *2010 International Symposium on VLSI Design Automation and Test (VLSI-DAT)*, 17–18, Apr. 26–29, 2010.
12. Chang, Y.-C., S. S. H. Hsu, D. Chang, J. Lee, S. Lin, and Y.-Z. Juang, "A de-embedding method for extracting S-parameters of vertical interconnect in advanced packaging," *2011 IEEE 20th Conference on Electrical Performance of Electronic Packaging and Systems*, 219–222, 2011, Doi: 10.1109/EPEPS.2011.6100231.
13. Yau, K. H., et al., "On-wafer S-parameter de-embedding of silicon active and passive devices up to 170 GHz," *2010 IEEE MTT-S International Microwave Symposium Digest (MTT)* 600–603, May 2010.
14. Cressler, J. D., "Measurement and modeling," *Silicon Heterostructure Handbook, Material, Fabrication, Devices, Circuits, and Applications of SiGe and Si Strained-layer Epitaxy*, 781–792, CRC Press, Boca Raton, Florida, 2006.
15. *Manual of ANSYS HFSS v.13,* ANSYS Inc., Canonsburg, PA, 2011.
16. Xu, Z. and J. Lu, "Through-silicon-via fabrication technologies, passives extraction, and electrical modeling for 3-D integration/packaging," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 26, No. 1, 23–34, 2013, Doi: 10.1109/TSM.2012.2236369.