Progress In Electromagnetics Research, Vol. 146, 181–186, 2014

High Performance Silicon-Based Inductors for RF Integrated Passive Devices

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Abstract—High-Q inductors are realized on a 3–8 $\Omega \cdot$ cm silicon substrate in the buildup of BCB/Cu. Anisotropic wet etching is utilized to remove the silicon in the cavities underneath the spirals from the backside. Examples of 3.5-turn spiral inductors with and without cavity are compared, and their parameter extractions are accomplished with an equivalent circuit model. Compared to the inductor without cavity, the measured peak quality factor of a 8.19-nH inductor with cavity increases from 24 at 0.8 GHz to 39 at 2.5 GHz by 67%, and the inductor with cavity has a wider bandwidth using the same equivalent model. The inductors utilizing this technique have a potential wide application in hand-held RF modules either as part of an off-chip device or as an integrated passive in a silicon interposer.

1. INTRODUCTION

It is the trend that the integrated passive devices substitute for the discrete ones, because increasing functionality and miniaturization are strongly demanded in the handset markets. Integrated passive devices on silicon, with thin film multilayer technologies, offer small size and high precision. Nevertheless, common silicon substrates with low resistivity bring high substrate losses and high parasitic capacitances to the inductors. There have been many methods to decrease the substrate losses, e.g., by using high resistivity silicon [1–3], glass [4–6], or other types of substrate and fabricating suspended inductors with 3-D methods [7–11]. However, high-resistivity silicon wafers are very expensive while other types of substrates may bring about CTE mismatching problems. In addition, 3-D inductors are difficult to fabricate and not easy to be integrated with other components.

In this paper, we present high Q inductors with back-etching cavities underneath the coils on common silicon substrates. As the cavities are etched in the backside, the front surface of the wafer is flat, on which other devices can be directly arranged. With a novel technique, the inductors are realized with BCB and Cu on a common silicon substrate. The Q-factor is measured up to 39 and demonstrates an inductance of 8.19 nH.

The back-etching technology is described in Section 2. The measured inductor performances are shown and compared with traditional silicon-based inductors in Section 3, and the proposed technology achieves a remarkable increase in both Q factor and resonance frequency.

2. FABRICATION

The cross, top and back views of the back-etching inductors are illustrated in Figure 1. The inductor is composed of two metal layers, two dielectric layers and a silicon substrate with cavity just underneath the copper coil. The first metal layer is used for the underpasses, which connect the inner contacts of the coils with their outside, and the second metal layer used for the coils. Thick photosensitive benzocyclobutene (12 µm) is used as the interlayer dielectric to planarize the bottom structures and

Received 8 April 2014, Accepted 16 May 2014, Scheduled 4 June 2014

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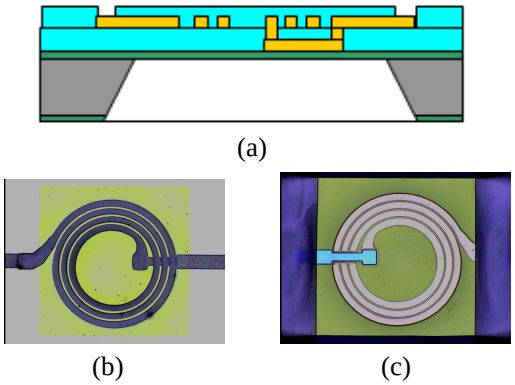

Figure 1. (b) Top, (c) back, and (a) cross-sectional views of the spiral inductor with a 3.5-turn spiral.

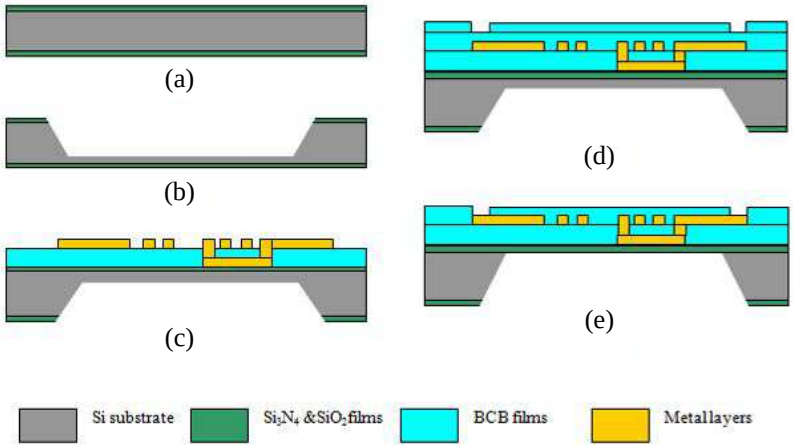

Figure 2. Schematic of the fabrication process.

reduce the capacitive coupling between the two layers sufficiently. In order to reduce substrate losses and parasitic capacitances, the silicon below the coils is removed by wet etching from the backside. The cavities are realized using two steps of anisotropic wet etching: one is implemented before the coils formation to etch most of the silicon in the cavities while the other is carried out after the formation of the coil and dielectric layers to etch the left silicon.

Figure 2 schematically shows the major process steps for the fabrication of the inductors. All steps are performed at 4-in (100) 430-μm-thick silicon wafers with a resistivity of 3–8 $\Omega \cdot$ cm. The detailed fabrication steps are as follows.

a) First of all, a 2-μm-thick silicon dioxide film and a 0.5-μm-thick silicon nitride film are formed on both sides of the wafer by thermal oxidation and low-pressure chemical vapor deposition (LPCVD) respectively.

b) Windows for etching cavities are opened on the backside of the silicon dioxide and silicon nitride films deposited, by reactive ion etching (RIE) after photolithography. The etched windows are aligned with $\langle 110 \rangle$ orientations for the sake of the etching of cavities just underneath the coils. After that, 380-μm-deep cavities are etched in KOH-based anisotropic etchant.

c) Titanium/tungsten and copper are sputtered on the top of the silicon nitride at the front side as the adhesion and seed layer. A 7-μm-thick photoresist (AZ9260) layer is coated and patterned. Then 5-μm-thick copper films are electroplated as the underpasses of the inductors. The photoresist and TiW/Cu seed layers are successively stripped by acetone and by plasma etching respectively. Then, the interlayer polymer is realized with the via holes connecting the first metal layer with the following one.

Photosensitive benzocyclobutene (BCB) is chosen for its resistance to strong alkali, easy processing and excellent electrical characteristics. To prepare the second metal layer, the same procedures as above are applied. 8-µm-thick copper lines are electroplated to create the spiral coils and metal pads.

d) A layer of BCB to be served as protective layer is coated by spinning after coating of Dow's AP3000 (adhesion promoter for BCB) followed by 90 seconds soft baking at 110°C. This layer, being used to protect metal lines from alkali in the following step, will selectively be moved later. More details will be proposed in the next subsection. A passivation film of BCB with openings for pads is realized with the same process as step c.

e) Then, the wafers are etched in 29 wt% 80° KOH solution to remove the left 50 µm silicon on the bottom of the cavities underneath the coils by one hour. Over etching is carried out to make sure that the silicon is clean, and the metal lines are protected by the silicon dioxide film underneath and the fully cured BCB films. Finally, ten-minute dry etch step has to be carried out in O_2/SF_6 plasma to remove the BCB covering metal pads.

3. MEASUREMENTS AND MODELING

The two-port S-parameters are measured using an on-wafer measurement station with vector network analyzer and 150 µm ground-signal-ground (GSG) coplanar probes after a short-open-load-thru (SOLT) calibration. Then, the parasitic parameters of the pad are removed by open-short de-embedding method. The sweep frequency ranges from 0.05 GHz to 10 GHz. Q-factor and inductance are calculated using Equations (1) and (2), respectively.

$$L_{11} = \frac{\mathrm{Im}\left(1/Y_{11}\right)}{2\pi f} \tag{1}$$

$$Q_{11} = \frac{\mathrm{Im}\left(1/Y_{11}\right)}{\mathrm{Re}\left(1/Y_{11}\right)} \tag{2}$$

Both the proposed inductors with back-etching cavities and the traditional ones without cavities are realized, and the performances are shown in Figure 3. Compared to the inductors without cavities, the back-etching ones demonstrate significantly higher resonance frequencies and higher Q-factor at the frequency above 1 GHz. The cavities underneath the spiral coils remarkably restrain the eddy current in the silicon substrates and diminish substrate loss. The influences of the parasitic capacitors become intense with the increase of frequencies. At the frequencies beyond resonance frequencies, parasitic capacitors are dominant, so the Q-factors and inductances are negative.

Lumped physical model in Figure 4(a) is commonly used to simulate the behavior over frequency of a two-port inductor on silicon. Parameter extractions are carried out with the equivalent model in

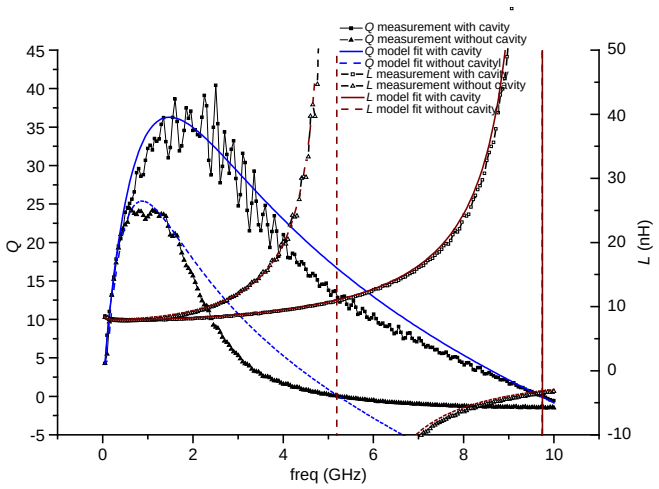

Figure 3. The measurement and modeling characteristic of the inductors.

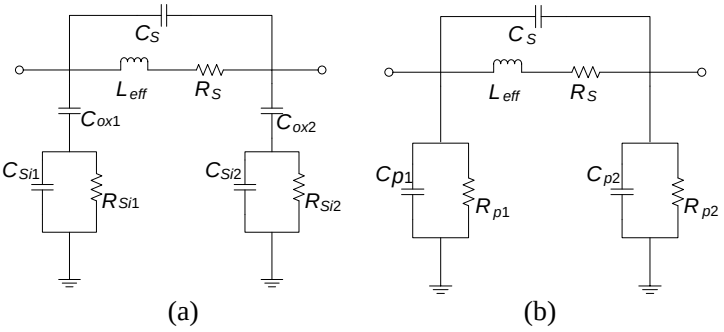

Figure 4. Equivalent circuit elements (a) lumped element conventional model; (b) simplified model for parameters extraction.

Table 1. The values of the equivalent circuit elements.

Extracted parameter	Inductors with cavities	Inductors without cavities
L_{eff}	7.89 nH	7.97 nH
Rs	$0.43 + 2.1e - 5\sqrt{f}\,(\Omega)$	$0.43 + 2.1e - 5\sqrt{f}\,(\Omega)$
Cs	19.1 fF	98.04 fF
C_{p1}	18.6 fF	19.48 fF
R_{p1}	5418 Ω	2489 Ω
C_{p2}	15.0 fF	20.85 fF
R_{p2}	7268 Ω	2791 Ω

Figure 4(b) with the combined impedance of C_{ox}, C_{Si} and R_{Si} substituted by R_P and C_P [12]. We extract the R_p, C_P, L_{eff}, and C_S using Equation (3) as described in [6].

$$\begin{cases} R_{p1} = \dfrac{1}{\mathrm{Re}\,(Y_{11} + Y_{12})}, & R_{p2} = \dfrac{1}{\mathrm{Re}\,(Y_{22} + Y_{12})} \\ C_{p1} = \dfrac{\mathrm{Im}\,(Y_{11} + Y_{12})}{\omega}, & C_{p2} = \dfrac{\mathrm{Im}\,(Y_{22} + Y_{12})}{\omega} \\ L_{eff} = -\dfrac{\mathrm{Im}\left(\frac{1}{Y_{12}}\right)}{\omega} \\ f_{res1} = \dfrac{1}{2\pi\sqrt{L\,(C_{gl} + C_s)}} \end{cases} \tag{3}$$

where f_{res1} is the resonance frequency of the inductors with port 1.

Equation (4) is used to catch the skin effect influence of the conductor.

$$R_s = R_0 + R_1\sqrt{f} \tag{4}$$

R_0 is the direct-current resistance of the coil. And R_1 is determined with equation

$$R_{Q\max} = R_0 + R_1\sqrt{f_{Q\max}} \tag{5}$$

where $f_{Q\max}$ is the frequency for the maximum Q factor, and $R_{Q\max}$ is extracted from Y_{12} of $f_{Q\max}$. After all the parameters are determined, ADS tune tool is used to optimize the parameters with the Q factor curve.

As an example, the spiral inductors with width 35 µm, space 10 µm and 3.5 turns on two kinds of silicon substrates are represented with the values of the equivalent circuit elements in Table 1 and inductors behavior in Figure 3. As shown in Table 1, R_P of the back-cavity inductor is larger than the solid one while C_S and C_P are smaller than the solid one. The back-cavity inductors exhibit not only

Table 2. Performances of various inductors.

Ref.	L (nH)	$Q_{\max}$ (Freq.)	SRF (GHz)	Methods
This work	8.19	39 (2.50 GHz)	9.7	Wet-etching cavity
[4]*	7	12 (0.5 GHz)/27 (1 GHz)	1.7/2	multilayer thin film technology on silicon/glass
[2]*	10	27 (1.2 GHz)/37 (2.5 GHz)	7	$3000\,\Omega \cdot$ cm HR-Si without/with surface passivation
[10]	2.78/2.96	28 (4.9 GHz)/45 (5.35 GHz)	> 10	Concave-suspended solenoid inductors
[13]*	1/5.2	25 (2.0 GHz)/20 (1.1 GHz)	$7/ > 7$	Thick BCB
[14]	4.92	34.3 (N.A.)	11	Polymer cavity

* The data is not specified and is read from the figures of measurements.

lower substrates loss, but also lower capacitance. With the same equivalent circuit model, the inductor with cavity is provided with wider bandwidth, as the simulated performances of the one with cavity agree well with the measurement results in the frequency range from 0.05 GHz to 10 GHz while the simulation Q-factor of the inductor without cavity mismatches with the measurement at the frequencies above 2 GHz.

The performances of the proposed inductors are compared to those using other technologies in Table 2. The proposed inductors show equivalent or better characteristics than those using other methods.

4. CONCLUSIONS

For high-Q planar inductors, a two-step wet-etching is applied to realize cavities underneath the spiral coils. BCB is chosen as the interlayer dielectric and passivation material as well as metal-protection layer from KOH etchant. The measurement results show that the fabricated inductors with cavities accomplish significantly higher Q-factors than the ones without. The backside cavities not only reduce the high frequency ohmic losses, but also diminish the unwanted parasitic capacitance. And these inductors can be widely used in the RF front-end circuits of wireless systems in 1–10 GHz frequency region either as off-chip devices or integrated in the silicon interposers with even surface.

ACKNOWLEDGMENT

The authors would like to thank SIMIT for the manufactory platform and package implementation. This work is supported by the National Major Fundamental Research Program of China (No. 2011CB932904), National Science and Technology Major Projects (No. 2011ZX02602), and Natural Science Foundation of Shanghai (No. 13ZR1447300).

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