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The Frequency Behaviour of the Intrinsic Immunity of the On-Chip Transistor Circuit

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Abstract—To extract the immunity model in an easy way and to complete the immunity simulation in a short time, it is preferred to consider only the disturbance propagation network in an integrated circuit system. However, through theoretical analyses, simulations and measurements, this paper shows that the on-chip transistor circuit has a nonuniform frequency response on its immunity against arrival disturbances. Including the nonuniform frequency response qualitatively improves the match between the simulation and measurement results. The conclusion is that both the disturbance propagation network and on-chip transistor circuit should be considered in the immunity simulation.

1. INTRODUCTION

The evaluation of the electrical performance in the design phase of an electronic system can only be conducted with simulation. Simulating the radio frequency (RF) immunity of integrated circuits (ICs) is interesting in the design phase of the ICs and printed circuit boards. IEC has established a standard for immunity modelling of ICs [1]. The frequency of the RF interference (RFI) signal is labeled with f_{RFI}. The RF immunity of ICs is characterized with immunity curves in f_{RFI} range from below 1 MHz to near or above 1 GHz. The immunity curve shows, for each f_{RFI}, the maximal RFI power ($P_{\mathrm{RFI\_}T}$) that the IC can tolerate. Normally, a measured RF immunity has the frequency behaviour that $P_{\mathrm{RFI\_}T}$ varies strongly with f_{RFI}. The main task of the RF immunity modeling is to simulate that frequency behaviour.

When a RFI signal is applied to an IC, the signal goes through the disturbance propagation network (DPN) and arrives at the on-chip transistor circuit (OCTC). Previous researches [2–7] in immunity modeling of modern ICs have focused on constructing the model of DPN and use the frequency behaviour of DPN to reproduce the frequency behaviour of the RF immunity. However, besides DPN, the response of OCTC to the arrived RFI may vary with f_{RFI}. The relationship between the maximal tolerable RFI voltage which has arrived at OCTC and f_{RFI} is called the intrinsic immunity of OCTC. The motivation of this paper is to check whether the intrinsic immunity of OCTC is, in f_{RFI} range from 1 MHz to 1 GHz, a constant or not. If the intrinsic immunity is a constant, then modeling the DPN is sufficient to simulate the RF immunity of the IC. Otherwise, the frequency behaviour of the intrinsic immunity of OCTC should be included in simulating the RF immunity of the IC. The latter will complicate the immunity modeling to a greater degree, because simulating a modern IC, no matter the whole chip or a functional module, at transistor level normally requires huge resources.

The "Frequency Behaviour of the Immunity" section analyses the signal relations in the immunity test fixture, and explains the concepts of immunity and intrinsic immunity. The "simulation" section illustrates two approaches of the immunity simulation. One approach considers the intrinsic immunity of OCTC while the other does not. The "Discussion" section compares the simulation results with the measurement results. The difference in the results of the two approaches brings out the conclusion on the importance of the intrinsic immunity.

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2. FREQUENCY BEHAVIOUR OF THE IMMUNITY

The circuit under test is the oscillator input and output (XIO) module of microcontroller (μC) XC2287 from Infineon Technologies. Here, the OCTC is the XIO module. The immunity test setup follows the Direct Power Injection (DPI) method [8] and is depicted in Fig. 1. The RFI is injected to the oscillator input (X_1) pin of the μC. The status of the μC is monitored through a feedback signal. The μC is considered to fail if the feedback signal is not completely inside the tolerance mask on the oscilloscope. The RFI output from the directional coupler is called the transmitted RFI. Its power is $P_{\mathrm{RFI\_}T}$. In the immunity test, $P_{\mathrm{RFI\_}T}$ at a specific f_{RFI} is increased until the μC fails. The maximal achieved $P_{\mathrm{RFI\_}T}$ is recorded as the immunity level at f_{RFI}. In our test, the range of the f_{RFI} is from 0.5 MHz to 1 GHz.

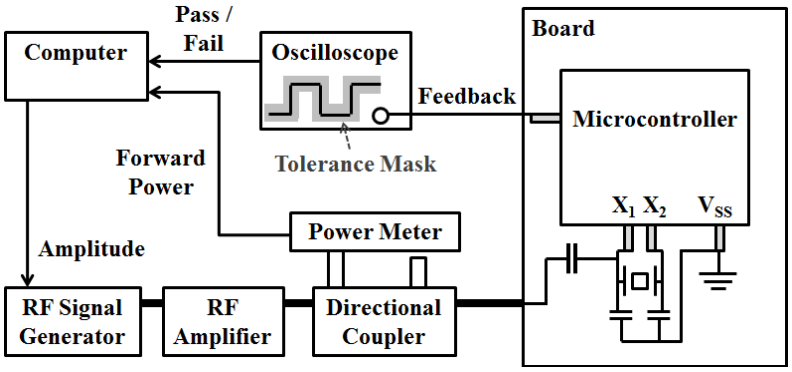

Figure 1. Immunity test setup.

The RFI which reaches the X_1 pad is called the arrived RFI. Its amplitude is denoted with $V_{\mathrm{RFI\_}R}$. The amplitude of the transmitted RFI is denoted with $V_{\mathrm{RFI\_}T}$. If the RF generator, amplifier and the directional coupler together are considered as a RFI source with an internal impedance of the system impedance Z_0, then $V_{\mathrm{RFI\_}T}$ is half of the source amplitude $V_{\mathrm{RFI\_}S}$. The amplitudes $V_{\mathrm{RFI\_}S}$ and $V_{\mathrm{RFI\_}R}$ are related with transfer coefficient of DPN, $\mathrm{TC_{DPN}}$, as is shown in (1).

If $V_{\mathrm{RFI\_}R}$ exceeds a threshold, the XIO module fails and consequently the μC fails. Suppose the value of the threshold is $V_{\mathrm{th\_XIO}}$, then the maximal allowed $V_{\mathrm{RFI\_}T}$ will be (2). The corresponding power is given in (3). $P_{\mathrm{RFI\_}T\_\mathrm{max}}$ is the immunity of μC. Of course the immunity of the μC will be different if RFI is injected to a pin other than X_1. However, let's focus on the X_1 pin in this paper and consider the immunity tested on pin X_1 as the immunity of the μC.

$$V_{\mathrm{RFI\_}R} = V_{\mathrm{RFI\_}S}\mathrm{TC_{DPN}} = 2V_{\mathrm{RFI\_}T}\mathrm{TC_{DPN}} \tag{1}$$

$$V_{\mathrm{RFI\_}T\_\mathrm{max}} = \frac{1}{2}\frac{V_{\mathrm{th\_XIO}}}{\mathrm{TC_{DPN}}} \tag{2}$$

$$P_{\mathrm{RFI\_}T\_\mathrm{max}} = \frac{(V_{\mathrm{RFI\_}T\_\mathrm{max}})^2}{2Z_0} \tag{3}$$

Now refer to (2). $V_{\mathrm{RFI\_}T}$ depends on both $V_{\mathrm{th\_XIO}}$ and $\mathrm{TC_{DPN}}$. $V_{\mathrm{th\_XIO}}$ is the maximal allowed RFI on the OCTC, therefore $V_{\mathrm{th\_XIO}}$ is the intrinsic immunity of the XIO module. If $V_{\mathrm{th\_XIO}}$ is independent from f_{RFI}, then the variation of $P_{\mathrm{RFI\_}T\_\mathrm{max}}$ in the frequency domain is due to the DPN. If $V_{\mathrm{th\_XIO}}$ is dependent on f_{RFI}, then both the DPN and $V_{\mathrm{th\_XIO}}$ contribute to the variation of $P_{\mathrm{RFI\_}T\_\mathrm{max}}$ in the frequency domain.

3. SIMULATIONS

The immunity simulations are performed with two approaches. According to (2) and (3), the immunity can be calculated once $\mathrm{TC_{DPN}}$ and $V_{\mathrm{th\_XIO}}$ are known. The two approaches handle $\mathrm{TC_{DPN}}$ in the same way but handle the $V_{\mathrm{th\_XIO}}$ in different ways.

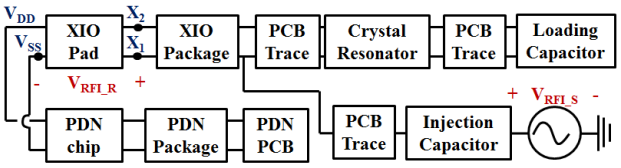

Figure 2. DPN model.

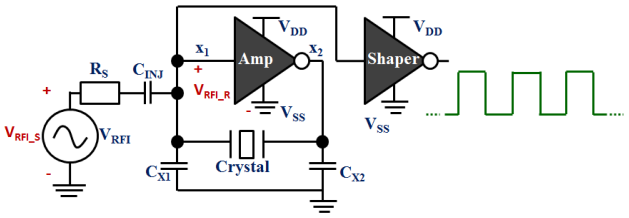

Figure 3. XIO model.

In the first approach, the DPN model is constructed. The model is in the format of SPICE netlist. TC_{DPN} is obtained through simulating on the DPN model. V_{th_XIO} is assumed to be constant and is obtained through direct current measurement. Inserting TC_{PDN} and V_{th_XIO} into (2) and (3) produces the simulated immunity of the first approach: P_{S_TC}.

The second approach differs from the first approach by the following point: V_{th_XIO} is not assumed to be constant. It is obtained through transistor level simulation on the XIO module. The simulated immunity of the second approach is denoted with $P_{S\_TC\_VTH}$.

The structure of the DPN model is shown in Fig. 2. Each block represents the SPICE-like equivalent circuit (EC) of a component. The EC of a PCB component is extracted through impedance measurement. The EC of a package component is extracted through filed simulation. The EC of the on-chip component is extracted through the combination of impedance measurement and field simulation. A more detailed description of the model construction can be found in [7]. The simulator is HSPICE.

A BSIM3v3 transistor-level model of XIO module is built to extract the intrinsic immunity, V_{th_XIO}. The model structure is shown in Fig. 3. The output of the shaper is a clock signal. Increasing V_{RFI_S} will distort the waveform of the clock. V_{th_XIO} is the value of V_{RFI_R} where the period of clock is shifted by 20% or the amplitude of the clock signal is reduced by 20% both with respect to clock waveform in absence of RFI. The simulator is HSPICE.

4. DISCUSSION

The matches between the simulation results and the measurement results are presented in Fig. 4 and Fig. 5. The measured immunity curve can be characterized with a few critical features like peaks and valleys. Referring to Fig. 4, the simulation results based on the DPN model can reflect those critical features in the frequency range above 200 MHz. However, the peak 8 MHz and the valley around 100 MHz are missing in the simulation results. By contrast, as shown in Fig. 5, the missing features can be recovered by adding the frequency response of the intrinsic immunity to the simulation.

The simulation results show that DPN is responsible for those critical features in above 100 MHz range while the intrinsic immunity is responsible for the range below 100 MHz. The inclusion of

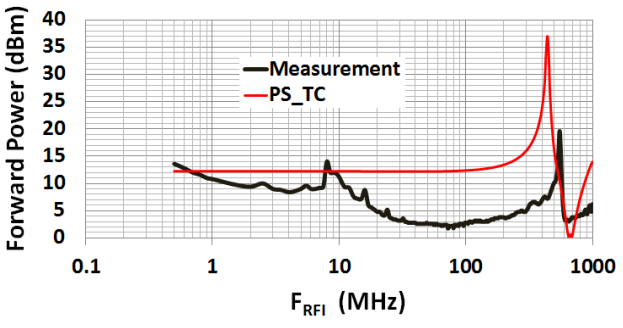

Figure 4. Comparison of measurement and simulation results. The frequency response of the intrinsic immunity is not considered.

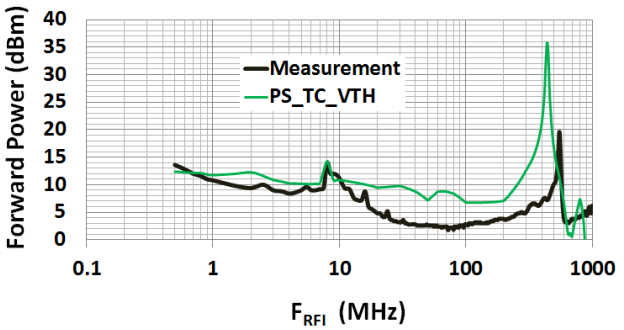

Figure 5. Comparison of measurement and simulation results. The frequency response of the intrinsic immunity is considered.

the intrinsic immunity gives a qualitative improvement on the matching between the simulation and measurement results.

To acquire the intrinsic immunity of OCTC costs a lot, especially for large ICs. It brings a great challenge on the immunity simulation methods. It is valuable to investigate on how to extract the intrinsic immunity in an easy and fast way without lose any critical feature.

5. CONCLUSION

The frequency response of the intrinsic immunity of OCTC is not uniform and is the origin of certain critical features in the immunity of the IC. Both DPN and the intrinsic immunity should be considered in simulation if the frequency response of the IC immunity needs to be fully reflected in the results.

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