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UWB Multilayer Power Divider with High Isolation

Long Xiao* and Tao Yang

Abstract—A novel compact slotline power divider is proposed in this article. This presented power divider employs a novel configuration with one lumped resistor, which makes it surpass most antecedent UWB power dividers based on microstrip-to-slotline transitions in aspect of isolation between output ports and return losses at output ports. The simulated and measured results illustrate the good performances of the novel power divider on return losses at all ports, isolation, amplitude and phase balances between output ports, as well as group delay over the wide frequency band from 3.8 GHz to 10.4 GHz.

1. INTRODUCTION

Since the unofficial definition about ultra wideband (UWB) was determined in 2002, hundreds of UWB components have been designed and applied [1–8]. Power dividers play an indispensable role in numerous wireless communication systems. With the rapid development of UWB wireless systems, the demands for UWB power dividers are greatly increasing. For the sake of satisfying the imperious needs, some UWB power dividers based on microstrip-to-slotline transition techniques have been designed and fabricated [9–11]. In order to improve the performance, some new UWB power dividers with improved structures have been proposed [12, 13]. In [9], one compact 180° out-of-phase UWB power divider based on slotline techniques was designed, where the two output ports locating in top layer were combined. However, because of the combination of output branches, the isolation between output ports and the return losses at output ports were very poor. In order to improve the performances of UWB power dividers based on microstrip-to-slotline transitions, the output branches of power dividers presented in [10, 11] were split into two parts. In [10], a multilayer compact UWB out-of-phase power divider was proposed. This power divider employed separated output branches and introduced two compensatory microstrip circular stubs. By making use of a similar method, a new coplanar in-phase UWB power divider was designed in [11]. In [12], one metal pin was utilized to extend the operating band. In [13], a tapered slotline and a fan-shaped slotline were utilized to take the place of the circular ones designed in [10]. The changes employed in [10–13] indeed improved the homologous performances to some extent. However, these improvements are negligible. The isolation and impedance matching at output ports are still poor.

As all know, a reciprocal and lossless three-port network cannot get good impedance matching at all ports simultaneously, which is the inherent property of three-port network. Therefore, in order to obtain good impedance matching at all ports as well as high isolation between output ports, the performance of lossless must be sacrificed. In this article, a novel UWB in-phase multilayer power divider with high isolation is proposed and designed. For the sake of introducing one isolation resistor to change the lossless property, this new power divider abandons traditional quarter-wavelength slotline and employs multilayer configuration.

In this presented design, the isolation between output ports and the impedance matching at output ports, according to the experimental results, have been improved greatly compared with those proposed in [9–13] over the range from 3.8 GHz to 10.4 GHz.

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2. ANALYSIS AND CIRCUIT DESIGN

2.1. Theoretical Analysis

Microstrip-to-slotline transition is the basic unit of UWB power divider proposed in the article. Figure 1 exhibits one transition which is a part of this new power divider. The equivalent circuit model has been established as shown in Figure 2. C_{oc} is the capacitance of the open-circuited microstrip-line stub and L_{os} the inductance of the short-circuited slot-line stub. Z_{om} and Z_{os} are the microstrip and slotline characteristic impedance, respectively. θ_m and θ_s are the electrical lengths of the homologous transmission lines at center frequency. n is the transformer turn ratio [14–17], which can be determined by (1).

$$n = \frac{J_0(k_{es}W_m/2)J_0(k_{em}W_s/2)}{k_{es}^2 + k_{em}^2} \cdot \left[\frac{k_{em}^2 k_2 \varepsilon_r}{k_2\varepsilon_r\cos(k_1h) - k_1\sin(k_1h)} + \frac{k_{es}^2 k_1}{k_1\cos(k_1h) + k_2\sin(k_1h)}\right] \quad (1)$$

where $J_0(\cdot)$ is the zeroth-order Bessel function and

$$\begin{aligned} k_1 &= \sqrt{\left|k_0^2\varepsilon_r - k_{es}^2 - k_{em}^2\right|} = k_0\sqrt{|\varepsilon_r - \varepsilon_{res} - \varepsilon_{rem}|} \\ k_2 &= k_0\sqrt{|\varepsilon_{res} + \varepsilon_{rem} - 1|} \\ k_{es} &= k_0\sqrt{\varepsilon_{res}}, \quad k_{em} = k_0\sqrt{\varepsilon_{rem}} \end{aligned}$$

Here, ε_{res} and ε_{rem} represent the effective dielectric constants of the microstrip line and slotline, respectively.

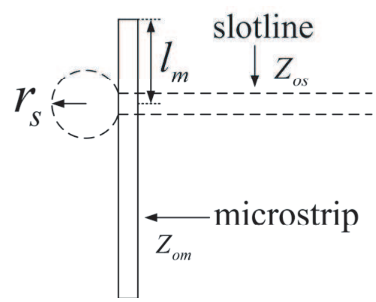


Figure 1. Model of microstrip-to-slotline transition.

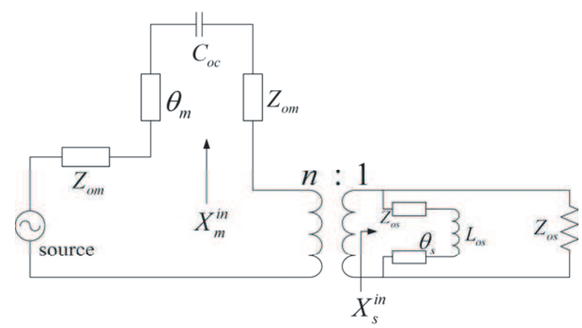


Figure 2. Equivalent circuit of the microstrip-to-slotline transition.

According to the equivalent circuit model and the expression about n, the reflection coefficient at input port Γ_{in} [14–16] can be expressed as

$$\Gamma_{in} = \frac{R_s - Z_{om} + j(X_m + X_s)}{R_s + Z_{om} + j(X_m + X_s)} \quad (2)$$

where

$$\begin{aligned} R_s &= \frac{n^2 Z_{os} X_s^{in}}{Z_{os}^2 + X_s^{in}} \\ X_s &= \frac{n Z_{os} X_s^{in}}{Z_{os}^2 + X_s^{in}} \\ X_m &= X_m^{in} \end{aligned}$$

Through a series of calculations and simplifications, we can get that when the microstrip characteristic impedance Z_{om} equals $n^2 Z_{os}$, the reflection coefficient at input port will reach minimum value. In order words, when $Z_{om} = n^2 Z_{os}$, microstrip-to-slotline transition can obtain good impedance matching.

2.2. Circuit Design

The configuration of the presented novel compact in-phase power divider with high isolation is exhibited in Figure 3. This power divider, as shown in Figure 3, employs a three-layer structure. The input port is placed in the bottom layer. The two output ports are designed on the top layer. And the slotline is etched in the middle layer. To install the lumped resistor on the ends of output branches, the slotline abandons conventional quarter-wavelength configuration (distance between input port and output port), and the microstrip-line stubs in top layer are buckled. Compared with the power dividers designed in [9–13], the structure of this novel UWB power divider is changed a lot. However, these changes will not affect the width of operating band [14].

Although the width of the operating band will not be influenced, the flatness will be affected. As shown in Figure 4, the influence of the length of slotline on flatness is studied. The flatness will be worsened with increasing the length of slotline as exhibited in Figure 4. In order to offset the negative influence resulting from the change of slotline, several compensatory stubs are designed as exhibited in Figure 3. One circular microstrip stub and two circular slotline stubs are placed at the ends of input branch and slotline, respectively. The output branches, however, introduce two common microstrip-line stubs to replace circular stub so that the lumped resistor can easily be soldered. Moreover, to obtain

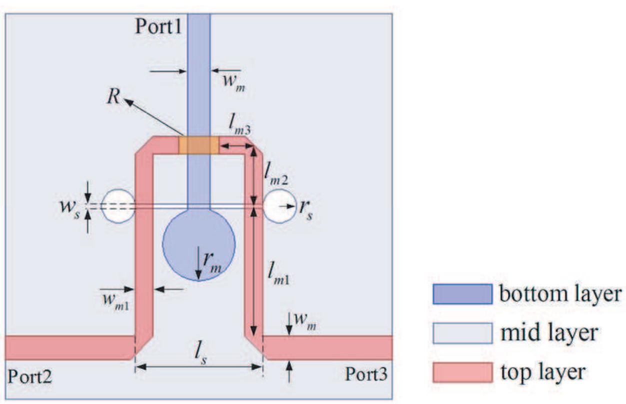


Figure 3. Configuration of the UWB multilayer power divider.

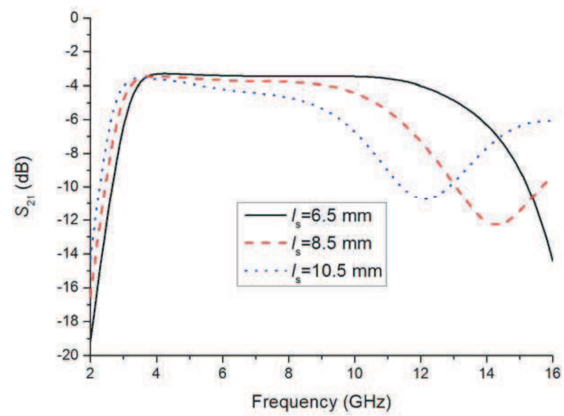
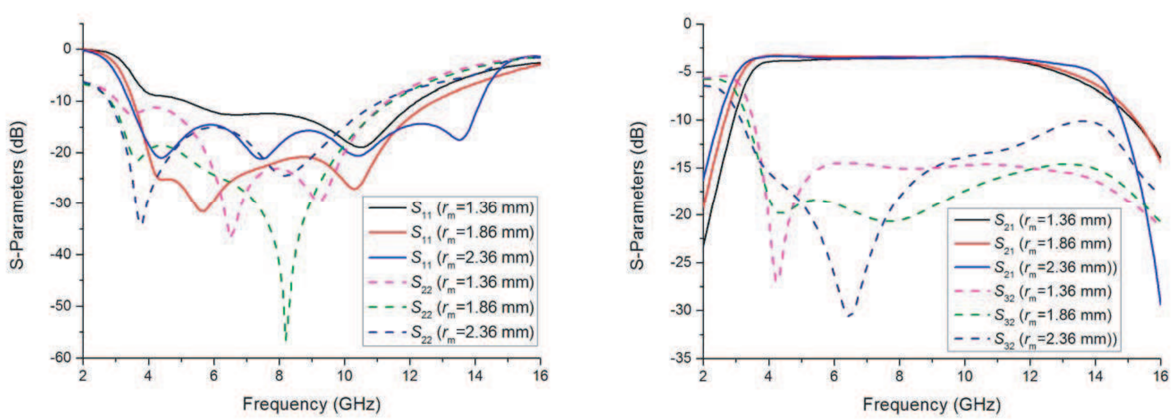


Figure 4. The influence of the length of slotline on flatness.



(a) (b)

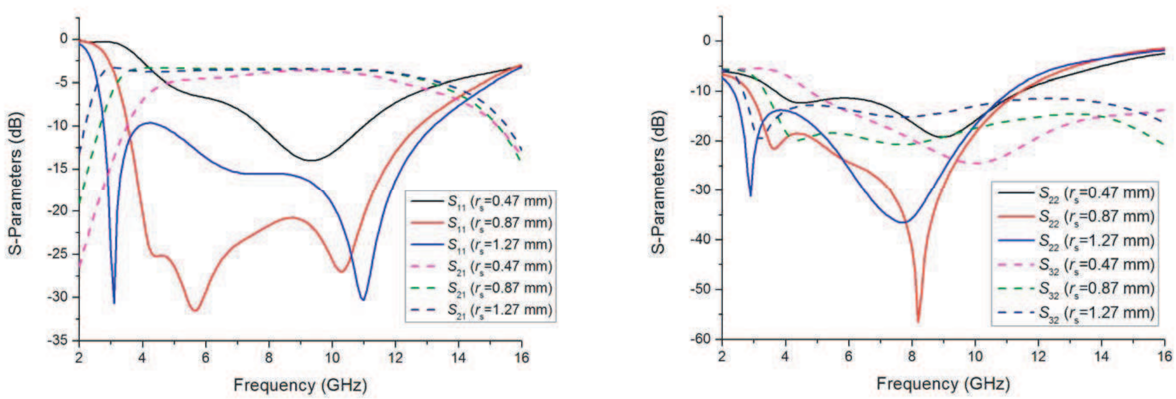
Figure 5. The influence of rm on frequency response. (a) The influence on return losses at input and output ports. (b) The influence on insertion loss and isolation.

two dividing signals with equal amplitude and phase, this proposed power divider is symmetrical.

For understanding the influence of parameters of the proposed power divider on frequency response in detail, more studies about the designed power divider have been done. Figures 5–7 show the influence on frequency response with different dimensions. As exhibited in Figure 5, the size of the compensatory circular open-circuited microstrip stub will not affect the flatness of the passband (S_{21}). The return losses at all ports, however, will be worsened because the change of microstrip stub will make the ports mismatched. To obtain good impedance matching, the radius of the circular microstrip stub is usually chosen as about $\lambda_m/12$. λ_m is the wavelength of microstrip line at center frequency point.

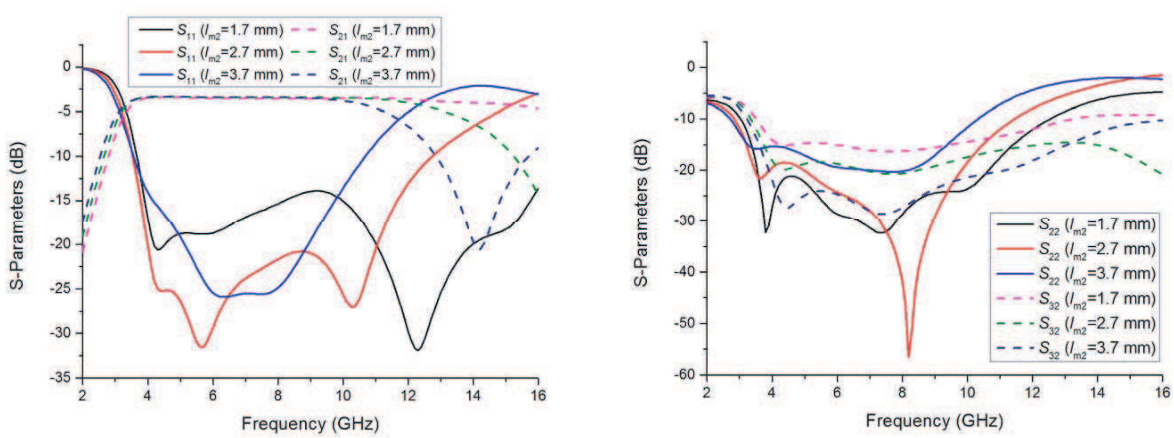
In Figure 6, the influence of r_s on the frequency response has also been researched. The width of operating band will increase with the radius of short-circuited slotline stub increasing. In addition, the size of slotline stub will affect the impedance matching, too. Usually, radius r_s is selected as about $\lambda_s/24$ to obtain good impedance matching. λ_s is the wavelength of slotline at center frequency point.

In Figure 7, the influence of another microstrip stub on frequency response is studied. Different from the microstrip stub at input port, the size of this stub at output port will affect the width of operating band. With the length of l_{m2} increasing, the width of operating band will decrease. The influence of l_{m3} is the same as that of l_{m2}. Their total length is about a quarter wavelength.



(a) (b)

Figure 6. The influence of r_s on frequency response. (a) The influence on insertion loss and return losses at input port. (b) The influence on isolation and return loss at output port.



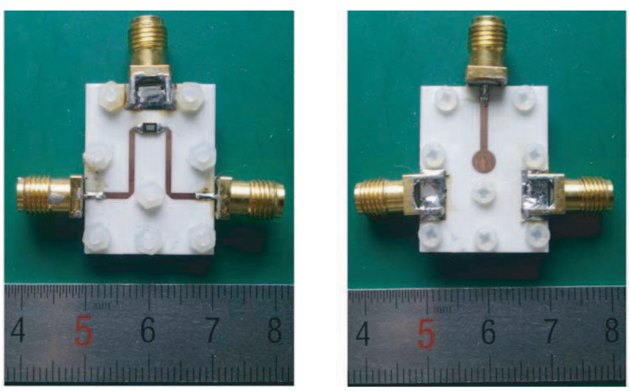
(a) (b)

Figure 7. The influence of l_{m2} on frequency response. (a) The influence on insertion loss and return losses at input port. (b) The influence on isolation and return loss at output port.

3. EXPERIMENTAL RESULTS

The presented UWB in-phase multilayer power divider with high isolation is designed and fabricated on Rogers 4003C substrate with dielectric constant of 3.38, thickness of 0.508 mm, and loss tangent of 0.0023. Figure 8 shows the fabricated multilayer in-phase power divider with high isolation. As mentioned above, the length of slotline is shorter than the ones designed in [9–13]. This change will not only make the process on lumped resistor more easy, but also diminish the size of the power divider. Although a small dielectric constant has been used, the practical UWB power divider is very compact with a size of 25 mm × 20 mm. The dimensions, which have been optimized by EM simulation software HFSS V13.0, about the practical power divider are listed as (units: mm): $w_m = 1.16$, $w_{m1} = 0.89$, $w_s = 0.23$, $r_m = 1.86$, $r_s = 0.87$, $l_{m1} = 6.66$, $l_{m2} = 2.7$, $l_{m3} = 2.23$, $l_s = 6.5$. The value of the lumped resistor R is 100 Ω.

The simulated and measured results, which show a good agreement, are exhibited in Figures 9–11. In the frequency range 3.8 GHz–10.4 GHz, the measured return loss at input port (S_{11}) is better than 15 dB, while the simulated one is better than 20 dB. The simulated and measured return losses at output port (S_{22}) are about 18 dB and 15 dB, respectively. Besides, the measured isolation between



(a) (b)

Figure 8. Photographs of the presented power divider with high isolation. (a) Top view. (b) Bottom view.

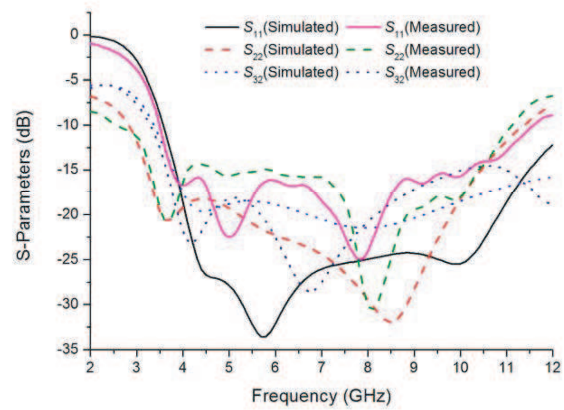


Figure 9. Simulated and measured return loss, isolation of the proposed power divider.

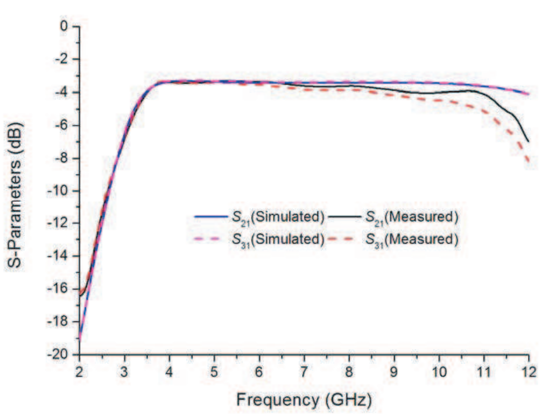


Figure 10. Simulated and measured insertion loss of the novel power divider.

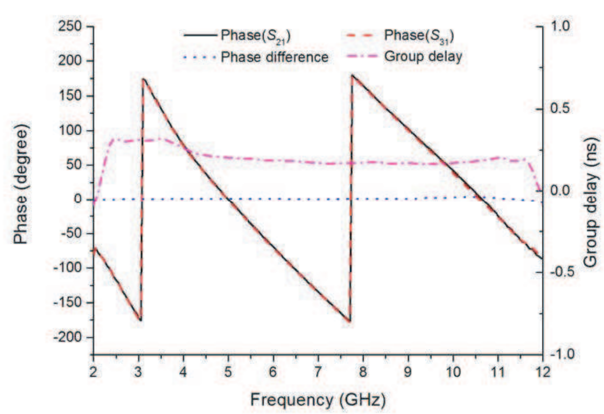


Figure 11. Measured phase difference and group delay.

output ports (S_{23}) is about 16 dB, while the simulated one is about 20 dB. Compared with the ones in [9–13], the return loss at output port and the isolation of this UWB multilayer power divider have been improved approximately 8 dB and 10 dB, respectively over the band from 3.8 GHz to 10.4 GHz.

The measured insertion loss is about 1 dB, which is a little bit bigger than the simulated one. The measured amplitude unbalance is about 0.5 dB. The difference between simulated and measured data results from the machining error.

The results about phase difference and group delay are shown in Figure 11. The measured phase difference that represents the phase unbalance is about 1° over the range from 3.8 GHz to 10.4 GHz. The group delay which shows a good flatness is about 0.25 ns over the same frequency band.

4. CONCLUSION

A new UWB multilayer in-phase power divider with high isolation has been analyzed and designed by using slotline techniques. By breaking through conventional configuration for slotline and introducing one lumped resistor, the isolation between output ports as well as the return losses at output ports have been improved greatly compared to the antecedent ones. In addition, this novel power divider also exhibits good performance on insertion loss, amplitude and phase balances, and group delay over the band from 3.8 GHz to 10.4 GHz.

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