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# Generic InP-Based Integration Technology: Present and Prospects

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(*Invited Review*)

**Abstract**—The generic foundry approach will lead to a revolution in micro and nanophotonics, just as it did in microelectronics thirty years ago. Generic integration leads to a drastic reduction in the entry costs for developing Photonic Integrated Circuits. Integrated circuits using generic integration open up a whole new range of applications including data communications, fiber-to-the-home, fiber sensors, gas sensing, medical diagnostics, metrology and consumer photonics. Present status and prospects of InP-based photonic foundry technology are reviewed.

## 1. INTRODUCTION: THE DEVELOPMENT OF PHOTONIC CHIP COMPLEXITY

In microelectronics there is a clear exponential development in the number of transistors per chip, which has been doubling every two years on average during the last four decades. This phenomenon is known as Moore's law [1, 2]. In Photonics we observe a similar development, albeit in an early stage. Figure 1 shows the complexity development of InP-based Photonic ICs (PICs), measured as the number of components integrated on a single chip.

Early examples of complex InP-based PICs are a WDM source by Koren et al. (1989) [3], a grating-based receiver by Cremer et al. (1991) [4], a switch array by Gustavsson et al. (1992) [5], and a heterodyne receiver by Kaiser (1994) [6]. The highest complexities so far have been reported in AWG-based PICs. It started with the publication of the first AWG by Smit [7] in 1988, followed by Takahashi et al. (1990) [8] and Dragone (1991) [9]. After the invention of the AWG a number of AWG-based devices with increasing circuit complexity was reported: WDM receivers with 5–10 components by Amersfoort et al. (1993) [10], Zirngibl et al. (1995) [11] and Steenbergen et al. (1996) [12]; WDM lasers with 10–20 components by Zirngibl et al. (1994, 1996) [13, 14] and Staring et al. (1996) [15]; WDM channel selectors with 10–20 components by Zirngibl and Joyner (1994) [16], Ishii et al. (1998) [17], Menezo et al. (1999) [18], Mestric et al. (2000) [19] and Kikuchi et al. (2001) [20] and a crossconnect chip with 66 components by Herben et al. (1999) [21].

A special device is the WDM-receiver with integrated pre-amplifiers by Chandrasekhar et al. (1995) [22] which counts 81 components, most of them electronic (transistors and resistors). The new century brought a significant increase in complexity: WDM receiver and transmitter chips with 44–51 components by Tolstikhin (2003) [23], ThreeFivePhotonics (2004) [24] and Infinera (2005) [25]. Shortly after, in 2006, Infinera published a 40-channel WDM transmitter with 241 components [26]. Recent devices with a very high complexity are an all-optical tunable $8 \times 8$ wavelength router with more than 175 components by Nicholes et al. [27] in 2009 and a 100-channel Arbitrary Waveform Generator with more than 300 components by Soares et al. [28] in 2010. The latter device also contains 400 phase shifters for reducing the high crosstalk level in the very large AWG which is used to separate 100 wavelength channels. Recently, Infinera reported a PM-DQPSK transmitter with more than 400

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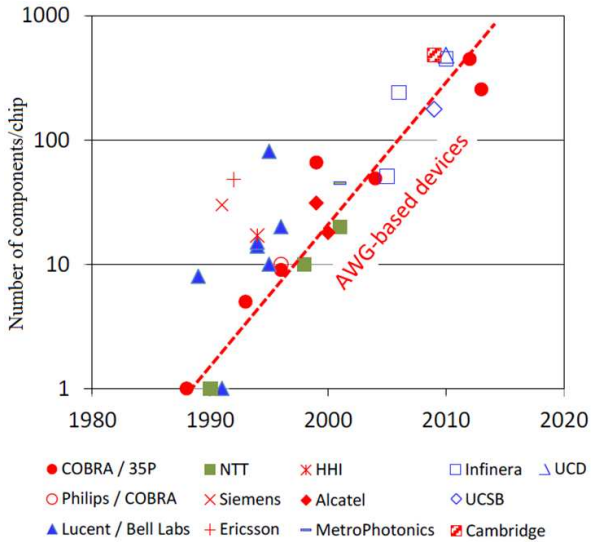


| Year | #comp | Short Title | 1st Author | Institute | Ref. |
|---|---|---|---|---|---|
| 1988 | 1 | AWG | Smit | COBRA | [7] |
| 1989 | 8 | WDM source | Koren | Bell Labs | [3] |
| 1990 | 1 | AWG | Takahashi | NTT | [8] |
| 1991 | 30 | Grating Spectrograph | Cremer | Siemens | [4] |
| 1991 | 1 | AWG | Dragone | Bell Labs | [9] |
| 1992 | 48 | Switch Array | Gustavsson | Ericsson | [5] |
| 1993 | 5 | WDM receiver | Amersfoort | COBRA | [10] |
| 1994 | 12 | Heterodyne receiver | Kaiser | HHI | [6] |
| 1994 | 14 | WDM laser | Zirngibl | Bell Labs | [13] |
| 1994 | 15 | WDM channel selector | Zirngibl | Bell Labs | [16] |
| 1995 | 10 | WDM receiver | Zirngibl | Bell Labs | [11] |
| 1995 | 81 | WDM receiver and preamp | Chandrasekhar | Bell Labs | [22] |
| 1996 | 9 | WDM receiver | Steenbergen | COBRA | [12] |
| 1996 | 20 | WDM laser | Zirngibl | Lucent | [14] |
| 1996 | 10 | WDM laser | Staring | Philips | [15] |
| 1998 | 10 | WDM channel selector | Ishii | NTT | [17] |
| 1999 | 66 | WDM Crossconnect | Herben | COBRA | [21] |
| 1999 | 31 | WDM laser | Menezo | Alcatel | [18] |
| 2000 | 18 | WDM channel selector | Mestric | Alcatel | [19] |
| 2001 | 20 | WDM channel selector | Kikuchi | NTT | [20] |
| 2003 | 45 | WDM receiver | Tolstikhin | Metro | [23] |
| 2004 | 49 | WDM receiver | 35 Photonics | 35Photonics | [24] |
| 2005 | 51 | WDM transmitter | Nagarajan | Infinera | [25] |
| 2006 | 240 | WDM transmitter | Kato | Infinera | [26] |
| 2009 | 177 | Tunable WDM router | Nicholes | UCSB | [27] |
| 2010 | 302 | Arb. Waveform Generator | Soares | UCD | [28] |
| 2010 | 400 | PM-DQPSK WDM transm. | Corzine | Infinera | [29] |

**Figure 1.** Development of chip complexity measured as the number of components per chip. The number of components, counts the number of basic components like AWGs, MMIs, SOAs and modulators. It does not count for the fact that a DFB laser is more complex than an MMI coupler, for example, so a higher number does not always mean a more complex chip. In the table, the last column refers to the references listed at the end of this article.

components, the most complex PIC reported so far [29]. Figure 1 shows a more or less exponential increase in complexity, with a much larger scatter than its microelectronic counterpart. If we restrict ourselves to devices based on AWGs, with a more or less comparable technology (integrated amplifiers and/or detectors) most of the outliers disappear as can be seen in the "clean" photonic Moore's law shown in Figure 5.

### 1.1. Differences between Photonics and Microelectronics

The complexity development of PICs resembles the early development of microelectronics, but there are distinct differences which have prevented the success of microelectronics to be repeated in photonics.

The microelectronics development, described by the Moore's law graph lists the complexity development of commercially applied ICs, whereas most of the points in Figure 1, are about devices which resulted in one or more papers but they did not bring a circuit to the market. The problem with current project funding models is that they tie the technology development closely to an application: to get money it is necessary to present a new clear and challenging application. Usually the technology was fully optimized for that single application, and due to the absence of coordination, every fab developed its own processes. As a result we have almost as many technologies as applications, most of them very similar, but sufficiently different to prevent easy transfer of a design from one fab to another. Owing to this huge fragmentation, the market for these application specific technologies is usually too small to justify their further development into a low-cost industrial volume manufacturing process, *and as result the chip costs remain too high to serve also small and medium volume markets.* This is quite different from micro-electronics where a huge market is served by a small set of integration technologies (most of them CMOS compatible). The solution to the problem in photonics seems obvious: apply the methodology that allowed microelectronics to change our world also to photonic integration. This requires two steps:

- Develop a few generic integration technologies that support realization of a broad range of functionalities.
- Develop a foundry infrastructure for providing low-cost open access to these generic technologies.

Both aspects are introduced, respectively, in Sections 1.2. and 1.3.

### 1.2. Generic Photonic Integration Technology

In micro-electronics a broad range of functionalities is realized from a rather small set of basic building blocks, like transistors, diodes, resistors, capacitors and interconnection tracks. By connecting these building blocks in different numbers and topologies we can realize a huge variety of circuits and systems.

In photonics we can do something similar. Most of the functionality of a PIC is realized from a rather small set of components: lasers, optical amplifiers, modulators, detectors and passive components like couplers, filters and (de)multiplexers. By proper design, these components can be reduced to an even smaller set of basic building blocks. As basic building blocks we need passive devices for combining and splitting of light, both wavelength dependent (filters, wavelength multiplexers) and wavelength

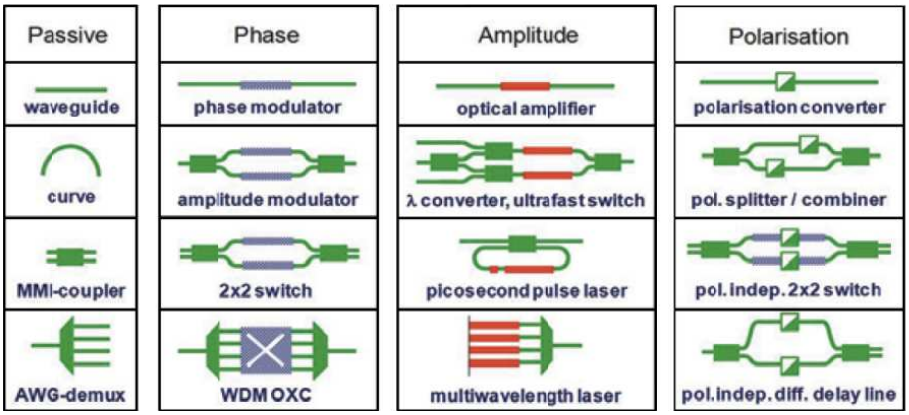


**Figure 2.** Example of the functionalities that can be realized in a generic integration technology that supports four basic building blocks: passive waveguide devices, (optical) phase modulators, semiconductor optical amplifiers and polarisation converters.

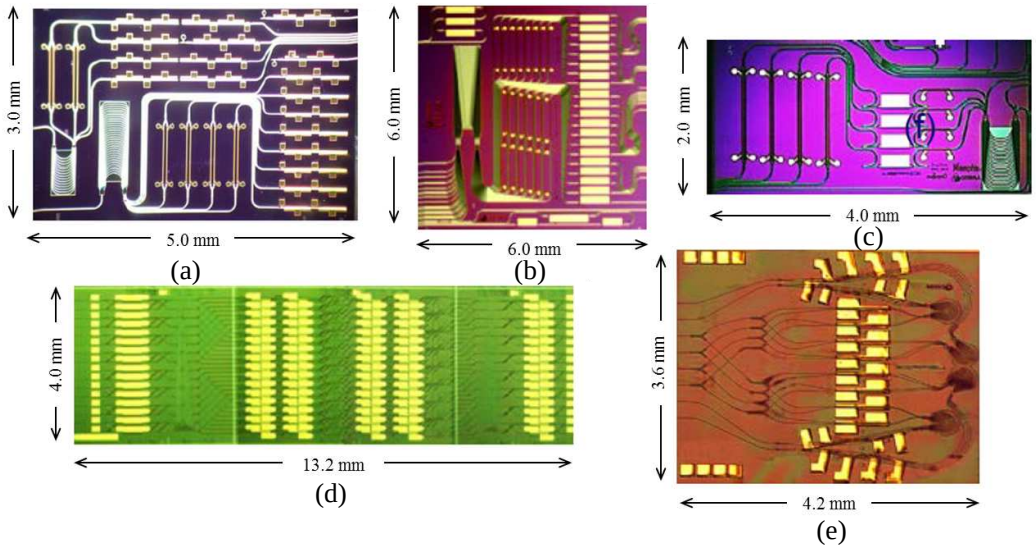


**Figure 3.** Examples of Photonic ICs realised on the generic Oclaro platform: (a) 4 and an 8-channel WDM transmitter. The 8-channel transmitter integrates 74 components on a chip area of $3 \times 5\,\mathrm{mm}^2$, (b) pulse shaper for bio-imaging integrating a 20-channel AWG with 20 SOAs and 20 Phase modulators on a chip area of $6 \times 6\,\mathrm{mm}^2$, (c) filtered-Feedback Multi-Wavelength transmitter on a chip area of $2 \times 4\,\mathrm{mm}^2$; and generic COBRA platform d) Monolithic $16 \times 16$ photonic switch for broadband photonic packet-routing on a chip area of $4 \times 13.2\,\mathrm{mm}^2$, and (e) $4 \times 4$ Space and wavelength selective cross-connect on a chip area of $4.2 \times 3.6\,\mathrm{mm}^2$.

independent (power splitters, couplers and combiners). Most of these devices can be composed of a combination of passive waveguides of different widths and lengths, so in a proper integration process that supports integration of passive waveguides a variety of passive devices, such as MMI couplers and AWGs can be realized. In addition to these passive devices we need basic building blocks for manipulating the phase, the amplitude and the polarization of the light signal, in order to support a broad range of functionalities.

Figure 2 illustrates some functionalities that can be realized in a generic Indium Phosphide technology that supports integration of four basic building blocks: passive waveguide devices, phase modulators, semiconductor optical amplifiers and polarization converters. Most of the functionalities shown in Figure 2 have been reported by us: compact MMI couplers [30] and AWGs [31], optical switches [32] and modulators [33], multiwavelength and tunable lasers [34], flip-flops and ultrafast wavelength converters [35], picosecond pulse lasers [36] and polarization splitters and converters [37].

Figure 3 reports a few examples of Photonic ICs realized on the generic Oclaro platform (Figures 3(a), 3(b) and 3(c)) and COBRA platform (Figures 3(d) and 3(e)). An advantage of generic integration technologies is that, because they can serve a large market, they justify the investments in developing the technology for a very high performance at the level of the basic building blocks. This will make circuits realized in such a technology highly competitive.

Just like in microelectronics different classes of applications need different processes, e.g., for high-voltage, high speed, high power or low power, etc.. In a similar way photonics will need a few different generic technologies, optimized for different kinds of applications, to cover a major part of all applications. But the number of generic technologies that is required is far smaller than the number of technologies which are presently in use.

### 1.3. A Generic Foundry Model in Photonics

Once a mature generic integration technology has been developed it needs to be made accessible with a low entry barrier to a large number of users. After the turn of the century a number of photonic fab owners have opened their fabs to external, so called fabless users. These companies, which call themselves foundries, develop processes for specific customer components and specific customer requirements, in close cooperation with the customer. Usually the process is owned by the customer, who has paid for its development. We call such a foundry, therefore, a custom foundry, and the approach the "custom foundry model". This approach has led to a significant reduction of the entry costs for newcomers, because a newcomer does not have to build his own cleanroom, but shares the costs of the cleanroom with a large number of other fab users. In this model the process development is still application specific, however, so that its costs will not be shared with other users. The entry costs will, therefore, remain significantly higher than in microelectronics, where existing generic foundry processes are available for the development of Application Specific ICs (ASICs), so that not only the cleanroom costs, but also the process development costs are shared by a large number of users. In Photonics, generic foundries, offering access to generic integration processes, were non-existent until recently, but as a result of work done in a number of European projects they are presently emerging. It started in September 2004 with a large number of academic and industrial members with the ambitious mission to move from a model of independent research to a model of integrated research with shared use of expensive technological infrastructure.

In the background were the steadily increasing costs of cleanroom facilities that restricted Photonic Integration research to the ever smaller group of institutes that could afford a cleanroom. The idea was to enlarge the group of users by stimulating cleanroom owners to organize access to their facilities for a broader circle of non-cleanroom owning partners. After experimenting for two years with facility access activities the ePIXnet Steering Committee published a vision document [38] about a foundry model in micro- and nanophotonics and it took the step to the initiation of integration technology platforms.

Two major integration technologies were identified: InP based integration technology, which supports the highest degree of functionality, including compact lasers and amplifiers, and Silicon Photonics technology, which offers most of the functionality offered by InP except for the compact lasers and amplifiers, but at a potentially better performance and lower cost because of its compatibility with mature CMOS technology. For both technologies a platform organization was established: JePPIX for InP-based integration technology [39], and ePIXfab for Silicon Photonics [40]. Later a third platform

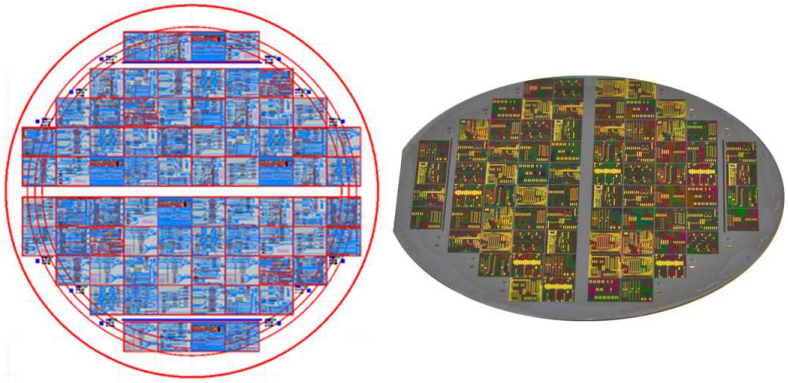

**Figure 4.** Example of a Multi-Project Wafer (MPW) realized on the Generic COBRA platform. The wafer is subdivided in 76 sectors where a few of them are for test structures and the others are for user designs. The left imagine represents the mask layout and the right image is a photograph of the realized wafer.

with dielectric waveguide technology was added (TriPleX), which offers low-loss and high quality passive optical functions and some thermo-optic active functions, through the whole wavelength range from visible to infrared [41]. All three platforms started by providing open access for research purposes to a relatively mature integration technology: the JePPIX platform to the InP-based integration technology of the COBRA institute of TU Eindhoven and later also the platform technologies of Oclaro and Fruanhofer HHI, the ePIXfab platform to the SOI-technology of IMEC and LETI, and the TriPleX platform to the technology of the Dutch company Lionix. All three platforms offer access to their technologies through Multi-Project Wafer Runs (MPWs) (Figure 4), a well-known concept in microelectronics, but not earlier applied in Photonics.

MPWs lead to a significant reduction of the costs of chip R&D by combining test versions from different users in a single wafer run, so that the costs of a run are shared by several users. Each pattern is repeated a number of times on a wafer, so that each user will get several samples of his chip. Figure 4 shows a multi-project wafer combining designs from 14 different users, and each user gets 6 chips.

The initiatives taken by ePIXnet were first steps towards full introduction of the generic foundry model in photonics. In a fully operational model the following activities have to be addressed: 1. access to mature and well documented commercial foundry processes via full or MPW runs; 2. availability of dedicated design software and component libraries for enabling fast and accurate design (design kits); 3. brokering service: assistance and training of users that are not familiar with the technology. Assembling different user designs in a mask set for an MPW-run; 4. design houses that can help users that do not have the know-how to design their own chips; 5. access to generic test facilities; 6. access to generic packaging facilities.

This model is well known in microelectronics for the development and manufacturing of ASICs. The ePIXnet integration technology platforms are presently gaining experience with all these activities at a research level, but a number of projects have been started for moving the foundry model from the research to the industrial stage and introducing ASICs in photonics, where we will call them ASPICs: Application Specific Photonic ICs.

About silicon photonics the generic integration model is well consolidated and many fab owners provide high-performance silicon photonics cells and design tools to fabless users [42].

### 1.4. Prospect for Generic Photonic Integration

A generic foundry model will lead to a dramatic reduction of the costs of PIC R&D and manufacturing for small or medium volumes and to a significant shortening of the R&D cycle. Through access to an existing well documented high performance process the relatively high entry costs of process development, which form a major cost contribution in the custom foundry model, are strongly reduced through cost sharing with many users. A further reduction of the R&D costs is achieved by combining designs of several

users in a single MPW run, the costs of which are shared by all participating users and through the availability of accurate design software the number of R&D cycles needed for getting a chip onto specs will be strongly reduced. Another time and cost reduction is obtained in testing and qualification of the chip, which is a major cost factor for chips for which reliable operation is required under harsh conditions. A large part of the qualification applies to the manufacturing and packaging process and this part need not be repeated for each individual product, but it applies to all ASPICs that are developed according to the design rules. Due to these cost and time advantages the costs of PIC R&D and manufacturing in the generic foundry model will be reduced by more than a factor of ten for small and medium volumes, as compared to the custom foundry model. More details about the cost reductions in the generic foundry model are given in [43]. Such a large reduction of R&D time and chip manufacturing costs will lead to a large growth of the share of PICs in the photonic components market.

Even though generic processes will not be the solution for any application they will be competitive for a broad range of applications. For InP-based generic integration, for example, the foundry processes that are being developed in the EuroPIC and the PARADIGM process are based on existing integration platform technologies for high performance tunable lasers and high speed receivers. The research is focused on extending the functionality of these platform technologies without loss of performance for the individual building blocks. It combines a broad functionality with a high performance on the level of the individual building blocks, and we expect that through focused investments in a few generic technologies their performance will increase steadily and outperform ever more application specific technologies, similar to what happened with CMOS in microelectronics.

So far the use PICs has been mainly restricted to some niche areas in telecom applications, where their specific functionality cannot be met by competing technologies. With the expected cost reductions through a generic foundry approach they will also become competitive in high volume markets like the telecom access network, where they may be applied in the Central Office for integration of larger numbers of circuits that have to be repeated for each subscriber or group of subscribers. In future 10 Gb/s access network they may become competitive also in the subscriber transceiver module.

But when R&D and manufacturing costs drop, photonic chips will increasingly penetrate also other applications. A good example is the fiber sensor market, which was over 300M$ in 2007 with double digit annual growth figures. A significant part of the sensor costs is in the readout unit, which contains a light source, a detector and some signal processing circuitry. Here Photonic ICs can replace a significant part of the existing modules, and enable novel sensor principles. Examples are various types of strain sensors, heat sensors and a variety of chemical sensors [44]. Optical Coherence Tomography is another potential application. Traditionally OCT is done in the 800 nm window, which is the preferred choice for retina diagnostics. For skin or blood vessel diagnostics 1500 nm is a better wavelength, because there the penetration depth is three times as large due to reduced scattering losses at this wavelength. This provides good opportunities for InP PICs in OCT equipment [45]. An interesting class of devices are

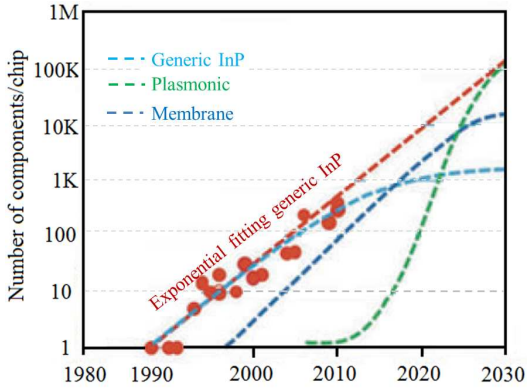


**Figure 5.** Complexity development of Photonic Integrated Circuits. The red-dotted line represent the exponential fitting according with development of chip complexity measured as the number of components per chip.

pico- and femtosecond pulse lasers [46]. Here PICs containing mode locked lasers, optionally combined with pulse shapers, can provide small and cheap devices that can be used in widely differing applications, such as high-speed pulse generators and clock recovery circuits, ultrafast AD-converters, and in multi-photon microscopy. These are just a few examples.

Once ASPICs get really cheap they will offer ample opportunity for small and large companies to improve their competitiveness by applying them in their products. A more extensive discussion of a foundry model for InP-based Photonic ICs is given in [43]. Alternative visions on the development of Photonic Integration are given in [47, 48].

We expect that in the second half of this decade the market for Photonic ICs will strongly increase when low-cost access to Photonic IC-technology will become available through commercial foundries. We do not expect, however, that with the present technology this market growth will be accompanied by a strong further increase in chip complexity.

In passive devices unavoidable component losses will restrict the total number of components that can be cascaded, and in active PICs SOAs and lasers typically have a power dissipation of several 100 mW. So their number is restricted to several tens up to a maximum of a few hundreds, because of heat sinking limitations. Secondly, although today's PICs often carry digitally modulated signals, the basic building blocks and the circuits built from them essentially operate in an analog mode, which means that on passing a number of components the signal will accumulate noise and distortion and needs to be regenerated. Regenerators can be integrated too, but they consume space and power.

We expect, therefore, a saturation of chip complexity at a level in the order of 1000 components per chip, as indicated in Figure 5 by the curve labeled "Generic InP". This does not mean that the complexity development of photonic chips will end at that level. For higher complexity levels we will have to move to other technologies, which will be discussed in the next sections.

## 2. THE NEXT GENERATION: INDIUM PHOSPHIDE MEMBRANE ON SILICON

A larger complexity can be supported, in principle, in membrane based circuits, where component dimensions and power dissipation can be significantly smaller. This is a consequence of the strong light confinement in thin membranes with a high vertical refractive index contrast, as they are presently applied in Silicon Photonics. In the past years silicon membrane technology has seen a great improvement in performance and maturity. Because in many cases smaller also means faster and lower power consumption, membrane technologies are a promising candidate for becoming the next generation generic integration technologies. A serious problem that has to be addressed is the integration of active devices. Recent research has demonstrated the feasibility of high speed modulators and detectors using SiGe technology [49]. The main remaining problem in silicon based photonic ICs is the generation and amplification of light: being an indirect semiconductor silicon is not suitable for fabricating compact and efficient light sources and amplifiers. Several interesting ideas have been pursued to obtain monolithic integration of light sources in silicon photonics. These include porous Si [50], Si nanocrystals [51], Er-doped Si [52] and using GeSn [53]. In 2010 MIT [54] has proposed and demonstrated that gain can be obtained from strained and heavily n-doped Ge grown on Si. So far the performance of these lasers is still far away from the performance of direct bandgap semiconductor lasers on GaAs and InP. Therefore, the most promising silicon membrane integration platforms aim at using III-V lasers. Four different approaches are depicted in Figure 6. IBM [55] and MIT [56] follow an approach in which light is coupled into the silicon membrane from an external source (Figure 6(a)).

In Figure 6(a) the technologically least challenging approach is reported, which is the best candidate for early applications. However, due to the lack of on-chip light generation and amplification, the scalability of this approach to higher circuit complexities is limited. This is the main reason that up till now the complexity of silicon photonic ICs is lagging behind InP, with 86 components per chip being the highest complexity reported so far [57]. IMEC, LETI and COBRA are currently working on an approach in which lasers and detectors are fabricated in a III-V layer stack on top of the silicon membrane, in such a way that the light tunnels to the silicon layer through a thin low-index layer [58] (Figure 6(b)). In this approach it is difficult to get efficient coupling to the silicon layer, however, especially if the devices get smaller. UCSB and Intel apply a slightly different approach, in which the silicon waveguide is provided with gain by atomic bonding of an active III-V layer stack directly onto

the silicon membrane [59] (Figure 6(c)). Also in this approach coupling of the light from the active layer to the passive silicon waveguide remains difficult because the requirements for high confinement and high coupling efficiency are contradictory.

We have, therefore, chosen another approach in which we replace the silicon membrane with an InP-membrane; IMOS: InP Membrane On Silicon (Figure 6(d)). The major advantage of InP-based membranes over, for example, Si-based membranes is the possibility to integrate active devices (lasers, amplifiers).

The basic fabrication steps of IMOS devices are represented in Figure 7. It starts from a layer structure containing a 200 nm InP-membrane layer on top of three etch-stop layers (InGaAsP-InP-InGaAsP) on an InP-substrate.

In this layer stack a pattern is defined by e-beam lithography with a positive resist on a 50 nm thick $SiN_x$ layer, deposited by plasma-enhanced chemical vapor deposition (PECVD). After development and post-bake of the resist, the layer is etched with a $CHF_3$-based reactive ion etching (RIE) to transfer the pattern into a hard mask. The resist post-bake reduces the sidewall roughness, which is critical for low propagation losses. A $CH_4/H_2$-based ICP etching step follows to etch the open part through the whole InP membrane. Finally, the $SiN_x$ hard mask is removed with a hydrofluoric acid solution.

After the pattern definition, a BCB layer is spin-coated onto the InP-sample and cured for 1 hour at 250°C in a nitrogen environment. Then, the sample is bonded onto a host-substrate with a thick BCB layer. This BCB layer is also cured for 1 hour at 250°C in a nitrogen environment. The InP-substrate is removed using wet-etching in HCl until the InGaAsP etch stop layer is reached. Finally, the InGaAsP-InP-InGaAsP etch-stop layer stack is removed using three selective wet-etching steps. Active regions are created locally in this membrane prior to bonding, using selective epitaxial regrowth techniques on a submicron scale (Figure 6(d)).

This concept promises a number of important advantages. As both active and passive functions are now realized in one membrane, coupling between them is no longer a critical issue. Also, the requirements on alignment with respect to the underlying substrate are much alleviated, because there is only electrical coupling between the photonic membrane and the underlying electronics and the

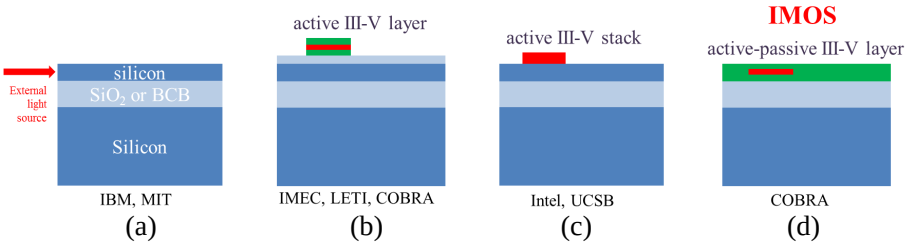


**Figure 6.** Schematic representation of four approaches to generate light in a photonic layer on top of a silicon IC: (a) the light is coupled from an external source into the passive circuit, (b) the light is coupled from a laser source which is processed on top of the passive circuit, (c) an active InGaAsP/InP layer is bonded and processed on top of the passive circuit, and (d) the silicon membrane is replaced with an InP-membrane that contains both passive and active regions (IMOS).

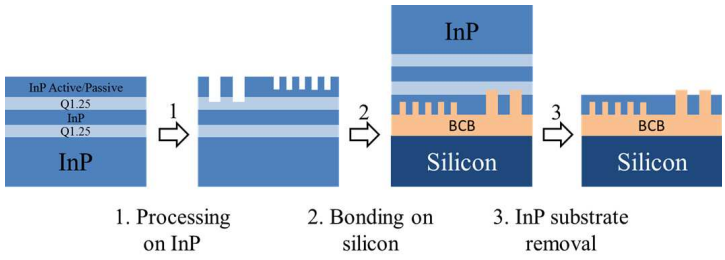


**Figure 7.** Fabrication of IMOS devices.

much more critical optical coupling is avoided. Finally, because we use a thick polymeric layer for bonding of the InP-membranes on a substrate, the realization becomes virtually independent of the surface morphology. This is important for future combination of IMOS photonic integrated circuits with CMOS circuitry. The optical properties of an InP-membrane for passive optical components are very similar to those of a silicon membrane.

We have already demonstrated a number of high quality passive components in IMOS technology: photonic wires with 7 dB/cm losses (Figure 8(a)), extremely small MMI-couplers with only 0.6 dB excess loss (Figure 8(b)) curved waveguides with only 5 µm bending radius and negligible loss (Figure 8(c)), and ring filters with a $Q$-factor larger than 15000 [60].

Recently, in [61] we also reported a 0.25 $mm^2$ footprint eight-channel planar concave grating demultiplexer fabricated in a 300-nm-thick InP membrane adhesively bonded to silicon (Figure 8). The measured crosstalk between the different channels of the device is better than −18 dB, while the insertion loss is 2.8 dB. Being realized in an InP membrane, the device is suitable for integration with active devices in InP-based membranes on silicon platforms.

However, to achieve a full set of devices for a photonic integration platform more is needed. A key device for the development of a photonic integration platform is the polarization converter. We already proposed an ultrasmall ($< 10$ µm length) polarization converter in IMOS (Figure 9). The device relies on the beating between the two eigenmodes of chemically etched triangular waveguides. Measurements show a very high polarization conversion efficiency of $> 99\%$ with insertion losses of 1.2 dB at a wavelength of 1.53 µm. Furthermore, our design is found to be broadband and tolerant to dimension variations [62].

The most important part in creating a photonic integration platform in a membrane technology is including active devices: lasers and amplifiers. We have achieved encouraging results for selective growth of very small active regions [63]. Figure 10 shows a disc-shaped active region of 250 nm radius, containing four quantum wells designed for light emission at $\lambda = 1.55$ µm. After the regrowth these very small active regions show light emission.

Successful active-passive integration with submicron active regions in membranes is an essential step to obtain the complete development of the IMOS. The active–passive integration should satisfy two critical conditions: *first*, a smooth and flat interface should be realized between the active and passive materials. A rough interface causes both reflection and scattering loss when light is coupled between active and passive regions. Meanwhile a good surface flatness is required for processing

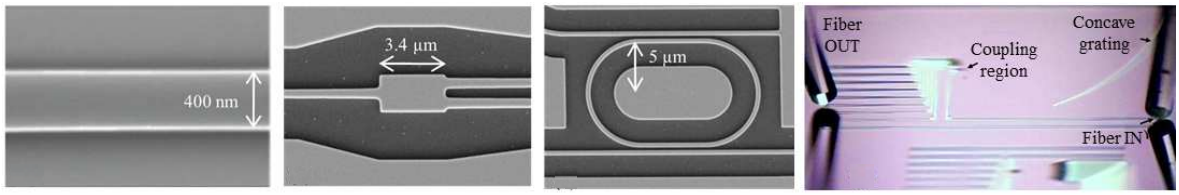


**Figure 8.** SEM pictures of IMOS components: (a) waveguide, (b) MMI splitter, and (c) race-track ring resonator, d) Microscope picture of an eight-channel planar concave grating.

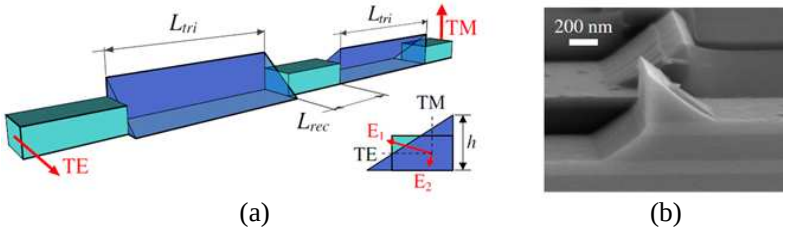


**Figure 9.** Schematic representation of the polarization converter with (Inset) representation of the triangular waveguide eigenmodes and electron microscope photograph of a fabricated device.

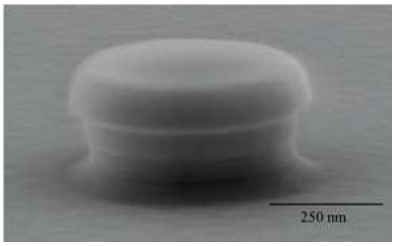


**Figure 10.** A sub-micron active region before regrowth.

and bonding of membranes. *Second*, since the smallest active regions are around submicron size, it is possible that the active quantum well materials will be damaged by the processing. Due to the smaller component dimensions and power consumption of membrane devices we expect that membrane technologies with efficient and compact integrated light sources and amplifiers will allow for a complexity an order of magnitude higher than classical InP-photonics, as indicated in Figure 5 by the curve labeled "membrane".

However, a number of problems still need to be addressed before the concept is fully operational. A technique has to be developed to efficiently supply currents and voltages to the active devices on the membrane. Furthermore, also the thermal management and the mechanical stability of the membranes need to be addressed. Our next research efforts will focus on these issues.

## 3. CONCLUSIONS

By applying the methodology of microelectronics to photonics we expect a dramatic reduction of the costs for R&D and manufacturing of photonic ICs and a breakthrough to a wide range of application fields, in telecommunications and data communications, but also for application in sensors, medical equipment, metrology and consumer photonics. Such a breakthrough will accelerate the development of more advanced integration technologies. Parts of this article have been published earlier in [64].

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