A Method for Designing Broadband Doherty Power Amplifiers

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Abstract—In this contribution, a design approach for the realization of broadband Doherty Power Amplifiers (DPAs) is proposed and demonstrated. The methodology is based on the exploitation of the wideband response of 2-sections branch-line couplers both as input splitter and output combiner of the DPA. These couplers are designed through a CAD optimization process which is specifically oriented to the development of DPAs. The method is also applied to realize a GaN based hybrid prototype that shows more than 36% of fractional bandwidth around 2 GHz frequency range, validated through single carriers and modulated signals (3gpp and WiMax). In single carrier mode an efficiency higher than 41% (> 50% in saturation, with a peak of 72%) is obtained in 6 dB of output power dynamic range in the entire operating band. Experimental results with 5 MHz 3gpp and WiMax signals shown an average efficiency of 50% and 45% when 37 dBm and 34 dBm of average output power are reached, respectively.

1. INTRODUCTION

The future communications aim to achieve an efficient use of radio spectrum and available energy, by developing fully reconfigurable and adaptable systems able to assure connectivity in any operative scenario [1,2]. In this context, the development of power amplifiers that can efficiently operate in different frequency bands and with many communication standards is a *sine-qua-non* condition [3,4].

The efficiency benefits that the Doherty Power Amplifier (DPA) allows with the most powerful communication standards, characterized by high peak-to-average power ratio (PAPR), are largely documented [5–8]. The new frontier to make this architecture suitable for the transmitters of the future systems is the development of methods and solutions to realize DPAs able to operate at different frequency bands and with different standards.

The first step towards this goal has been proposed in [9] with the development of a topology to realize concurrent dualband DPAs, then improved in [10–14] and finally extended to three bands in [15]. However, a multiband DPA approach allows to operate only in predefined frequency bands. In order to realize an hardware fully adaptable and reconfigurable in frequency, broadband DPAs design approaches are required.

The frequency limitation of the conventional DPA, in which the output combiner is realized by means of a $\lambda/4$ transformer, has been analyzed in [16]. In the same paper it is also shown that a reduction of the impedance transformation ratio leads to a bandwidth extension. A frequency compensation approach of the conventional output combiner is, instead, proposed in [17], demonstrating 18.2% of fractional bandwidth. The replacement of the conventional combiner with an equivalent semilumped network with broadband behaviour is suggested for MMIC designs in [18], achieving 26% of fractional bandwidth, even though with a large gain ripple (about 6 dB). However, the best bandwidth enlargements of the DPAs are demonstrated when the adopted circuital scheme is different from the conventional one: a solution based on real frequency technique is proposed in [19], while the Klopfenstein taper approach is exploited in [20]. An unconventional solution for both output combiner and input

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splitter of the DPA is also presented in this contribution, demonstrating state-of-art results in terms of fractional bandwidth and gain ripple.

The idea here described starts from [21], where we have proposed a new output combiner based on a single-section branch-line coupler, with an open circuit at the fourth port. Analogously, the input power splitter was realized by using a single-section branch-line coupler, thus self-compensating the output $\lambda/4$ phase response. A 15% of fractional bandwidth with a maximally flat efficiency behavior has been achieved with that solution [22].

In order to obtain a larger bandwidth capability, 2-sections branch-line couplers [23–26] are here adopted both at the output and at the input of the DPA, achieving more than 35% of fractional bandwidth. Both couplers are designed with a computer-aided approach, whose a detailed description is reported in Section 2. The benefits of the methodology are validated designing a GaN-based hybrid prototype, described in Section 3. The experimental characterization with single carrier, 3gpp and WiMAX signals in the operating frequency range (1.7–2.4 GHz) is reported in Section 4.

2. DESIGN APPROACH

A DPA can generally be represented as two amplifiers, namely Main and Auxiliary, joined by suitable input splitter and output combiner, as shown in Fig. 1. On how these networks are implemented, independent of other aspects, for low input power levels, only the Main amplifier is active. At a defined input power level, from hereafter referred as *break point*, the Auxiliary amplifier starts to conduct, modulating the load of the Main amplifier up to the saturation. The output power range between the break point and the saturation is defined as the output back-off (OBO) of the DPA.

In order to obtain high efficiency levels in the OBO range, proper output loading conditions for both amplifiers at break and saturation have to be fulfilled. These loading conditions, R_M for the Main and R_A for the Auxiliary, can be computed by the design requirements and active device characteristics [27]:

$$R_{M,break} = \frac{(V_{DD} - V_k)^2}{2 \cdot \alpha^2 \cdot P_{sat}}$$

$$R_{M,sat} = \frac{(V_{DD} - V_k)^2}{2 \cdot \alpha \cdot P_{sat}}$$

$$R_{A,sat} = \frac{(V_{DD} - V_k)^2}{2 \cdot (1 - \alpha) \cdot P_{sat}}$$
(1)

where P_{sat} is the saturated output power of the overall DPA, V_{DD} the drain bias voltage, and V_k the device knee voltage, assumed to be the same for both devices. The parameter α is related to the OBO (defined in decibels) by

$$\alpha = 10^{\frac{\text{OBO}}{20}} \tag{2}$$

Thus, considering a classical design with 6 dB of OBO, i.e., $\alpha \approx 0.5$, it follows:

$$R_{M,sat} \approx R_{A,sat} \approx 0.5 \cdot R_{M,break} \tag{3}$$

The value of $R_{M,sat}$ is usually selected equal to the optimum load resistance (R_{opt}) of the active device.



Figure 1. Generalized blocks diagram of a DPA..



Figure 2. Generalized circuit that realize the active load modulation.

The role of the output combiner is to allow the loading conditions in (3) in the entire operating frequency range. However, a broadband output combiner is not sufficient to assure a wideband behavior for the DPA. In fact, the loads $R_{M,sat}$ and $R_{A,sat}$ are obtained by means of the active load modulation. Its generalized analytical description, derived by the circuit in Fig. 2, is:

$$Z_{1} = R \left(1 + \frac{I_{2}}{I_{1}} e^{i(\phi_{2} - \phi_{1})} \right)$$

$$Z_{2} = R \left(1 + \frac{I_{1}}{I_{2}} e^{i(\phi_{1} - \phi_{2})} \right)$$
(4)

Equations in (4) highlight the need to have the proper ratio (I_1/I_2) and phase relation $(\phi_1 - \phi_2)$ between the output currents of the active devices in the entire frequency range. Since the output currents directly depend on gate voltages, the role of the input splitter is to assure the proper driving voltages (magnitude and phase) in the operating frequency range.

As it will be demonstrated, the 2-sections branch-line coupler can be adopted in DPAs to play the role of both the output combiner and input splitter in a wide frequency range. In the following subsections, the methodology to properly design these structures is presented.

2.1. Output Combiner

The scheme of the output combiner, based on a 2-sections branch-line coupler topology, is reported in Fig. 3.



Figure 3. Branch-line-like network to be used as output combiner in DPAs.

The proposed structure has to combine on port 4 the powers coming from Main and Auxiliary amplifiers, connected to ports 1 and 2, respectively. To allow a constructive power combination, the signal of the Auxiliary amplifier has to be 90° phase shifted with respect to the signal of the Main. The output termination is placed on port 4, to interpose an odd number of $\lambda/4$ transmission line sections between it and the Main amplifier. This condition is mandatory to assure the decreasing of the output load seen by the Main amplifier in the OBO range [27]. Port 3 of the combiner is open circuit terminated to avoid power losses when the amplifiers are delivering different power levels.

Since the output combiner has to transform the 50Ω termination into the optimum loading conditions given in (3), the multi-sections broadband impedance transforming branch-line solution is adopted [25]. Thus, the characteristic impedance of the lines in the top and bottom horizontal path is Z_1 , while Z_2 , Z_3 and Z_4 are the characteristic impedances of the vertical lines, from left to right, respectively. The optimum values of such characteristic impedances can be derived by adopting a computer-aided optimization, based on the approach described in the following.

Due to the well-known matching limitations [28–30], the optimum loading condition in (3) cannot be achieved for a continuous range of frequencies. Thus, the optimization process is aimed to find the best values for Z_i (i = 1, 2, 3, 4) that allow to keep the loading conditions within a predefined constant power contour in the operating band [31, 32].

For this purpose, the following frequency dependent reflection coefficients are defined:

$$\Gamma_{Mb} = \frac{Z_{M,break} - 2 \cdot R_{opt}}{Z_{M,break} + 2 \cdot R_{opt}}$$

$$\Gamma_{Ms} = \frac{Z_{M,sat} - R_{opt}}{Z_{M,sat} + R_{opt}}$$
(5)

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$$\Gamma_{As} = \frac{Z_{A,sat} - R_{opt}}{Z_{A,sat} + R_{opt}}$$

 Z_M and Z_A being the impedances seen from port 1 and port 2 of the output combiner (Fig. 3). In particular, the loads at break point and saturation are obtained by simulating the output coupler with the following sources applied on port 1 and port 2:

- at break point port 1: $V_M = V_{DD} - V_k$ port 2: $I_A = 0$
- at saturation port 1: $V_M = V_{DD} - V_k$ port 2: $I_A = (V_{DD} - V_k)/R_{opt}$

Due to the different normalization impedances assumed for Γ_{Mb} , Γ_{Ms} and Γ_{As} in (5), for each of them the constant power contours are centred in the origin of the Smith chart. Then, in order to define a goal for the optimization, the simulated Γ_i (i = Mb, Ms, As) are rearranged by means of the following definition:

$$\Gamma_i^* = \sqrt{\Delta} \cdot \operatorname{Re}\left\{\Gamma_i\right\} + j \cdot \frac{\operatorname{Im}\left\{\Gamma_i\right\}}{\sqrt{\Delta}} \tag{6}$$

where

$$\Delta = \frac{|\Gamma_{\max}|}{|\Gamma_{\min}|} \tag{7}$$

 $|\Gamma_{\text{max}}|$ and $|\Gamma_{\text{min}}|$ being the greatest and lowest magnitudes, respectively, of the reflection coefficients belonging to the constant power contour, as highlighted in Fig. 4(a). As analytically demonstrated in the appendix, the value of Δ can be directly derived from the ripple (e.g., n dB) of the constant power contour:

$$\Delta = \frac{|\Gamma_{\max}|}{|\Gamma_{\min}|} = \sqrt{\frac{1+10^{-0.1 \cdot n}}{1-10^{-0.1 \cdot n}}}$$
(8)

The above relationship shows that the value of Δ depends only on the selected constant power contour (n), while it is independent from the actual value of R_{opt} .



Figure 4. (a) Conventional Γ -plane and 1 dB-ripple constant power contour. (b) Γ^* -plane and relative 1 dB-ripple constant power contour, obtained from (6).

Figure 5. $\lambda/4$ transmission line section and equivalent semi-lumped II-network.



Figure 6. (a) Network of Fig. 3 obtained by introducing the equivalent Π -network to integrate the output capacitance C_{ds} of the devices. (b) Realization with fully distributed elements.

The rearrangement of the reflection coefficient in (6) transforms the conventional Γ -plane of Fig. 4(a) to an oval shape, as shown in Fig. 4(b). In this rearranged Γ^* -plane, the constant power contours become practically circles as represented by $|\Gamma^*_{\max}| = |\Gamma^*_{\min}|$ in Fig. 4(b). Consequently, the goal to be fulfilled with the optimization becomes a simple constraint for the magnitude of Γ^*_i (see appendix):

$$|\Gamma_i^*| \le \left(\frac{1 - 10^{-0.1 \cdot n}}{1 + 10^{-0.1 \cdot n}}\right)^{3/4} \tag{9}$$

with i = Mb, Ms, As.

Once the optimum values of Z_1 , Z_2 , Z_3 and Z_4 are computed, a method to integrate the parasitic of the active device in the output combiner structure is also proposed. It is based on the substitution of the $\lambda/4$ transmission line with the equivalent Π -network reported in Fig. 5. The validity of this method has been, in fact, successfully demonstrated in both broadband [33] and multiband [34, 35] branch-line coupler designs.

By applying this approach, the branch-line coupler in Fig. 3 can be realized as shown in Fig. 6(a), where both quarter-wave transmission lines in front of the active devices are replaced with the equivalent II-network. In particular, the device drain-source parasitic capacitance (C_{ds}) is embedded in the scheme, using it as shunt capacitor on the left side of the II-network. An external capacitor $(C_T = C_{ds})$ is, instead, added on the right side of the line section. Finally, to avoid the use of lumped elements, the capacitor C_T can be replaced with an equivalent open circuited stub [33] as reported in Fig. 6(b). Even though the bandwidth of the coupler is reduced when the equivalent II-network is adopted, a broadband behavior is still achievable if the highest operating frequency is lower than the cut-off frequency of the semi-lumped transmission line [33].

2.2. Input Splitter

The scheme of the 2-sections branch-line coupler reported in Fig. 7 has been adopted to design the input power splitter.

The source is connected at the input port (P_1 in Fig. 7) in front of the Main amplifier (P_3 in Fig. 7), in order to obtain the desired 90° phase delay for the Auxiliary amplifier (P_4 in Fig. 7). A 50 Ω



Figure 7. 2-sections branch-line coupler to be used as input divider in DPAs.

resistance is connected at the isolated port $(P_2 \text{ in Fig. 7})$.

Since the input coupler has to provide the impedance transformation from the input loads of the amplifiers to the external source, the multi-sections broadband impedance transforming branch-line [25] is also adopted in this case. However, due to the different gate bias voltages, the input impedance of Main and Auxiliary amplifiers are quite different. Consequently, the horizontal symmetry plane of the coupler in Fig. 7 is removed with respect to the approach proposed in [25], considering different values for the top and bottom lines. In this way, a proper impedance transformation is also allowed when the output ports are terminated on different impedances.

The possibility to adopt such kind of 2-sections branch-line couplers as input splitter of DPAs has already been demonstrated in [13] with the implementation of a dual-band DPA. However, in that case, the splitting factor was optimized only at the two operating frequencies. Conversely, to achieve a broadband behavior of the DPA, the coupler has to show the same uneven splitting factor and quadrature phase balance for a continuous and wide frequency range.

The values of the characteristic impedances of the lines in Fig. 7 (Z_1 to Z_5) are obtained by means of a computer-aided optimization approach. In particular, the network in Fig. 7 is implemented in a CAD environment. Designed Main and Auxiliary amplifiers are used to terminate the output ports (P_3 and P_4) of the coupler, respectively. The ratio between the voltages at the gate of the amplifiers ($V_{g,A}/V_{g,M}$), i.e., the splitting factor, and the levels of $|S_{11}|$ and $|S_{41}|$ in the operating band are used as optimization goals.

3. PROTOTYPE DESIGN

In order to validate the proposed design approach, an hybrid prototype was implemented [36]. The targets for the designed DPA were a saturated output power $P_{sat} = 14$ W, with 6 dB of OBO and an operating band from 1.7 GHz to 2.4 GHz, thus achieving a relative bandwidth greater than 30%. For the design, a bare-die GaN HEMT (Cree-CGH60008D), whose nonlinear model is extracted at $V_{DD} = 28$ V, was adopted. This device shows a knee voltage and maximum current about 4 V and 1.3 A, respectively. For the DPA implementation, the optimum output resistance $R_{opt} = 45.6 \Omega$ is derived from (1)–(3).

Accounting for the value of R_{opt} , the computer-aided design approach described in Section 2.1 was performed to infer the characteristic impedances of the output combiner. The goal of the optimization was represented by the n = 1 dB constant power contour. The resulting values of the characteristic impedances are summarized in Table 1.

Subsequently, the drain-source parasitic capacitance of the active device $(C_{ds} \approx 0.8 \text{ pF})$ was estimated from the nonlinear model. This capacitance was integrated in the output combiner by means of the topology shown in Fig. 6(a). The characteristic impedance (Z_T) and equivalent electrical length (L_T) of the line between the two capacitors are reported in Table 1. Finally, the full distributed

Table 1. Design parameters of the output combiner.

Z_1	Z_2	Z_3	Z_4	Z_T	L_T	Z_W	L_W
55Ω	143Ω	124Ω	94Ω	78Ω	$46 \deg$	124Ω	$48 \deg$

topology in Fig. 6(b) was obtained by substituting each capacitor C_T with an open circuited stub having characteristic impedance (Z_W) and equivalent electrical length (L_W) , listed in Table 1. The results in terms of simulated output loads for Main and Auxiliary devices with the three implemented topologies are reported in Fig. 8.

As expected, the topologies in Figs. 6(a) and 6(b) shown a bandwidth reduction and an asymmetrical frequency behavior [33]. The loads exceed the 1 dB constant power contour when the transmission lines are replaced with their equivalent II-network. Nevertheless, such an effect can be reduced by performing a further CAD optimization step directly on the last combiner, i.e., the one in Fig. 6(b). The final design parameters are summarized in Table 2.

The output loads of Main and Auxiliary devices from the last optimization are shown in Fig. 8(d), resulting within the 1.2 dB constant power contour.

Similarly, in order to design the input splitter, the computer-aided design approach described in Section 2.2 was performed. More in details, the first step was to assure an unconditional stability of the devices both inside and outside the operating band. This was obtained by means of a capacitive/resistive network on the gate path (see Fig. 11). Then a pre-matching network (see Fig. 11) was inserted at the input of the stabilized devices to obtain a flat return loss in the operating band. The optimum splitting factor in terms of gate voltages was inferred performing nonlinear simulations of the biased devices combined at the output with the designed coupler, resulting in $|V_{g,A}|/|V_{g,M}| = 1.5$. Finally, the topology in Fig. 7 was used to join the two amplifiers at the input. Its characteristic impedances were optimized to achieve the desired splitting factor, in magnitude and phase, and levels of $|S_{11}|$ and



Figure 8. Simulated output loads of main and auxiliary devices obtained with (a) topology in Fig. 3, (b) topology in Fig. 6(a), (c) topology in Fig. 6(b), and (d) after the final optimization of the output combiner.

Table 2. Final design parameters of the output combiner.

Z_1	Z_2	Z_3	Z_4	Z_T	L_T	Z_W	L_W
55Ω	170Ω	130Ω	85Ω	70Ω	$56 \deg$	130Ω	$40 \deg$

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 $|S_{41}|$ as low as possible. The simulated performance of the input splitter is shown in Fig. 9, while the characteristic impedances used in the design are summarized in Table 3.

The complete scheme of the designed DPA is shown in Fig. 11. A $\lambda/4$ transmission line at 2 GHz with high characteristic impedance was shunted to the 50 Ω output termination to supply the drain bias voltage. Such high characteristic impedance was selected to reduce its reactive effect in the operating band. Finally, a set of shunting capacitors are added to each DC access point to avoid sensitivity of the DPA to the supplier.

The passive networks were realized on Duroid 5880 ($H = 381 \,\mu\text{m}, T = 17 \,\mu\text{m}, \epsilon_r = 2.2$). Planar electromagnetic simulations were performed to finalize the design. The bare-die devices were finally



Figure 9. Simulated performance of the input splitter.



Figure 10. Photograph of the realized prototype.



Figure 11. Schematic of the designed DPA.

Table 3. Design parameters for the input splitter.

Z_1	Z_2	Z_3	Z_4	Z_5
53Ω	38Ω	106Ω	62Ω	110Ω

connected to the input and output matching networks by using three bond wires (25 μ m of diameter, 900 μ m of length) on each side. Coaxial connectors are used at both input and output RF interfaces. A photo of the realized DPA is reported in Fig. 10.

4. EXPERIMENTAL RESULTS

The realized prototype was characterized under small signal condition at the nominal bias voltages: $V_{DD} = 28 \text{ V}, V_{GG,M} = -2.5 \text{ V}, V_{GG,A} = -5 \text{ V}$ and $I_D = 25 \text{ mA}$. The measured S-parameters are reported in Fig. 12 and compared with simulated ones showing a very good agreement.

The measured small signal gain ($|S_{21}|$ in Fig. 12) is greater than 10 dB from 1.67 GHz to 2.41 GHz, with a peak of 11.2 dB at 1.75 GHz. More than 36% of relative bandwidth is achieved accounting for a gain ripple of ± 0.6 dB. Moreover, the intrinsic filtering capabilities of the adopted 2-sections branch-line couplers result in a high rejection levels outside the operative band. The measured input and output return losses are better than 8 dB and 10 dB, respectively.

The experimental measurements with a single carrier signal are summarized in Fig. 13 and Fig. 14. In particular, gain and drain efficiency versus output power for several frequencies inside the operating band (1.7 GHz, 1.9 GHz, 2.2 GHz and 2.4 GHz) are reported in Fig. 13. An efficiency higher



Figure 12. Measured and simulated S-parameters of the realized DPA.



Figure 13. Measured single carrier performance versus output power at 1.7 GHz, 1.9 GHz, 2.2 GHz and 2.4 GHz.



Figure 14. Measured single carrier performance versus frequency at 27 dBm and 33 dBm input power levels.

than 40% in a 6 dB of OBO (i.e., from 34 dBm up to 40 dBm of output power for all reported frequencies) can be noted.

The measured output power and drain efficiency versus frequency are depicted in Fig. 14 for an input power level of 27 dBm and 33 dBm, corresponding to the break and saturation conditions, respectively.

For both input power levels, the output power is within $\pm 0.75 \,\mathrm{dB}$ ripple from 1.7 GHz to 2.4 GHz, demonstrating an almost linear increase of output power with input power in the entire operating band. Moreover, high levels of both backed-off efficiency (> 41% @ 27 dBm input power) and saturation efficiency (> 50% @ 33 dBm input power) are obtained, with a peak of 58% at the break point at 2.4 GHz and 72% at the saturation at 2.35 GHz.

Finally, the prototype was also characterized with signals having complex modulation schemes. In particular, 5 MHz-3gpp and 5 MHz-WiMAX were used as testing signals, whose peak-to-average power ratios (PAPR) are about 5.4 dB and 9.3 dB, respectively. To evaluate the capability of the prototype to efficiently operate in a wide frequency range, these two modulation schemes were applied in the entire operating band.

The measured performance in terms of average efficiency and adjacent channel power ratio (ACPR),



Figure 15. Measured performance applying (a) 5 MHz-3gpp and (b) 5 MHz-WiMAX modulation schemes at 1.8 GHz, 2 GHz and 2.3 GHz and sweeping the average power level. (c) Measured performance when 37 dBm, in 5 MHz-3gpp operating mode, and 34 dBm, in 5 MHz-WiMAX operating mode, of average output power are reached with center carrier frequency swept from 1.7 GHz to 2.4 GHz at step of 0.1 GHz. (d) Measured output spectrums when 37 dBm, in 5 MHz-3gpp operating mode, and 34 dBm, in 5 MHz-WiMAX operating mode, and 34 dBm, in 5 MHz-WiMAX operating mode, and 34 dBm, in 5 MHz-WiMAX operating mode, of average output power are reached at 2 GHz as center carrier frequency.

without predistortion, are resumed in Fig. 15. In particular, the results as a function of the average output power and for different center carrier frequencies are reported in Fig. 15(a) and Fig. 15(b) for the 3gpp and the WiMAX, respectively. The frequency responses, from 1.7 GHz to 2.4 GHz at step of 0.1 GHz, are shown in Fig. 15(c). These results refer to the condition when 37 dBm and 34 dBm of average output power are reached with 3gpp and WiMAX, respectively. For the same power levels, Fig. 15(d) reports the measured output spectrums at 2 GHz as center carrier frequency. As expected, due to higher PAPR of the WiMAX signal, a degradation of the performance is obtained with respect to the 3gpp case. However, in both operating modes, the amplifier demonstrates the capability to operate with almost similar performance at every center carrier frequency. Finally, the possibility to drastically reduce the ACPR level of the amplifier by using a polynomial digital predistorter has been verified with a 20 MHz LTE signal [36].

5. CONCLUSION

In this contribution, a novel design approach to realize broadband DPAs is presented. The methodology exploits the wideband features of the 2-sections brach-line couplers to implement both the input and output DPA networks. The developed computer-aided approach to synthesize these structures has been discussed in details and applied to design an hybrid prototype. The realized GaN-based DPA shows more than 36% of fractional bandwidth around 2 GHz frequency range, validated through both single-carrier and multi-carrier signals (3gpp and WiMax). In single carrier mode an efficiency higher than 41% (> 50% in saturation, with a peak of 72%) was obtained at 6 dB of output power dynamic range in the entire operating band. Results with 5-MHz 3gpp and WiMax signals showed an average efficiency of 50% and 45% when 37 dBm and 34 dBm of average output power are reached, respectively.

APPENDIX A.

In order to derive the relation (8), the following equation for Γ_{\min} can be written:

$$\Gamma_{\min} = \frac{R_{Low} - R_{opt}}{R_{Low} + R_{opt}} \tag{A1}$$

being (see Equation (4.18) of [32])

$$R_{Low} = R_{opt} \cdot 10^{-0.1 \cdot n}. \tag{A2}$$

Then, replacing (A2) in (A1), it follows:

$$|\Gamma_{\min}| = \frac{1 - 10^{-0.1 \cdot n}}{1 + 10^{-0.1 \cdot n}} \tag{A3}$$

Similarly, for Γ_{\max} it is possible to write:

$$\Gamma_{\max} = \frac{R_{Low} + j \cdot X_{Low} - R_{opt}}{R_{Low} + j \cdot X_{Low} + R_{opt}}$$
(A4)

where (see Equation (4.20) of [32])

$$X_{Low} = \sqrt{R_{opt}^2 - R_{Low}^2} \tag{A5}$$

Thus, replacing (A2) and (A5) in (A4), it follows:

$$|\Gamma_{\max}| = \sqrt{\frac{1+10^{-0.1 \cdot n}}{1-10^{-0.1 \cdot n}}}$$
(A6)

Finally, applying the definition given in (7), it follows:

$$\Delta = \frac{|\Gamma_{\text{max}}|}{|\Gamma_{\text{min}}|} = \sqrt{\frac{1+10^{-0.1 \cdot n}}{1-10^{-0.1 \cdot n}}}$$
(A7)

thus demonstrating Equation (8).

After the reflection coefficients rearrangement by using (6), the constant power contour becomes similar to a circle, whose radius is

$$r = \sqrt{\Delta} \cdot |\Gamma_{\min}| = \frac{1}{\sqrt{\Delta}} \cdot |\Gamma_{\max}|$$
(A8)

As a consequence, the condition to assure $n \, dB$ output power ripple is

$$|\Gamma_i^*| \le \sqrt{\Delta} \cdot |\Gamma_{\min}| \tag{A9}$$

Then replacing (A3) and (A7) it follows (9).

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