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Design of a Compact and Broadband Class-F^{-1} Power Amplifier

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Abstract—In this paper, a broadband class-F^{-1} power amplifier (PA) that can be integrated into compact-sized micro-radio units is introduced. This PA utilizes a multi-harmonic impedance merging technique at harmonic frequencies so that the circuit areas of matching networks can be minimized. As well, in order to maximize the bandwidth of high efficiency, circuit configuration was optimized by the first order differentiation of the fundamental-frequency impedance. For the sake of verification, a 10 W inverse class-F PA operating at 1.9 GHz was designed with a commercial GaN transistor. It exhibited at least 39.2% size reduction as compared to conventional PAs of the similar power. In addition, it exhibited a bandwidth of 600 MHz (1.6 $\sim$ 2.2 GHz) at an efficiency greater than 60%, a peak efficiency of 83.9%, and an output power of 42.2 dBm.

1. INTRODUCTION

The wireless communications field has recently witnessed a proliferation of mobile devices. Driven by the rapid increase in the number of devices with advanced media features, such as smartphones, the demand for flexible and high-capacity base station equipment is gradually increasing. In an effort to address this issue, a compact reconfigurable radio unit was proposed [1]. Because of its compact size, the proposed radio unit can be placed right below the transmit antennas, greatly reducing the power loss from the transmission line between the radio unit, and thus, increasing the system efficiency.

However, on the PA side, the efficiency is degraded in general by non-idealities such as on-resistance and output parasitic components of transistors. In addition, the requirements on multi-harmonic impedances for high efficiency limit the bandwidth of optimal operation owing to the constraints on the components [2]. For these reasons, previous studies are either focused on frequencies lower than UHF band [3–5], or bulky for the sake of high efficiency [6, 7], or for low-power operation [8, 9].

Consequently, in order to design broadband, highly efficient PAs that fit into the aforementioned micro-radio unit, many practical aspects have to be considered for the optimum but balanced operation between size, linearity, bandwidth, and efficiency. Therefore, this paper suggests a design method for minimizing the circuit footprints of PAs by combining the harmonic impedances in matching networks. The circuit was optimized for the widest bandwidth when operated in the inverse class-F condition. In Section 2, the harmonic impedance merging technique is introduced to design matching networks, along with a mathematical approach that was previously introduced by the authors [10]. Afterwards, the impedances of the input and output matching networks are designed for broadband inverse class-F operation. In Section 3, the performance of the inverse class-F PA is verified by simulation with a GaN HEMT transistor. The measurement results and a discussion follow.

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2. COMBINING MULTI-HARMONIC TRANSMISSION LINES FOR COMPACT MATCHING NETWORKS

Designing a high-efficiency PA necessarily includes the definition of harmonic impedances at the matching networks, and the output matching network decides most of its characteristics. For this reason, major design conditions on the output matching network are set for the best performance, whereas on the input side mainly the circuit area minimization is performed.

A general circuit for input matching networks of wireless amplifiers is shown in Fig. 1, where the DC and AC (particularly the fundamental and the second harmonic) paths are terminated with suitable impedances. Commonly, l_2 is close to zero, and l_3 is one-quarter wavelength at the fundamental frequency so that its impedance is seen as open from the right-hand-side port. In order to reduce the occupied area of the circuit, a systematic method to combine the harmonic impedance requirements while maintaining its performance was suggested by the author [10]. Looking from the right-hand-side port that is connected to the gate of a transistor, the impedance, Z_g, from the reflection equations throughout the transmission line l_2 is found as follows [11]:

$$Z_g = Z_{o2}\frac{Z_R + jZ_{o2}\tan(\beta l_2)}{Z_{o2} + jZ_R\tan(\beta l_2)}, \tag{1}$$

where β is the propagation constant, Z_{o2} the characteristic impedance of l_2 transmission line, and Z_R the shunt connected impedance of Z_1 and Z_3.

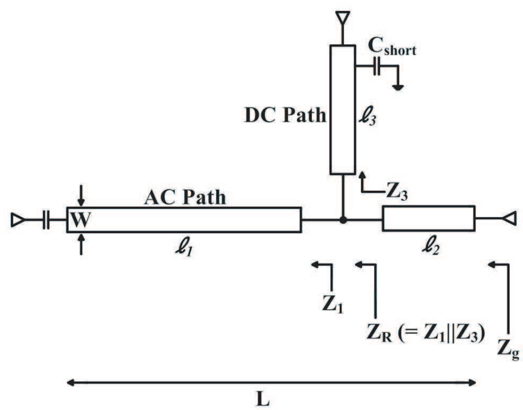

Figure 1. Input matching network for the optimal harmonic impedance combination.

For the design of an input matching network of a PA, the following three conditions on Z_g should be met:

- *Condition A*: $Z_g = 0$ at DC

$$Z_g = Z_{o2}\frac{Z_R + jZ_{o2}\cdot 0}{Z_{o2} + jZ_R\cdot 0} = Z_1||Z_3 = Z_3. \tag{2}$$

- *Condition B*: $Z_g = 0$ at $2f_0$

  Assuming the general case when Z_1 is greater than Z_3 at the second frequency, Equation (1) is used to obtain Z_g at $2f_o$.

$$Z_g = Z_{o2}\frac{Z_1||Z_3 + jZ_{o2}\alpha_2}{Z_{o2} + j(Z_1||Z_3)\alpha_2} \tag{3}$$

$$\approx Z_{o2}\frac{j(Z_{o2}\alpha_2 + Z_{o3}\alpha_3)}{Z_{o2} - Z_3\alpha_2\alpha_3} = Z_{o2}\frac{j(\alpha_2 + \alpha_3')}{1 - \alpha_2\alpha_3'}$$

$$\approx jZ_{o2}\tan\beta(l_2 + l_3'), \tag{4}$$

  where α_2 and α_3 respectively represent $\tan(\beta l_2)$ and $\tan(\beta l_3)$, and Z_{o2} and Z_{o3} are respectively the characteristic impedances of l_2 and l_3 transmission lines. Also, l_3' is the effective length of $l_3(= \alpha_3 Z_{o3}/Z_{o2})$, and α_{o3}' is defined as $\tan(\beta l_3')$.

- *Condition C*: $Z_g = R_g + \mathrm{j}X_g$ at f_0
  When Equation (1) is expanded at f_o for the required Z_g, the Z_1 can be found as follows:

$$Z_1 = \frac{-Z_{o2}Z_{o3}\alpha_3(Z_{o2}\alpha_2 + jZ_g)}{Z_g(Z_{o2} - Z_{o3}\alpha_2\alpha_3) - jZ_{o2}(Z_{o2}\alpha_2 + Z_{o3}\alpha_3)}. \tag{5}$$

  It is clear that as long as α_3 is not zero (a value of zero corresponds to the l_3 transmission line of zero length), Z_1 can be found to obtain the desired value of Z_g.

In conjunction with these three constraints on the impedance at each frequency, a figure of merit (FOM) is defined to evaluate the effectiveness of the size reduction, which also reflects the forward transmission ratio of the signal [10]. With this measure, the lengths of the transmission lines in matching circuits can be analyzed systematically for the sake of circuit area:

$$\begin{aligned} FOM_{IMN} &= Signal\ Transmission\ Rate \cdot Circuit\ Area\ Reduction \\ &= \frac{Impedance\ Ratio}{Circuit\ Area} \cong \frac{|\ Z_3/Z_1\ |}{L \times (\lambda_1/4 - l_2 + W)}. \end{aligned} \tag{6}$$

3. DESIGN CONSIDERATIONS FOR THE OUTPUT MATCHING NETWORK

For the output matching network, three important design constraints are equally important:

- The impedance should lie within an acceptable efficiency region on the Smith chart over the specified frequency range.
- The locus of the harmonic impedances should stay as much inside the lowest Q-line as possible over the frequency range for wideband operation.
- The lengths of the transmission lines should be minimized for the sake of the minimal circuit area.

Among many highly efficient PA architectures, and with the above conditions considered, the inverse class-F architecture was adopted for the PA design because of its harmonic impedance characteristic: the second harmonic impedance infinite and the third harmonic impedance open. Considering that the fundamental output impedance of high-power amplifiers is as low as a few ohms [4], the first three harmonic impedances of the inverse class-F condition are 180° apart in a row. This can lead to a smaller circuit area over the conventional class-F operation, which requires the reflection coefficients for the fundamental and the second harmonic frequencies to be 360° (a full wavelength) apart. Therefore, the first two harmonic impedances are very closely located on the Smith chart. Fig. 2 shows designed output matching networks as per the class-F and the inverse class-F requirements. For the class-F matching, as shown in Fig. 2(a), the length of a transmission line to have the first two harmonic frequencies near zero ohm is at least a half wavelength of the fundamental frequency.

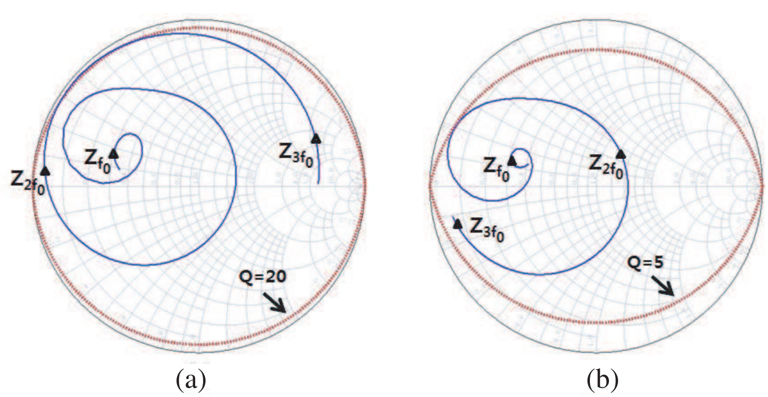

Figure 2. Output impedance (blue, solid line) and Q line (red, dotted line) of (a) class-F condition and (b) inverse class-F condition.

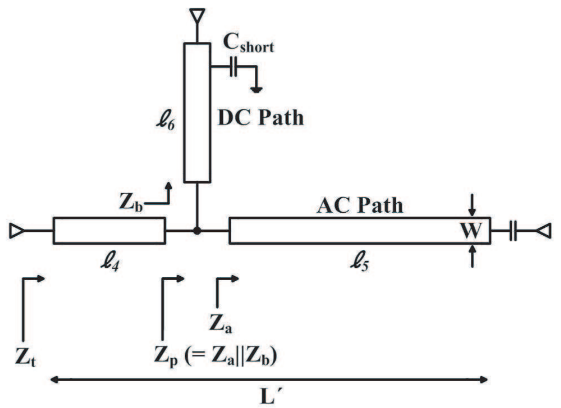

Figure 3. Output matching network for the optimal FOM and bandwidth analysis.

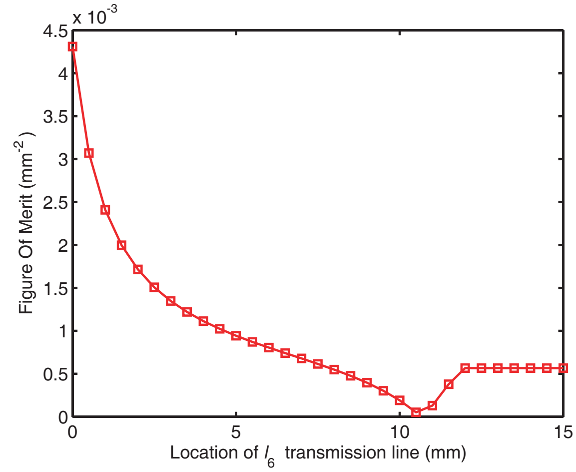

Figure 4. Figure of merit (FOM) over the location of the shunt transmission line, l_6, in the output matching network.

However, when the second harmonic impedance is required to be infinite, as in the inverse class-F operation (Fig. 2(b)), the minimum separation for the harmonic impedances can be a quarter wavelength of the fundamental frequency. Consequently, from the standpoint of the occupied circuit areas, this makes it much easier to implement compact-sized class-F^{-1} PAs than class-F PAs. Although there might be some methods of overcoming this issue, such as by placing additional resonance in the circuit, the inherent difference in the circuit areas still remains, resulting in narrower bandwidth. Fig. 2 also compares the maximum quality-factor lines of these two cases, in which class-F shows a higher quality factor than class-F^{-1}. This implies that class-F^{-1} inherently has wider bandwidth than class-F does. Therefore, for these aforementioned reasons, class-F^{-1} architecture is adopted for the compact, wide-bandwidth power amplifier design.

In the next step, the output matching of the class-F^{-1}, as shown in Fig. 3, is analyzed for the best FOM metric in a similar manner as was done for the input matching network. Then, analysis of the frequency sensitivity is conducted to extract the best condition for a wide bandwidth.

Based on (6) and (7), the FOM metric for the output matching network is calculated to find the best location minimizing the occupied area of the circuit without sacrificing its performance:

$$Area_{Output\ Matching} = (l_4 + l_5) \times (l_6 + W) \approx L' \times (\lambda_1/4 - l_4 + W), \tag{7}$$

$$FOM_{OMN} = \frac{Impedance\ Ratio}{Circuit\ Area} \cong \frac{|\, Z_b/Z_a \,|}{(l_4 + l_5) \times (l_6 + W)} \cong \frac{|\, Z_b/Z_a \,|}{L' \times (\lambda_1/4 - l_4 + W)}. \tag{8}$$

As a result of the FOM analysis of the output matching network, Fig. 4 suggests that the best location of the l_6 transmission line is right next to the drain of the transistor (l_6 location $= l_4 = 0$ mm).

Along with the FOM result, bandwidth optimization is performed by the first-order differentiation on the fundamental load resistance $R_{L,f_o} (= \mathrm{Real}(Z_t))$ with respect to the frequency so that the load impedance has minimal sensitivity to the frequency.

$$\frac{\partial R_{L.f_0}}{\partial f} = \frac{\partial}{\partial f}\left[\mathrm{Real}\left(Z_{o4}\frac{Z_a||Z_b + jZ_{o4}\tan(\beta l_4)}{Z_{o4} + jZ_P\tan(\beta l_4)}\right)\right] = \frac{\partial}{\partial f}\left[\mathrm{Real}\left(Z_{o4}\frac{Z_a||Z_b + jZ_{o4}\tan\left(2\pi\frac{f}{c\sqrt{\epsilon_r}}l_4\right)}{Z_{o4} + jZ_P\tan\left(2\pi\frac{f}{c\sqrt{\epsilon_r}}l_4\right)}\right)\right] = 0. \tag{9}$$

This equation is solved for the location of the shunt transmission line l_6 (which is represented by the length of l_4), and its solution defines the optimum location of l_6 for the sake of bandwidth. As a result, in Fig. 5, the best location of the l_6 stub from the bandwidth perspective is found to be $2 \sim 3$ (mm) off from the drain port. Therefore, although the FOM in Fig. 4 suggests that the minimal size of the

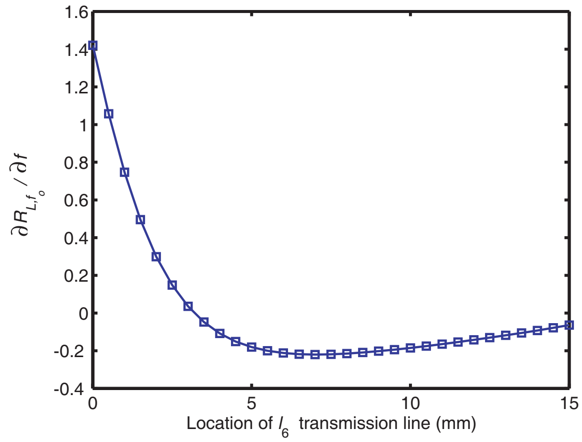

Figure 5. Analysis for the widest bandwidth on the location of the l_6 stub.

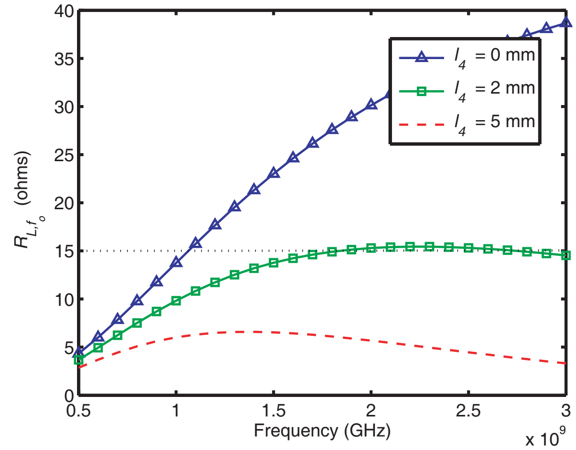

Figure 6. Simulated R_L with $l_4 = 2$ (mm) shows a wide bandwidth for the target resistance of 15 ohm.

circuit is achieved with $l_4 = 0$ (mm), the implementation of the class-F^{-1} power amplifier was done with $l_4 = 2$ (mm) for the sake of broader bandwidth. However, the circuit still occupies far less area compared to conventional designs. Fig. 6 compares calculated load resistances over frequency with different l_4 values, in which the R_{L,f_o} with $l_4 = 2$ (mm) shows the widest bandwidth around the target impedance of 15 ohm.

4. DESIGN AND MEASUREMENT OF INVERSE CLASS-F POWER AMPLIFIER

On the basis of the analysis introduced in the previous sections, a compact and broadband inverse class-F PA was implemented. This PA is designed with a 10-watt commercial GaN transistor (CGH40010F from CREE Inc.) populated on an RF-35 substrate board, and it had the bias condition of 28 V and 200 mA at the drain. With the given transistor, source-pull and load-pull simulations were performed for the best operation, from which the circuit was designed to have an efficiency higher than 50% (dotted lines in Fig. 7) over the frequency range from 1.6 GHz to 2.2 GHz. The simulated result of the matching is shown in Fig. 7.

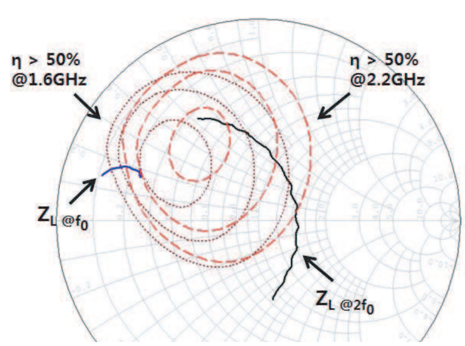

Figure 7. Results of the simulated load-pull test and the output matching network.

Based on the source-pull and load-pull simulations followed by electromagnetic (EM) simulations, the input impedance was chosen as $4 + j0\,\Omega$ at a fundamental frequency of 1.9 GHz. In addition, the output impedance was selected as $15 + j10\,\Omega$ at 1.9 GHz, whereas it was designed to be $18 + j9\,\Omega$ and $15 + j13\,\Omega$ at the boundary frequencies of 1.6 GHz and 2.2 GHz, respectively. The final FOM was 0.0017 with l_6 located at 2 mm off from the drain.

With regard to the harmonic impedances for the inverse class-F operation, the second harmonic impedance was designed to be $91 + j3\,\Omega$. On the other hand, the third harmonic impedance was assigned a value as close as zero ohms, which was $3 + j1\,\Omega$.

Consequently, the measured output impedances at the harmonic frequencies were $12 + j8.7\,\Omega$ at f_0 ($= 1.9\,\text{GHz}$), $64.5 + j23.7\,\Omega$ at $2f_0$, and $1.6 - j14.8\,\Omega$ at $3f_0$. The fundamental impedance varied from $5.6 + j7\,\Omega$ at 1.6 GHz to $11.5 + j10\,\Omega$ at 2.2 GHz.

Figures 8 and 9 show the measured performance of the PA, which include the following: an output power of 42.2 dBm, a peak efficiency of 83.9%, and a frequency range of 600 MHz for 60% and higher efficiency. In addition, a circuit size reduction of 39.2% was achieved as compared to the size of conventional PA circuit [3]. Table 1 compares performance metrics of the suggested design with the ones of previous studies. Fig. 10 shows the picture of the realized PA circuit.

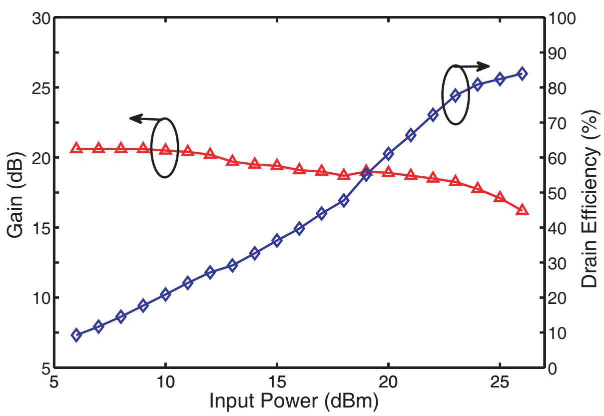

Figure 8. Drain efficiency and gain versus input power at 1.9 GHz.

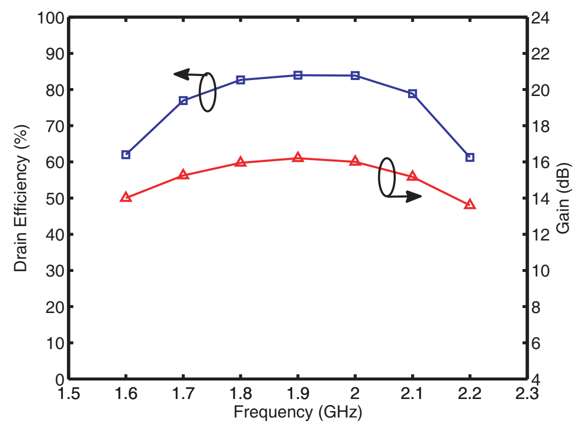

Figure 9. Drain efficiency and gain versus frequency with the input power of 26 dBm.

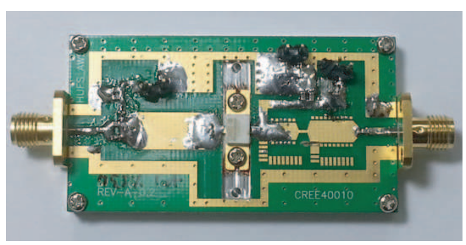

Figure 10. Final circuit of the inverse class-F power amplifier.

Table 1. Comparison between the suggested design and previous studies.

	Total Circuit Area (mm^2)	Output Power (dBm)	Gain (dB)	Operational Frequency (MHz) for $\eta > 60\%$
Suggested PA	61.6×27.8	42.2	16.2	1600–2200
[3]	140×70	43	17	50–550
[6]	120×100	47.5	10.6	875–925
[8]	100×100	19.6	10	2400–2410

5. CONCLUSION

In order to meet the stringent requirements for the next-generation micro-sized radio units, methods for designing compact, efficient, and broadband PAs are necessary. In this respect, this paper suggests a systematic design method to minimize the circuit area while maintaining wide frequency range and high efficiency. This is achieved by merging the multi-harmonic impedances at the matching networks and by operating the transistor in an inverse class-F condition, which is found to be a better option for high efficiency over a wide range of frequencies. In addition, the circuit configuration to achieve the widest bandwidth is calculated from the first-order differentiation of the output impedance. For the sake of the verification of the suggested method, a 10-watt PA at 1.9 GHz center frequency was implemented. This inverse class-F PA occupies at least 39.2% less area than the conventional PA of the similar power, whereas it showed a peak output power of 42.2 dBm, a maximum efficiency of 83.9%, an operation frequency range from 1.6 GHz to 2.2 GHz with an efficiency greater than 60%. Consequently, the PA with the suggested design method fits into the size of next-generation micro-radio units as well as shows the highest efficiency of its power class and reasonable bandwidth of 600 MHz.

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