Progress In Electromagnetics Research C, Vol. 44, 225–238, 2013

LOW THIRD-ORDER INTERMODULATION DISTORTION IN $Ba_{0.6}Sr_{0.4}TiO_3$ THIN FILM INTERDIGITAL CAPACITORS

Muhammad F. Abdul Khalid[1, 2, *], Ernest A. Fardin[3], James R. Scott[1], Anthony S. Holland[1], and Kamran Ghorbani[1]

[1]School of Electrical and Computer Engineering, RMIT University, Melbourne, VIC 3001, Australia

[2]Faculty of Electrical Engineering, Universiti Teknologi MARA, Shah Alam, Selangor 40450, Malaysia

[3]Radio Frequency Systems, Kilsyth, Victoria 3137, Australia

Abstract—A new method for the theoretical analysis of the third-order intermodulation distortion (IM_3) in barium strontium titanate (BST) thin film interdigital capacitors (IDCs) on r-plane sapphire substrates is presented. Two circuit topologies — the dual and series dual BST varactor circuit — are proposed and their theoretical models along with simulated and measured results are presented. Low IM_3 is demonstrated and experimentally verified. By proper selective biasing, very low nulls are observed in both dual and series dual BST varactor circuit topologies which indicate minimum distortion. The measured first nulls are achieved at ± 13 V and ± 20 V for the dual and series dual topologies respectively. These results demonstrate the potential of incorporating these highly linear BST varactors in silicon on sapphire (SoS) applications.

1. INTRODUCTION

Barium Strontium Titanate (BST) varactors have found many applications in frequency agile microwave devices mainly due to their performance in the frequency region above 10 to 20 GHz. In this frequency region, which is known as the "varactor gap" region, BST varactors have significantly higher tuning speed, Q-factor and power handling compared to well-established silicon varactor

Received 2 September 2013, Accepted 11 October 2013, Scheduled 15 October 2013

* Corresponding author: Muhammad Farid Abdul Khalid (m.abdulkhalid@student.rmit.edu.au).

technology [1, 2]. Also, the high dielectric permittivity contributes to the size reduction of the microwave components and compact, small-scaled microwave devices can be realised.

Integration of BST with the existing semiconductor technologies has long been of interest and silicon-on-sapphire (SoS) technology presents one of the possible solutions due to its many advantages. One of the main advantages over traditional bulk silicon integrated circuits is the high isolation between devices. This offers lower power dissipation, higher operating speed and minimum parasitic semiconductor junctions due to the highly insulating sapphire substrate. This technology uses a very thin layer of silicon deposited on an r-plane sapphire substrate, which provides a suitable orientation for the growth of silicon [3]. By depositing the BST film early in the SoS process, the high deposition temperature can be tolerated without affecting the silicon epilayer [4]. Some frequency agile microwave devices that have the potential to be incorporated in this technology had been developed with epitaxial BST thin films on r-plane sapphire substrates at 10 GHz and above such as interdigital capacitors (IDCs) [4], bandpass filters [5] and phase shifters [6].

Intermodulation distortion in nonlinear semiconductor and BST varactors is also another issue that has gained interest over the past few years. Meyer et al. had previously analysed the intermodulation distortion in varactor diodes using the Volterra series approach in which closed-form expressions for intermodulation distortion in parallel- and series-tuned circuits were successfully derived. Antiparallel and back-to-back circuit topologies were introduced and experimentally verified for achieving minimum distortions [7]. Since then, several research groups have demonstrated the effectiveness of implementing this idea in BST, MEMS and varactor diode technologies to enhance linearity of the devices [8–11]. A linearity improvement technique based on BST-stacked parallel-plate capacitors has been analysed by connecting several capacitors in series, which reduced the RF swing across each capacitor [8, 12]. RF MEMs varactors in antibiased topology showed enhanced linearity and reduced bias noise [9]. Anti-series and anti-series/anti-parallel varactor diode topologies were presented in [10], in which the doping profile and area ratio parameters influenced the design to achieve minimum distortion.

We recently investigated the third-order intermodulation distortion (IM_3) in BST thin film IDCs and proposed the dual BST varactor circuit topology [13]. In this paper, we have not only experimentally verified the previous technique, but also introduced a new topology to reduce the IM_3 further. Two circuit topologies, the "dual" and "series dual" BST varactor circuit are proposed to validate the theo-

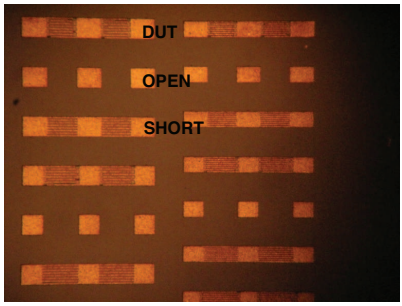

Figure 1. An array of the fabricated BST interdigital capacitors with adjacent open and short circuit calibration standards on a 10 mm × 10 mm diced r-plane sapphire substrate.

retical analysis in comparison with the circuit simulation results. Low IM_3 is experimentally demonstrated in both topologies and, by proper selective biasing, a significant reduction in IM_3 is achieved.

2. BST INTERDIGITAL CAPACITOR FABRICATION

In this work, IDCs were fabricated on 50 nm thick $Ba_{0.6}Sr_{0.4}TiO_3$ thin films grown on 10 mm × 10 mm diced r-plane sapphire substrates. The BST thin films were initially deposited on the 500 µm thick sapphire substrates by pulsed laser deposition (PLD). The details of the BST thin film deposition and material characterisation can be found in [4, 14]. The fabrication of IDCs was realized in a multistep process. First, a seed layer composition of Ti/Ni/Au was deposited using e-beam evaporation. Next, the IDCs with adjacent open and short-circuit calibration standard patterns were achieved by lift-off. A 2.5 µm Au layer was then electroplated within the defined plated seed layer region. Finally, the non-plated seed layer region was removed by chemical wet etching. The purpose of the open and short-circuit calibration standards patterned adjacent to the IDCs was to de-embed the parasitic elements related to the interdigital electrodes from the measured data to accurately determine the final capacitance and Q-factor values of the varactors [15, 16]. An array of IDCs with different sets of geometry in terms of the finger gap, finger length, finger width and number of fingers was realised. The finger gap ranged from 2 µm to 8 µm and finger length from 90 µm to 130 µm. The finger width and number of fingers were fixed at 5 µm and 8 respectively. The IDCs were designed with two sets of electrodes to enable ground-signal-ground (GSG) configuration. The IDCs are shown in Figure 1.

The BST varactors were selected based on the measured performances in which they had reasonably good tunability of $\sim 43\%$ and Q-factor values in the range of $\sim$ 13.4 to 78.3 from 0 to 40 V at 10 GHz. Note that the highest tunability of 64% was recorded with the 200 nm BST films but compensated by the lowest Q-factor in the range of $\sim$ 7.8 to 32.2 [4]. The reduction in the tunability of the measured 50 nm BST film was caused by the tensile strain. However, the permittivity remained quite high, $\sim$ 800 at 0 V. The capacitance and Q-factor values were computed using an RC equivalent circuit model, taking into account all the parasitic elements associated with the pad metallization [14, 16].

3. THEORETICAL ANALYSES AND SIMULATIONS

3.1. Theoretical Analysis of Dual BST Varactor Circuit Topology

In order to analyse the nonlinear behaviour of the BST varactor, a polynomial expression is initially defined as shown in (1), which perfectly fits the measured capacitance values,

$$C(V) = K_0 + K_2(V_{dc}+v)^2 + K_4(V_{dc}+v)^4 + \ldots + K_{16}(V_{dc}+v)^{16} \quad (1)$$

where K_o, $K_2 \ldots K_{16}$ are the coefficients of the polynomial, and V is the sum of bias voltage, V_{dc} and RF voltage, v. This 16th degree polynomial equation also compares favorably to the nonlinear BST model in [17], where the fringing capacitance, C_f is taken into account. The comparison between the polynomial equation in (1) and the measured capacitance values is shown in Figure 2.

The general nonlinear capacitance of a varactor can be expanded by a power series as a function of the incremental voltage v and is

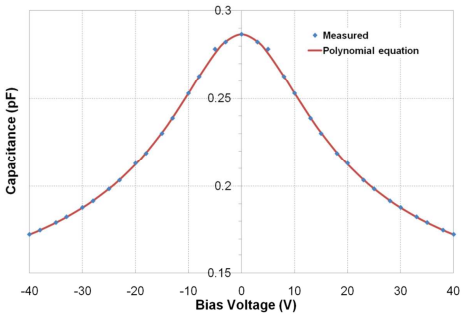

Figure 2. Polynomial expression in comparison with the measured data of the interdigital BST capacitor.

expressed as

$$C(v) = C_0 + C_1 v + C_2 v^2 + \dots \tag{2}$$

The polynomial expression in (1) is then converted into the form of (2) and the value of each coefficient (C_0, C_1 and C_2) is extracted with respect to its incremental voltage, v as tabulated in Table 1. These coefficients are subsequently substituted into the well-established closed-form IM_3 expression of a varactor diode [7], where it is found that this expression is also ideal for the analysis of a BST varactor.

Table 1. Coefficients of ideal dual BST varactor circuit topology.

C_{0left}	$[K_0 + K_2(V_{dc})^2 + K_4(V_{dc})^4 + K_6(V_{dc})^6 + K_8(V_{dc})^8$ $+K_{10}(V_{dc})^{10} + K_{12}(V_{dc})^{12} + K_{14}(V_{dc})^{14} + K_{16}(V_{dc})^{16}]/2$
C_{0right}	$[K_0 + K_2(-V_{dc})^2 + K_4(-V_{dc})^4 + K_6(-V_{dc})^6 + K_8(-V_{dc})^8$ $+K_{10}(-V_{dc})^{10} + K_{12}(-V_{dc})^{12} + K_{14}(-V_{dc})^{14} + K_{16}(-V_{dc})^{16}]/2$
C_{1left}	$[2K_2(V_{dc}) + 4K_4(V_{dc})^3 + 6K_6(V_{dc})^5 + 8K_8(V_{dc})^7 + 10K_{10}(V_{dc})^9$ $+12K_{12}(V_{dc})^{11} + 14K_{14}(V_{dc})^{13} + 16K_{16}(V_{dc})^{15}]/2$
C_{1right}	$[2K_2(-V_{dc}) + 4K_4(-V_{dc})^3 + 6K_6(-V_{dc})^5 + 8K_8(-V_{dc})^7 + 10K_{10}(-V_{dc})^9$ $+12K_{12}(-V_{dc})^{11} + 14K_{14}(-V_{dc})^{13} + 16K_{16}(-V_{dc})^{15}]/2$
C_{2left}	$[K_2 + 6K_4(V_{dc})^2 + 15K_6(V_{dc})^4 + 28K_8(V_{dc})^6 + 45K_{10}(V_{dc})^8$ $+66K_{12}(V_{dc})^{10} + 91K_{14}(V_{dc})^{12} + 120K_{16}(V_{dc})^{14}]/2$
C_{2right}	$[K_2 + 6K_4(-V_{dc})^2 + 15K_6(-V_{dc})^4 + 28K_8(-V_{dc})^6 + 45K_{10}(-V_{dc})^8$ $+66K_{12}(-V_{dc})^{10} + 91K_{14}(-V_{dc})^{12} + 120K_{16}(-V_{dc})^{14}]/2$

IM_3 is defined as the ratio of the magnitude of the third-order distortion component to the fundamental signal. Recently, this IM_3 expression has been slightly modified from [7] to perfectly fit the simulated data and is given by

$$\mathrm{IM}_3 = \frac{3}{8} V_o^2 \frac{|A_3(j\omega_1, j\omega_1, -j\omega_2)|}{|A_1(j\omega_1)|^2 \, |A_1(j\omega_2)|} \tag{3}$$

where V_o is the peak of each fundamental output voltage and the third- and first-order Volterra coefficients are derived as

$$A_3(j\omega_1, j\omega_1, -j\omega_2) = -\frac{(2j\omega_1 - j\omega_2)\left[C_1 \hat{A} + \frac{C_2}{3} A_1(j\omega_1)^2 A_1(-j\omega_2)\right]}{\frac{1}{R} + (2j\omega_1 - j\omega_2)\, C_0} \tag{4}$$

$$A_1(j\omega) = \frac{1}{\frac{1}{R} + j\omega C_0} \tag{5}$$

where

$$\hat{A} = \frac{1}{3}\left[2A_1(j\omega_1)A_2(j\omega_1, -j\omega_2) + A_1(-j\omega_2)A_2(j\omega_1, j\omega_1)\right] \tag{6}$$

and the second-order Volterra coefficient is derived as

$$A_2(j\omega_a, j\omega_b) = -\frac{\frac{C_1}{2}(j\omega_a + j\omega_b)A_1(j\omega_a)A_1(j\omega_b)}{\frac{1}{R} + (j\omega_a + j\omega_b)C_0} \tag{7}$$

The simplifications in the above equations are the slight modification in (3) for redefining the IM_3 in terms of the average output power, P_{av} to match the simulated data. Also, the exclusion of the inductance, L as observed in (4) to (7) from the original equations in [7] are needed to implement the two circuit topologies proposed, the "dual" and "series dual" BST varactor circuit.

The ideal dual BST varactor circuit topology is illustrated in Figure 3 and the IM_3 have been theoretically analysed in [13]. The concept of this topology was to integrate two identical BST varactors in a parallel mode with opposite bias voltages applied (antiparallel topology). Since the nonlinear C-V curve of the BST is symmetrical, either varactor can be forward or reverse biased, yielding the term "dual" topology. The DC blocking capacitor decoupled the varactors for individual biasing. Theoretically, by applying opposite bias voltages, the nonlinearity of one varactor will cancel the other and this will lead to the perfect cancellation of the second-order coefficient, C_1 [7, 13].

The ideal dual BST varactor circuit topology coefficients in Table 1 have subscripts "left" and "right" indicating the position of the varactors in the topology and the capacitance of each is half of the

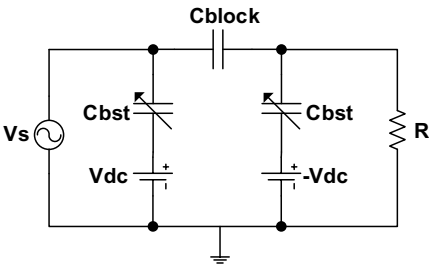

Figure 3. Ideal schematic of the dual BST varactor circuit topology.

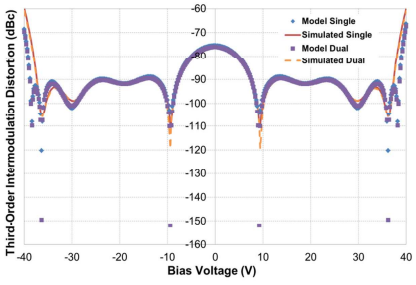

Figure 4. The third-order intermodulation distortion of model and simulated results for the dual BST varactor circuit topology.

single varactor for comparison. Also, the negative voltage, $-V_{dc}$ is applied to the right varactor. Here, it can be observed that the second-order coefficients, C_1 is perfectly cancelled out due to the sum of $C_{1\text{left}}$ and $C_{1\text{right}}$. The sums of "left" and "right" of similar coefficients are then substituted into (3) to (7) to compute the IM_3.

MAPLE and ADS software were utilised to compute the IM_3 equations and simulate the dual topology respectively. Two-tone signals, 1.80 GHz and 1.81 GHz were used. Here, the measured BST varactors with capacitance values of ~ 0.3 pF at 0 V were defined and the varactors were swept from -40 V to 40 V.

The IM_3 theoretical model and simulated results show excellent agreement. For the dual topology in Figure 4, it can be observed that the nulls are lower compared to the single topology at specific bias voltages, indicating minimum second-order coefficient, C_1. The first null can be achieved at ± 9 V with an average of 10 dB linearity improvement. The second null can be observed at ± 36 V with 13 dB linearity improvement. Hence, by proper tuning at a low voltage of ± 9 V, a significantly low theoretical IM_3 can be achieved. In the next section, with the introduction of a new topology, an improved IM_3 is expected over all bias voltages.

3.2. Theoretical Analysis of Series Dual BST Varactor Circuit Topology

The IM_3 equation in (3) is also applicable to the ideal series dual BST varactor circuit topology shown in Figure 5 by substituting the proper varactor coefficients. This topology is proposed to further reduce the nonlinearity in the dual topology. It has two identical BST varactors in series with opposite bias voltages applied (antiseries topology) and, in parallel with another identical set, yielding the term "series dual" topology.

In Table 2, the coefficients are summed up for the antiseries connections. Here, it can be observed that the second-order coefficient, C_1 is perfectly cancelled out and the third-order coefficient, C_2 is reduced significantly.

For the series dual topology in Figure 6, it can be observed that the entire IM_3 level has dropped significantly compared to the single topology. A 13 dB improvement can be achieved at 0 V and at higher bias voltages, an average of more than 40 dB improvement, starting from the first null at 20 V. The lower IM_3 achieved in this topology is due to the second and third-order coefficients being minimised [7].

Since measured BST capacitance values with slight tolerances between them were implemented in both dual and series dual topologies, the perfect cancellation of the second-order term or much

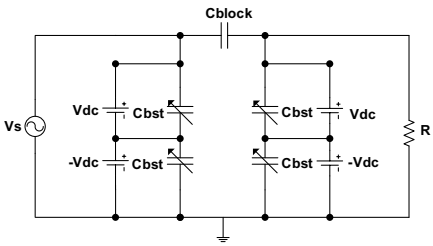

Figure 5. Ideal schematic of the series dual BST varactor circuit topology.

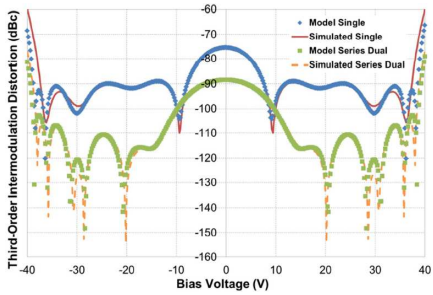

Figure 6. The third-order intermodulation distortion of model and simulated results for the series dual BST varactor circuit topology.

lower third-order term could not be achieved. However, linearity improvements can still be realised.

4. MEASUREMENTS AND ANALYSES

The selected IDCs as discussed in Section 2 were mounted on a 20 mm × 32 mm Rogers RO4003C board with a dielectric constant, ε_r of 3.38. Two diced chip varactors were positioned in between the 50 Ω microstrip signal lines and ground planes and, integrated in a dual BST varactor circuit topology. On another board, four diced chip varactors were integrated in a series dual BST varactor circuit topology. Each diced chip had three varactors in array (two varactors as spares) with a footprint of 1.5 mm × 2 mm. On both boards, a 22 pF SMT capacitor decoupled the left-hand and right-hand sides of the chip varactors for biasing purposes. These varactors were wirebonded to the external 50 Ω signal and ground Au-plated Cu microstrip lines. The circuit board was mounted on an aluminium block for mechanical stability. The Device Under Test (DUT) is shown in Figure 7.

The DUTs for both topologies were initially designed in ADS, including the microstrip lines, bondwires and SMT capacitors and simulations were performed. The third-order intermodulation distortion (IM_3) was then measured by applying two-tone input signals at 1.80 GHz and 1.81 GHz. The frequencies were chosen to accommodate for the measurement setup which operates within the frequency range of interest. The measurement setup is illustrated in Figure 8 which consisted of signal generators, amplifiers, bandpass

Table 2. Coefficients of ideal series dual BST varactor circuit topology.

C_{0left_sum}	$1/2K_0 + 1/2K_2(V_{dc})^2 + 1/2K_4(V_{dc})^4$ $+1/2K_6(V_{dc})^6 + 1/2K_8(V_{dc})^8 + 1/2K_{10}(V_{dc})^{10}$ $+1/2K_{12}(V_{dc})^{12} + 1/2K_{14}(V_{dc})^{14} + 1/2K_{16}(V_{dc})^{16}$
C_{0right_sum}	$1/2K_0 + 1/2K_2(V_{dc})^2 + 1/2K_4(V_{dc})^4$ $+1/2K_6(V_{dc})^6 + 1/2K_8(V_{dc})^8 + 1/2K_{10}(V_{dc})^{10}$ $+1/2K_{12}(V_{dc})^{12} + 1/2K_{14}(V_{dc})^{14} + 1/2K_{16}(V_{dc})^{16}$
C_{1left_sum}	0
C_{1right_sum}	0
C_{2left_sum}	$1/8[K_2 + 6K_4(V_{dc})^2 + 15K_6(V_{dc})^4 + 28K_8(V_{dc})^6$ $+45K_{10}(V_{dc})^8 + 66K_{12}(V_{dc})^{10} + 91K_{14}(V_{dc})^{12}$ $+120K_{16}(V_{dc})^{14}][1 - [1.5[2K_2V_{dc} + 4K_4(V_{dc})^3$ $+6K_6(V_{dc})^5 + 8K_8(V_{dc})^7 + 10K_{10}(V_{dc})^9 + 12K_{12}(V_{dc})^{11}$ $+14K_{14}(V_{dc})^{13} + 16K_{16}(V_{dc})^{15}]^2/[K_0 + K_2(V_{dc})^2$ $+K_4(V_{dc})^4 + K_6(V_{dc})^6 + K_8(V_{dc})^8 + K_{10}(V_{dc})^{10}$ $+K_{12}(V_{dc})^{12} + K_{14}(V_{dc})^{14} + K_{16}(V_{dc})^{16}][K_2$ $+6K_4(V_{dc})^2 + 15K_6(V_{dc})^4 + 28K_8(V_{dc})^6 + 45K_{10}(V_{dc})^8$ $+66K_{12}(V_{dc})^{10} + 91K_{14}(V_{dc})^{12} + 120K_{16}(V_{dc})^{14}]]]$
C_{2right_sum}	$1/8[K_2 + 6K_4(V_{dc})^2 + 15K_6(V_{dc})^4 + 28K_8(V_{dc})^6$ $+45K_{10}(V_{dc})^8 + 66K_{12}(V_{dc})^{10} + 91K_{14}(V_{dc})^{12}$ $+120K_{16}(V_{dc})^{14}][1 - [1.5[2K_2V_{dc} + 4K_4(V_{dc})^3$ $+6K_6(V_{dc})^5 + 8K_8(V_{dc})^7 + 10K_{10}(V_{dc})^9 + 12K_{12}(V_{dc})^{11}$ $+14K_{14}(V_{dc})^{13} + 16K_{16}(V_{dc})^{15}]^2/[K_0 + K_2(V_{dc})^2$ $+K_4(V_{dc})^4 + K_6(V_{dc})^6 + K_8(V_{dc})^8 + K_{10}(V_{dc})^{10}$ $+K_{12}(V_{dc})^{12} + K_{14}(V_{dc})^{14} + K_{16}(V_{dc})^{16}][K_2$ $+6K_4(V_{dc})^2 + 15K_6(V_{dc})^4 + 28K_8(V_{dc})^6$ $+45K_{10}(V_{dc})^8 + 66K_{12}(V_{dc})^{10}$ $+91K_{14}(V_{dc})^{12} + 120K_{16}(V_{dc})^{14}]]]$

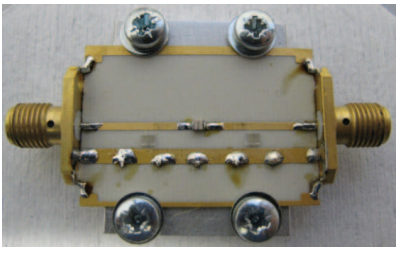

Figure 7. Device under test of the dual BST varactor circuit topology.

filters, isolators, a power combiner, bias tees, power supplies, an attenuator and a spectrum analyser. Power amplifiers were used to generate sufficiently high input power levels to enable the BST varactors to produce IM_3 peaks above the noise floor. Each power amplifier has a built-in isolator to prevent the signals from reflecting back to it and the signal generators. Also, the isolator helps in avoiding possible leak-through from one signal generator to another [12]. Insertion losses between 0.5 dB to 1 dB were achieved when the DUTs were connected between the bias tees.

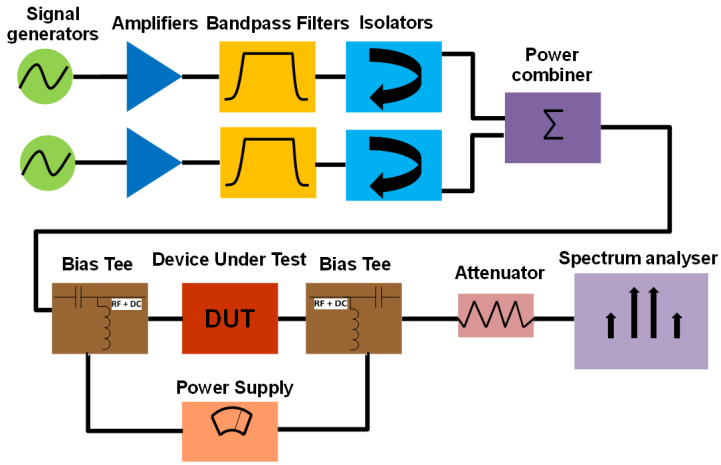

Figure 8. The third-order intermodulation distortion measurement setup.

For the dual topology, the IM_3 simulated and measured results are shown in Figure 9 with the BST varactors biased up to ±25 V. The measured first null is achieved at ±13 V, a ±4 V shift from the ideal value, however good agreement is observed where the general trend of reduced distortion is realized. A 5 dB deviation at higher voltages starting from 20 V between the simulated and measured data is observed.

In Figure 10, the entire IM_3 level has dropped about 5 dB for the series dual topology compared to the dual topology at 0 V. The measured first null was achieved at ±20 V with a ±8 V shift from the ideal value, though good agreement is observed. The general trend of much reduced distortion compared to the dual topology is realized. In comparison with Figure 6, the first null of this simulated result becomes significant at ±13 V due to the extra "islands" introduced in the circuit. These islands are basically small area of microstrip lines

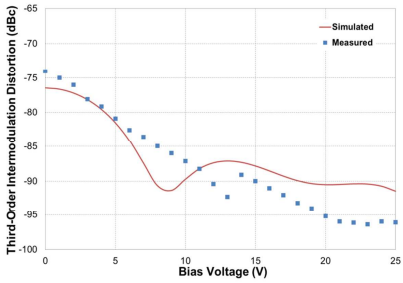

Figure 9. The third-order intermodulation distortion of simulated and measured results for the device under test of dual BST varactor circuit topology.

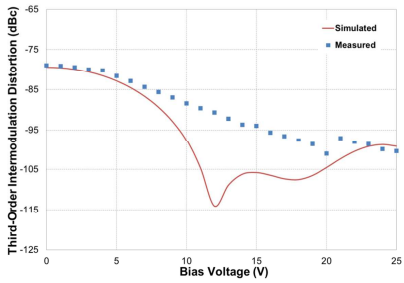

Figure 10. The third-order intermodulation distortion of simulated and measured results for the device under test of series dual BST varactor circuit topology.

which served as negative nodes for opposite biasing of the varactors.

The voltage shifts in both topologies were most likely to be caused by the degradation in the tunability of the BST varactors due to the compression of the C-V curves resulting from the high input power levels [18]. As shown in Figure 11, the compression of the C-V curves for the single BST varactor due to a continuous increase in input power levels, results in the degradation of its tunability. It can be observed that as the input power increases from 0 to 30 dBm, the peak capacitance ($C_{\max}$) at 0 V starts to compress. In Figure 12, the nulls are shifting to higher voltages as the input power increases. As observed, the first nulls are shifted to 9, 11 and 15 V for 20, 25 and 30 dBm respectively. An alternative to reduce this degradation is to increase the stacking of the BST varactors similar to [8].

The dual topology C-V curve is compressed further compared to the series dual topology due to the larger RF swing across the varactors, resulting in a broader C-V curve. A broader C-V curve tends to have better IM_3 which contributes to a higher third-order intercept point (IP_3). This justified the slight deviation between the simulated and measured data at higher voltages in Figure 9.

Several single bondwires were also used on the DUTs, mainly in the series dual topology, which contributed to the parasitic inductances and degraded the IM_3 level. Figure 13 shows the simulation which confirmed the effects of these inductances that degraded the IM_3 level by 6 dB at 0 V.

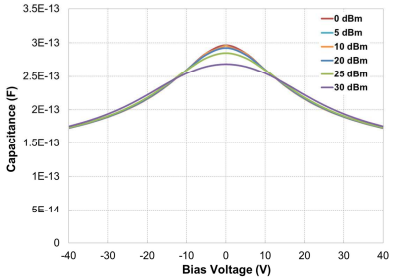

Figure 11. Compression of the C-V curves for the single BST varactor due to increasing input power.

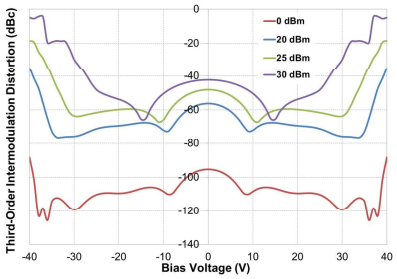

Figure 12. Shifting of the nulls in the dual BST varactor circuit topology due to increasing input power.

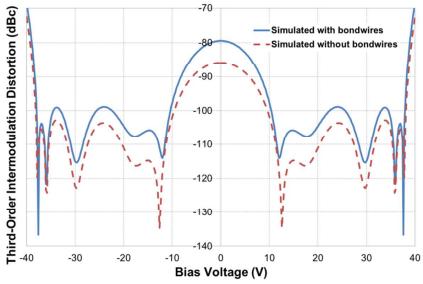

Figure 13. Bondwire effects which degraded the linearity.

5. CONCLUSION

A new method for the theoretical analysis of the third-order intermodulation distortion in BST thin film interdigital capacitors on r-plane sapphire substrates has been presented. Two circuit topologies have been proposed for linearity improvement. Results from the developed theoretical models have been presented and compared with simulated and measured results. By biasing appropriately, significantly low nulls can be achieved due to minimum distortions. The performance degradation caused by tunability compression and bondwires have been confirmed through simulation. The good linearity achieved in these circuit topologies has the potential to be implemented in silicon on sapphire applications.

REFERENCES

1. Gevorgian, S., "Introduction: Overview of agile microwave technologies," *Ferroelectrics in Microwave Devices, Circuits and Systems: Physics, Modelling, Fabrication and Measurements*, 1st Edition, 1–19, Springer-Verlag, London, 2009.
2. Wee, F. H., M. F. B. A. Malek, S. Sreekantan, A. U. Al-Amani, F. Ghani, and K. Y. You, "Investigation of the characteristics of barium strontium titanate (BST) dielectric resonator ceramic loaded on array antennas," *Progress In Electromagnetics Research*, Vol. 121, 181–213, 2011.
3. Cristoloveanu, S., "Silicon films on sapphire," *Rep. Prog. Phys.*, Vol. 50, No. 3, 327–371, Mar. 1987.
4. Fardin, E. A., A. S. Holland, K. Ghorbani, E. K. Akdogan, W. K. Simon, A. Safari, and J. Y. Wang, "Polycrystalline $Ba_{0.6}Sr_{0.4}TiO_3$ thin films on r-plane sapphire: Effect of film thickness on strain and dielectric properties," *Appl. Phys. Lett.*, Vol. 89, No. 18, Art. No. 182907, Nov. 2006.
5. Jiang, H., B. Lacroix, K. Choi, Y. Wang, A. T. Hunt, and J. Papapolymerou, "Ka- and U-band tunable bandpass filters using ferroelectric capacitors," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 59, No. 12, 3068–3075, Dec. 2011.
6. Zhao, Z., X. Wang, K. Choi, C. Lugo, and A. T. Hunt, "Ferroelectric phase shifters at 20 and 30 GHz," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 55, No. 2, 430–437, Feb. 2007.
7. Meyer, R. G. and M. L. Stephens, "Distortion in variable-capacitance diodes," *IEEE J. Solid-State Circuits*, Vol. 10, No. 1, 47–54, Feb. 1975.
8. Fu, J.-S., X. A. Zhu, J. D. Phillips, and A. Mortazawi, "Improving linearity of ferroelectric-based microwave tunable circuits," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 55, No. 2, 354–360, Feb. 2007.
9. Chen, K., X. Liu, A. Kovacs, W. J. Chappell, and D. Peroulis, "Antibiased electrostatic RF MEMS varactors and tunable filters," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 58, No. 12, 3971–3981, Dec. 2010.
10. Buisman, K., L. C. N. de Vreede, L. E. Larson, M. Spirito, A. Akhnoukh, T. L. M. Scholtes, and L. K. Nanver, "'Distortion-free' varactor diode topologies for RF adaptivity," *IEEE MTT-S Int. Microw. Symp. Dig.*, 157–160, Long Beach, CA, 2005.
11. Huang, C., K. Buisman, M. Marchetti, L. K. Nanver, F. Sarubbi, M. Popadić, T. L. M. Scholtes, H. Schellevis, L. E. Larson,

and L. C. N. de Vreede, "Ultra linear low-loss varactor diode configurations for adaptive RF systems," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 57, No. 1, 205–215, Jan. 2009.

12. Fu, J.-S., X. A. Zhu, D.-Y. Chen, J. D. Phillips, and A. Mortazawi, "A linearity improvement technique for thin-film barium strontium titanate capacitors," *IEEE MTT-S Microw. Symp. Dig.*, 560–563, San Francisco, CA, 2006.
13. Abdul Khalid, M. F., A. S. Holland, J. R. Scott, and K. Ghorbani, "Analysis of third-order intermodulation distortion in BST varactors," *Proc. 2010 Asia-Pacific Microw. Conf.*, 650–653, Yokohama, Japan, 2010.
14. Fardin, E. A., "Barium strontium titanate thin films for tunable microwave applications," Ph.D. Thesis, School Elect. and Comput. Eng., RMIT Univ., Melbourne, Australia, 2007.
15. Fardin, E. A., A. S. Holland, K. Ghorbani, and P. Reichart, "Enhanced tunability of magnetron sputtered $Ba_{0.5}Sr_{0.5}TiO_3$ thin films on *c*-plane sapphire substrates," *Appl. Phys. Lett.*, Vol. 89, No. 2, Art. No. 022901, Jul. 2006.
16. Acikel, B., "High performance barium strontium titanate varactor technology for low cost circuit applications," Ph.D. Thesis, Dept. Elect. and Comput. Eng., Univ. of California, Santa Barbara, CA, 2002.
17. Chase, D. R., L.-Y. Chen, and R. A. York, "Modeling the capacitive nonlinearity in thin-film BST varactors," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 53, No. 10, 3215–3220, Oct. 2005.
18. Tombak, A., J.-P. Maria, F. Ayguavives, Z. Jin, G. T. Stauf, A. I. Kingon, and A. Mortazawi, "Tunable barium strontium titanate thin film capacitors for RF and microwave applications," *IEEE Microw. Wireless Compon. Lett.*, Vol. 12, No. 1, 3–5, Jan. 2002.