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WI-FI ENERGY HARVESTER FOR LOW POWER RFID APPLICATION

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Abstract—In recent years, active Radio Frequency Identification (RFID) tags have crossed into ultra low power domain. With obvious advantages over passive tags, a setback for active tag growth is the need for battery replacement and limited operational life. Battery life could be extended by scavenging surrounding Wi-Fi signals using rectenna architecture which consists of a receiving antenna attached to a rectifying circuit. A seven stage Cockroft-Walton voltage multiplier optimized for low input power (below 0 dBm) is proposed. Prototype was fabricated on RT/Duroid 5880 (RO5880) printed circuit board (PCB) substrate with dielectric constant and loss tangent of 2.2 and 0.0009 respectively. Experimental results show that 2 V output voltage can be harvested from an operating frequency of 2.48 GHz with −9 dBm (0.13 mW) sensitivity with 1.57 mm board thickness.

1. INTRODUCTION

Renewable energy has evolved to include micro energy harvesting. Once dismissed as nonviable power supply, ambient radio frequency (RF) is now a realizable energy source with the advent of ultra low power devices. With technology roadmaps keeping power consumption at bare minimum, integrated environmental energy scavengers within low power device applications will likely be the most economical and reasonable solution to battery powered systems.

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One such system would be active RFID tag technology where battery replacement is seen as a barrier that is inhibiting its growth. In spite of benefits including longer range capability and better reliability, passive tags command a substantial market share because they are cheap and battery free [1]. Interestingly, RFID market intelligence has forecasted wider acceptance of this emerging technology in the next 10 years [2]. Overcoming the need for frequent battery change could propel the popularity of active tags.

Scavenging ambient Wi-Fi transmission through the rectenna model can be a possible solution to prolong the battery life of the active RFID tag. Wi-Fi networks are becoming more accessible. Global market survey showed unprecedented growth in Wi-Fi hotspot deployments with an estimated 350% rise by 2015 [3]. With the entry of active RFID tags operating on very low power consumption, harvested Wi-Fi power in the sub-microwatt range would not be deemed useless. A similar approach was undertaken by Hande et al., whereby vibration energy harvesting was explored to increase battery life of active RFID tag. The developed prototype was capable of delivering 20 μW of continuous power with 2 V output voltage at low excitation levels of $0.06g_{\text{peak}}$ [4].

We define the boundaries of our research by benchmarking against the piezoelectric energy harvester design. Investigation will focus on RF energy conversion element and integration with harmonic suppression filters. We anticipate a minimum output voltage of 2 V and output power between 18–30 μW [4]. Measurement results will gauge operating voltage under 1 MΩ load which is an approximation of 2 MΩ ultra low power resistive load model from Pillai et al. [5]. The working prototype has to be optimized for low Wi-Fi signals from Wireless Access Point. RF exposure from Wi-Fi was measured to be between 0.37 V/m and 5.63 V/m in a study conducted by Universiti Putra Malaysia which translates to be in the vicinity of −5 to −28 dBm [6]. Hence, we evaluate prototype performance with low RF input signal from 0 till −20 dBm.

There is inherent trade-off between maximum output voltage and efficiency [7]. Other research papers investigate from the angle of varying resistive load to achieve highest possible efficiency. In our case, resistive load has been modelled after ultra low power active RFID tag application which inevitably produces low efficiency. Hence, the focus is on maximum output voltage instead of high efficiency.

Rectenna framework is discussed in Section 2 based on literature review and other related works. Section 3 details the design realization of integrating chip band pass filter (BPF) and lumped element DC lowpass filter (LPF) within a multistage rectifier followed by laboratory

setup methodology. We present simulation work and experimental results of fabricated prototype in Section 4 with analyses of empirical data. And finally, we conclude findings of this study in Section 5.

2. RECTENNA ARCHITECTURE

A rectenna is a hybrid between a receiving antenna and a rectifying circuit that converts microwave energy to DC power. As shown in Figure 1, a conventional rectenna constitutes an antenna, a matching circuit, LPF, rectifying circuit, post-rectification LPF for DC path and a resistive load [8]. To keep within the scope of our research, antenna design and matching network will not be discussed in ensuing sections.

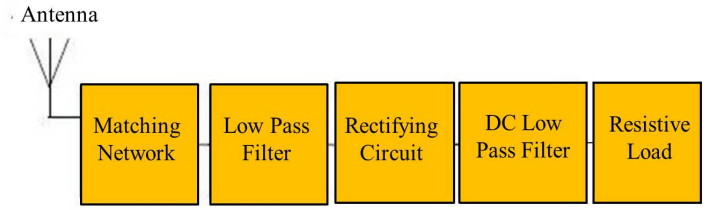

Figure 1. Conventional rectenna architecture.

2.1. Rectifier Topology

The choice of rectifying circuit topology is crucial for reliable device operation. Commonly associated modules include Schottky diodes based Cockroft-Walton, Dickson or Greinacher rectifiers. We understand that higher DC voltage can be achieved when low threshold Schottky diodes in multiple stages are employed. However, cascading too many stages may result in decreased input impedance caused by accumulated parasitic capacitances at high frequency. Consequently, a lower output voltage occurs instead [9]. Similarly, low junction capacitance and low series resistance are critical diode parameters within the voltage multiplier [10].

We pursue the Cockroft-Walton scheme because of design simplicity, taking the form of a half-wave rectifier compared to full-wave Greinacher rectifier. This would provide greater flexibility in improving the number of stages as diodes in Greinacher circuits are double that of Cockroft-Walton topology. Looking ahead, we foresee the potential to migrate unique traits from this study to CMOS chip process as evidenced by published work from Chow et al. [11].

Table 1 gives a comparison of 2 works depicting single stage Cockroft-Walton voltage multiplier performance. Extracted output

voltage reached 2.15 V and 1.54 V from RO5880 and FR4 substrates respectively with 0 dBm RF input signal.

Table 1. Comparison of single stage voltge multiplier performance.

Ref.	Substrate	Dielectric Thickness (mm)	Center Freq. (GHz)	P_{in} (mW)	R_{load} (kΩ)	V_{out} (V)
[12]	RO5880	0.787	2.630	1.0	7.88	2.15
[13]	FR4	0.787	0.925	1.0	5.00	1.54

Capacitance value for overall system was also considered. Each stage maintained same value of 1 µF except for the output capacitance before load, in which we evaluate with a smaller 1 nF capacitance to increase the speed of the transient response [14]. Optimization of the multistage rectifier is required to ensure maximum output voltage is achieved under low input condition at 2.4 GHz band.

2.2. Harmonic Rejection Filters

Filters are needed to attenuate high frequency harmonics present in the RF signal or generated by the highly nonlinear rectification process. Suppressing higher order harmonics aids in increasing output power at the fundamental frequency [15]. Pre-rectification and post-rectification signals can be filtered to remove unwanted harmonics in order to obtain additional output voltage. This was effectively portrayed by Y. Kim and S. Lim utilizing BPF and LPF in microstrip form within their rectenna design [16]. The relationship between power, P and RMS voltage, V_{RMS} for typical 50 Ω RF system and 1 mW reference wattage is given in Equation (1) [17]

$$P\,(\text{dBm}) = 20\log(V_{RMS}/0.224) \tag{1}$$

For our rectifier system, we incorporate a multilayer ceramic BPF for 2.4 GHz band and realize the DC LPF with lumped passive components. Accordingly, surface mount devices can be used to realize filters with operating frequencies up to a few GHz [18]. It is evident from Table 1 that RO5880 laminate has favorable power extraction qualities over FR4 laminate. Hence, RO5880 laminate with dielectric constant of 2.2 and loss tangent of 0.0009 was chosen.

Smallest overshoot characteristic in Bessel LPF appealed to our application where pulsed signals from Wireless Access Point could change abruptly [18]. The minimum order of the filter was then determined based on guiding principles from author W.-K. Chen [19]. Taking zero frequency delay of 230 psec that remains

nominally constant for signal frequencies up to 3 GHz, corresponding delay for 2.45 GHz cutoff frequency was found to be 188 psec [20]. The normalized frequency at 2.45 GHz was then calculated using Equation (2)

$$\omega T = 2 \times \pi \times 2.45 \times 188 = 2.9 \tag{2}$$

Based on 3 dB bandwidth requirement whereby maximum deviation in magnitude should not exceed 3 dB, we find that seventh order response in Figure 2 satisfies this criteria.

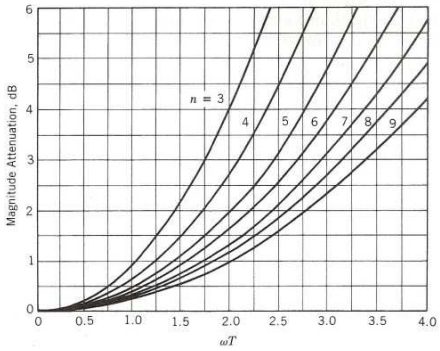

Figure 2. Magnitude error in dB as a function of normalized frequency ωT for various values of order n.

3. DESIGN AND FABRICATION

3.1. Harmonic Balance Simulation

Simulation was done using Harmonic Balance function in ADS software to compute the steady state solution of the nonlinear circuit [10]. HSMS286C SPICE parameters and equal stage capacitance apart from output capacitance were applied. Initial simulation using 0.787 mm RO5880 substrate showed that a 7 stage Cockroft-Walton rectifier with Bessel LPF would produce desired response. We increase to 8 stage rectification and investigate 1.57 mm thickness. Output voltage under 1 MΩ load was recorded with single fundamental RF tone signal from 2.40 GHz to 2.48 GHz. Input power varied from 0 till −20 dBm. Schematic designs of multistage rectifiers were then realized using Eagle PCB Design software to validate findings from simulation work.

3.2. Bessel Lowpass Filter Design

Seventh order Bessel LPF was designed to have cutoff frequency of −3 dB at 2.45 GHz which is the center frequency of Wi-Fi band. Fine

tuning of passive components and trace dimensions were carried out in order to generate maximum output voltage when combined with multistage rectifier in Harmonic Balance environment. Layout designs were then generated using Momentum.

3.3. Printed Circuit Board Fabrication

Once finalized, designs were submitted to PCB laboratory for photolitography process. Next, passive components were manually soldered using soldering kit.

3.4. Experimental Setup

Figure 3 shows laboratory setup involved with the measurement of developed prototypes. Due to non-linear nature of the cascaded multiplier, a methodology was developed to minimize data variation. Readings were recorded after achieving steady state condition. Input signal was evaluated in a descending manner with decreasing single step starting from 0 dBm.

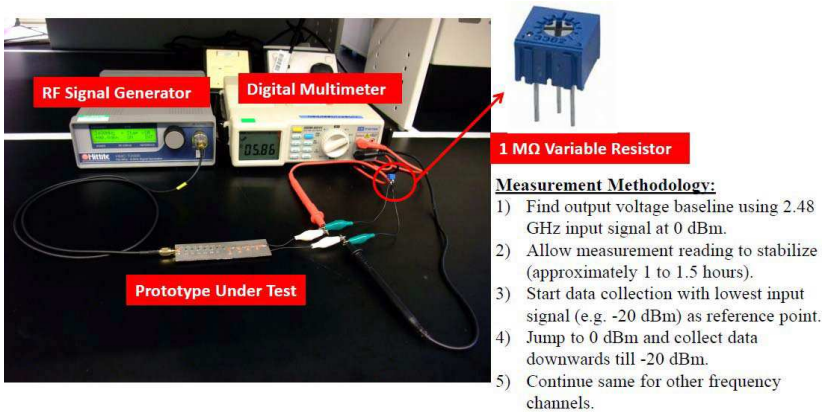

Figure 3. Experimental setup to measure output voltage.

4. RESULTS AND DISCUSSIONS

4.1. Post-rectification Filter Performance

Seventh order Bessel LPF was designed to increase output voltage at the load. Harmonic Balance simulation showed improved output voltage when LPF was integrated with 7 stage rectifier. Optimized components and filter layout corresponding to increased output voltage for both dielectric thicknesses are shown in Figure 4.

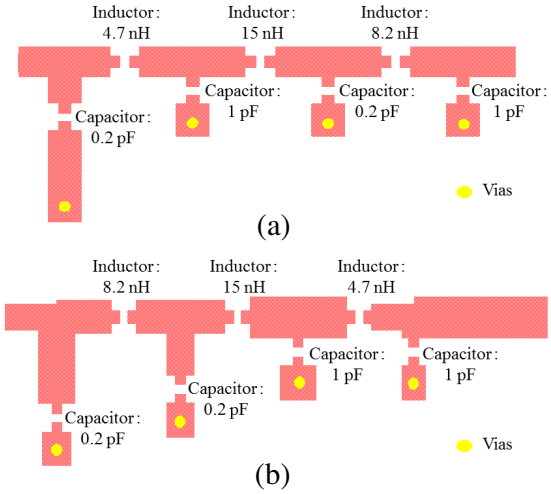

Figure 4. Finalized post-rectification Bessel LPF. (a) 0.787 mm RO5880 Bessel LPF. (b) 1.57 mm RO5880 Bessel LPF.

Table 2 shows measured results of 0.787 mm RO5880 prototypes at 2.40 GHz, 2.45 GHz and 2.48 GHz when input is varied from 0 till −10 dBm while Table 3 shows data of 1.57 mm board thickness under similar conditions.

Experimentally, output voltage increment was observed only for 1.57 mm RO5880 laminate with the addition of LPF across 2.4–2.48 GHz range. However, for thinner 0.787 mm board, reduced output voltage was observed across 2.4 GHz band. Within a lumped element lowpass filter, thicker dielectric height gave better performance compared to a thinner one. This can be explained as dominating parasitic influences impeding voltage gain as a result from a study investigating the effects of dielectric thickness on lumped element LPF using RO5880 material which revealed that thicker dielectric height with lower effective dielectric constant produced better output response [21].

We note with interest that highest output voltage came from 2.48 GHz. This observation is consistent with the findings of Mikeka and Arai, where voltage doubler configuration experienced reducing junction capacitance from Schottky diodes as frequency increased [22]. Thus, remaining results will undertake condition of 2.48 GHz RF input signal with 1 MΩ load in the quest to achieve highest possible DC voltage. The effects of RO5880 laminate thickness is graphically represented in Figure 5.

Table 2. Effect of adding LPF to 7 stage rectifier across 2.4 GHz band on 0.787 mm RO5880 laminate.

RF Input Power (dBm)	DC Output Voltage (V)					
	2.40 GHz Frequency		2.45 GHz Frequency		2.48 GHz Frequency	
	7 Stage Rectifier Only	7 Stage Rectifier + LPF	7 Stage Rectifier Only	7 Stage Rectifier + LPF	7 Stage Rectifier Only	7 Stage Rectifier + LPF
0	1.23	0.84	3.21	1.14	4.99	1.51
−1	1.01	0.63	2.84	0.91	4.49	1.26
−2	0.82	0.46	2.52	0.71	4.01	1.04
−3	0.62	0.32	2.15	0.52	3.44	0.80
−4	0.48	0.23	1.87	0.39	2.96	0.63
−5	0.39	0.17	1.64	0.30	2.51	0.49
−6	0.30	0.12	1.43	0.23	2.04	0.38
−7	0.22	0.09	1.30	0.19	1.71	0.34
−8	0.17	0.07	1.10	0.14	1.16	0.25
−9	0.13	0.05	0.93	0.10	0.75	0.19
−10	0.10	0.04	0.72	0.07	0.39	0.13

Table 3. Effect of adding LPF to 7 stage rectifier across 2.4 GHz band on 1.57 mm RO5880 laminate.

RF Input Power (dBm)	DC Output Voltage (V)					
	2.40 GHz Frequency		2.45 GHz Frequency		2.48 GHz Frequency	
	7 Stage Rectifier Only	7 Stage Rectifier + LPF	7 Stage Rectifier Only	7 Stage Rectifier + LPF	7 Stage Rectifier Only	7 Stage Rectifier + LPF
0	1.15	1.44	2.74	3.20	4.56	4.89
−1	0.94	1.20	2.43	2.84	4.15	4.44
−2	0.75	0.98	2.16	2.51	3.77	4.02
−3	0.56	0.75	1.84	2.14	3.32	3.55
−4	0.43	0.59	1.60	1.87	2.97	3.18
−5	0.34	0.46	1.40	1.63	2.66	2.85
−6	0.26	0.37	1.22	1.42	2.36	2.55
−7	0.19	0.27	1.11	1.30	2.16	2.36
−8	0.14	0.21	0.94	1.10	1.84	2.05
−9	0.11	0.16	0.80	0.94	1.53	1.77
−10	0.08	0.12	0.63	0.74	1.03	1.37

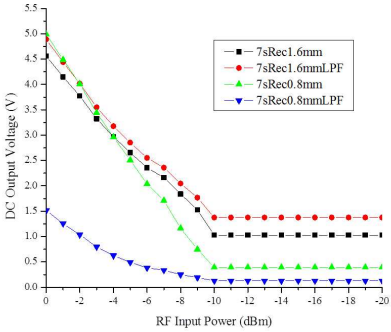

Figure 5. Effect of dielectric height on lumped element LPF.

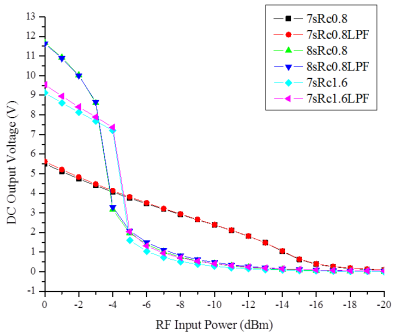

Figure 6. Simulation to find optimum number of stages.

4.2. Optimum Stages of Multiplication

Seven stage rectification is optimum under low input power. Lower voltage is attained with 8 stage circuit when input signal is unable to overcome parasitics from increased diodes. ADS simulation results are captured in Figure 6. We see that 7 stage 0.787 mm rectifier with LPF has the best performance below −5 dBm input signal with extra voltage gain over stand alone rectifier. Experimental results concurred that 7 stage was indeed optimum as displayed in Figure 7. However, the highest output voltage came from 1.57 mm prototype and not the thinner laminate. Influence of parasitics induced by thin dielectric height was not consolidated inside simulation which would result in lower DC voltage. Minimum input power to achieve 2 V for 7 stage 1.57 mm RO5880 integrated rectifier and Bessel LPF is −8 dBm (0.16 mW). We note that as input approaches below −10 dBm, there is a stagnation which demonstrates the nonlinear behavior and parasitic effects of the system. Instead of seeing a further voltage drop as input signal diminishes, we are confronted with raised input impedance. This condition was also observed by Nintanavongsa et al. [10].

4.3. Output Voltage Booster

In the context of boosting higher output voltage, multilayer ceramic BPF can be added. We see a progression of output voltage gain in Figure 8. Integrated BPF and LPF within 7 stage rectifier on 1.57 mm RO5880 laminate is pictured in Figure 9. Minimum input power to achieve 2 V improved from −8 dBm (0.16 mW) to −9 dBm (0.13 mW).

Table 4 gives a comparison of current data against earlier work. 7 stage rectification appears to be a common thread. Although

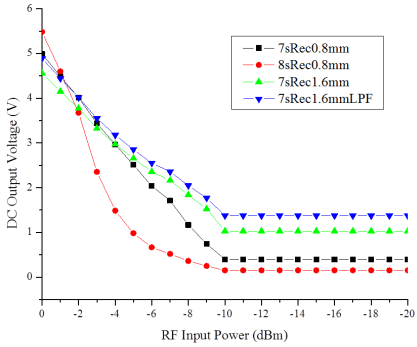

Figure 7. Measured data from various prototypes.

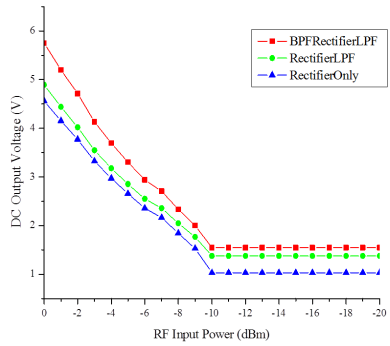

Figure 8. Output voltage gain progression.

resistive load is non-uniform, results do suggest strong leaning towards RO5880 high frequency laminate in the context of low power microwave energy conversion. While maintaining board thickness of 1.57 mm and employing Cockroft-Walton configuration, our prototype on RO5880 substrate was able to harvest slightly more output voltage compared to the prototype by Din et al.. Output voltage of 1.5 V was harvested with input power of 0.1 mW (−10 dBm). Apart from that, we were able to minimize the form factor of our prototype which has a dimension of 95 mm × 24 mm compared to PCB dimension of 98 mm × 34 mm developed by Din et al. The size reduction of assembled circuit board is attributed to the use of surface mount device (SMD) components in pre-rectification and post-rectification filters along with the choice of series pair configuration instead of single configuration for SMD Schottky diodes.

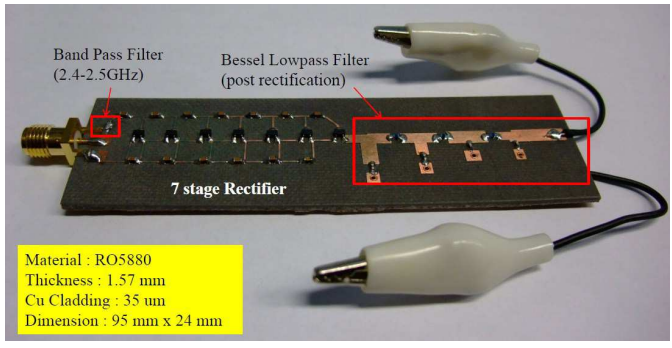

Figure 9. Integrated BPF and LPF within 7 stage rectifier.

Table 4. Comparison of 7 stage voltge multiplier performance.

Ref.	PCB	Circuit	Dielectric Thickness (mm)	Center Freq. (GHz)	P_{in} (mW)	R_{load} (kΩ)	V_{out} (V)
[10]	FR4	D†	1.57	0.915	0.1	100	∼0.3
[23]	FR4	C-W‡	1.57	0.900	0.1	100	∼1.4
This work	RO5880	C-W	1.57	2.480	0.1	1000	1.5

†Dickson
‡Cockroft-Walton

5. CONCLUSIONS

A multiple stage Cockroft-Walton rectifier suitable for low RF power energy harvesting has been presented in this article. Cascading multiple stages is limited by parasitic capacitance build up from passive components and dielectric laminate. Ceramic chip BPF and lumped element Bessel LPF are effective means of obtaining higher DC voltage. Harmonic Balance simulation was capable of evaluating optimum multiplication stage but was unable to include parasitic influences when dielectric thickness varied. We conclude that integrated BPF and LPF within 7 stage rectifier using 1.57 mm laminate is optimum for low power Wi-Fi signals. Experimental prototype showed higher output voltage in comparison with earlier published work when RO5880 laminate is utilized.

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