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STUDY OF THE COIL STRUCTURE FOR WIRELESS CHIP-TO-CHIP COMMUNICATION APPLICATIONS

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Abstract—In this work, we propose a merged coil structure for wireless chip-to-chip communication technology. Using the proposed coil structure, the chip size can be reduced, and the transmitted power can be improved by approximately 5 dB compared to typical coil structure. To verify the feasibility of the coil, an electromagnetic simulation and a schematic simulation are performed. The coil was implemented using 50-nm digital CMOS technology. From the experimental results, the feasibility was proved.

1. INTRODUCTION

Recently, three-dimensional (3D) semiconductors have been studied closely as researchers seek to reduce the system sizes and enhance the operating frequencies. Because data transmission is performed through a bonder-wire and PCB line for the two-dimensional (2D) semiconductor technology, the inductance of the bonder-wire and PCB line limits the data transmission speed. The 3D semiconductor was introduced to solve the various problems associated with 2D semiconductors. The physical path between the I/O PADs of each chip can be minimized compared to 2D semiconductor cases. In general, because there are no PCB lines between the chips, there is no parasitic inductance created by the PCB lines to enhance the signal or data transmission speed of the entire system.

The wireless chip-to-chip communication (WCC) method is especially regarded as next-generation 3D semiconductor technology,

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while the multi-chip package (MCP) [1] and through-silicon via (TSV) [2, 3] technologies are current technologies. Figure 1 shows a conceptual diagram of the WCC technology. As shown in Figure 1, wires and through-silicon vias are not required to communicate between stacked chips. Accordingly, the cost of the overall system can be reduced compared to the MCP and TSV technologies. WCC technology can solve the problems of many long bonder-wires and various resonance frequencies arising from MCP technology. Additionally, the problems related to the development cost and the low yield of TSV technology can be solved using WCC technology. However, few studies have focused on WCC technology because this technology requires digital IC and electromagnetic field knowledge simultaneously.

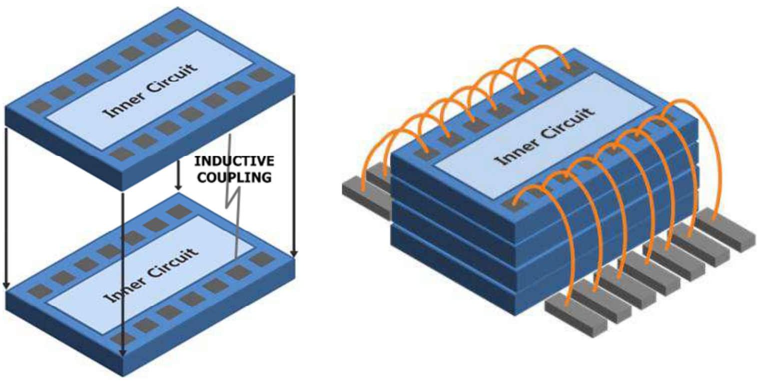

Figure 1. Conceptual diagram of wireless chip-to-chip communication.

In this study, we focus on the coil structures to improve the wireless communication quality in WCC technology. The coil is an essential component in systems that employ WCC technology [4–6]. We introduce typical coil related to the transmitted power and overall sizes. Finally, we propose a coil structure for WCC technology to improve the transmitted power and to reduce the overall size of the coil.

2. TYPICAL COIL STRUCTURE

Typical type of coil is the overlaid coil design, as shown in Figure 2 [7]. Figure 2 shows that the Tx. and Rx. coils are overlaid on each other. Typically, the Rx. coil is located on the outer side so as to receive the transmitted wireless data effectively. If the C_{O_T1} (or C_{O_T2}) and

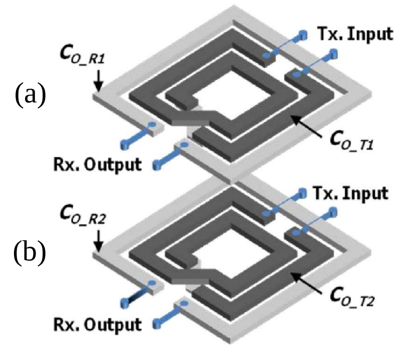

Figure 2. Typical coil for the wireless chip-to-chip communication.

C_{O_R1} (or C_{O_R2}) coils of the overlaid type operate simultaneously, the crosstalk between adjacent C_{O_T1} (or C_{O_T2}) and C_{O_R1} (or C_{O_R2}) coils distorts the required data communication. In this case, data transmission and reception cannot occur simultaneously.

Although the requirement that the Tx. and Rx. operation must be performed using a time-division process is satisfied, cross-talk problems between adjacent C_{O_T1} (or C_{O_T2}) and C_{O_R1} (or C_{O_R2}) coils can still arise. For successful wireless chip-to-chip communication, the signal power transmitted from C_{O_T1} must be coupled with the desired coil, C_{O_R2} in Figure 2(b). However, the signal transmitted from C_{O_T1} is also coupled to the undesired adjacent coil, C_{O_R1}, which is located in the same chip area as C_{O_T1}. The undesired coupling between the C_{O_T1} (or C_{O_T2}) and C_{O_R1} (or C_{O_R2}) coils located on the same chip leads to data loss and/or distorts the wireless data. To moderate the cross-talk problems, the distance between the stacked chips needs to be decreased.

For the sake of simplicity, we assume that only C_{O_T1} carries current. The magnetic coupling ϕ_{O_T1} emanating from C_{O_T1} has four components: one component ϕ_{O_T1T1} links only C_{O_T1}, ϕ_{O_T1R1} links C_{O_T1} and C_{O_R1}, ϕ_{O_T1T2} links C_{O_T1} and C_{O_T2}, and ϕ_{O_T1R2} links C_{O_T1} and C_{O_R2}. Hence, the emanating magnetic flux ϕ_{O_T1} can be described as follows:

$$\phi_{O\_T1} = \phi_{O\_T1T1} + \phi_{O\_T1R1} + \phi_{O\_T1T2} + \phi_{O\_T1R2} \quad (1)$$

Among the various components of ϕ_{O_T1}, only ϕ_{O_T1R2} is a desired component for WCC technology. The other components are undesired and may distort and degrade the wireless data. Thus, the coupling coefficient for the designed coupling is described as follows:

$$k_O = \phi_{O\_T1R2}/\phi_{O\_T1} \quad (2)$$

3. PROPOSED COIL STRUCTURE — MERGED COIL TYPE

We proposed the merged coil type to solve the additional chip size and the cross-talk problems of the overlaid type. A conceptual figure of the proposed type is shown in Figure 3. In the proposed type, the Rx. and Tx. coils are not distinguished, unlike in the typical type. The coils of C_{M_1} and C_{M_2} shown in Figure 3 can operate as Tx. or Rx. coils by means of a time-division process. During the Tx. operation of the system, the receiver of the chip is turned off and the coil serves as the transmitter. Similarly, during the Rx. operation of the system, the transmitter of the chip is turned off and the coil plays the role of the receiver.

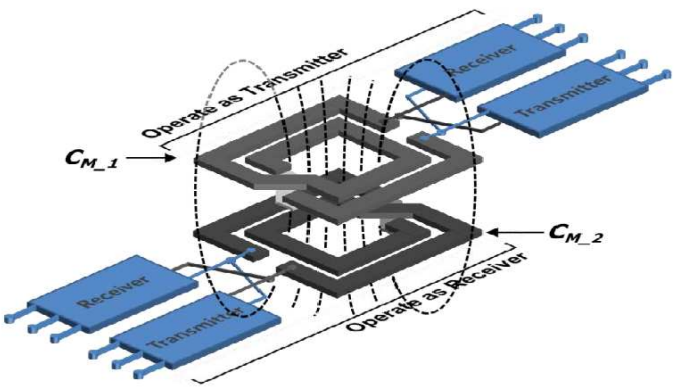

Figure 3. Proposed coil — merged type for wireless chip-to-chip communication.

The coil is designed with a differential structure because transceivers for WCC technology are composed of differential circuit blocks in general [8–12]. For the sake of simplicity, we assume that the only the C_{M_1} carries current. The magnetic coupling ϕ_{M_1} emanating from C_{M_1} has two components; one component, ϕ_{M_11}, links only C_{M_1}, while the other one, ϕ_{M_12}, links C_{M_1} and C_{M_2}. Hence, the emanating magnetic flux can be described as follows:

$$\phi_{M\_1} = \phi_{M\_11} + \phi_{M\_12} \tag{3}$$

Among the two components of ϕ_{M_1}, ϕ_{M_12} is the desired component for WCC technology. Thus, the coupling coefficient for the designed coupling is described as

$$k_M = \phi_{M\_12}/\phi_{M\_1}. \tag{4}$$

If the numbers of turns of C_{M_1}, C_{O_T1} and C_{O_R1} equal two in each case, the following equations are satisfied:

$$\phi_{M\_1} \cong \phi_{O\_T1} \quad \text{and} \quad \phi_{M\_11} \cong \phi_{O\_T1T1} + \phi_{O\_T1R1} \tag{5}$$

$$\phi_{M\_12} \cong \phi_{O\_T1T2} + \phi_{O\_T1R2} \tag{6}$$

From Eq. (6), the following equation holds:

$$k_M = \frac{\phi_{M\_12}}{\phi_{M\_1}} \cong \frac{\phi_{O\_T1T2} + \phi_{O\_T1R2}}{\phi_{O\_T1}} \cong \frac{\phi_{O\_T1T2}}{\phi_{O\_T1}} + k_O > k_O \tag{7}$$

As shown in Eq. (7), the desired coupling coefficient of the merged type is higher than that of the overlaid type because the cross-talk phenomenon between the Tx. and Rx. coils located on the same chip is removed. Accordingly, the distance between the stacked chips which use merged coils can be increased compared to the overlaid coil case.

4. EXPERIMENTAL RESULTS

To verify the feasibility of the proposed coil structure, we performed electromagnetic (EM) simulations. In this study, we compare the overlaid and merged coil types with the maximum available gain (MAG). For a fair comparison, the outer sizes of the two coils are designed to be $80 \times 80\,\mu\text{m}^2$ in size. We designed the metal width to be $2.6\,\mu\text{m}$ and the space between the adjacent metal lines to be $0.8\,\mu\text{m}$. The distance between the chips is fixed at $50\,\mu\text{m}$. In the overlaid coil, the Rx. coil is located on the outer side with two turns and the Tx. coil is located on the inner side with two turns. The merged coil was designed in two different cases: one using two turns and the other using four turns.

Figure 4 shows the simulated MAG values for various cases. For the overlaid coil, the cross-talk component is highest compared to the

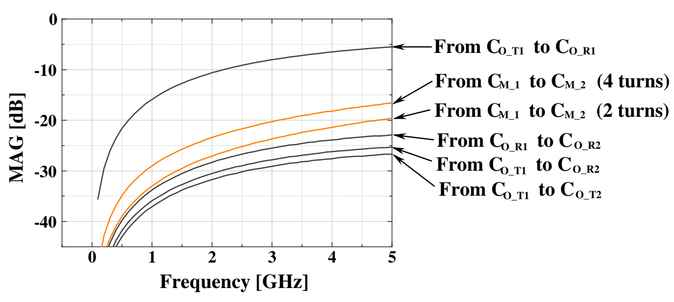

Figure 4. Simulated maximum available gains for the overlaid and merged coils.

other cases. This indicates that the undesired power transmitted from C_{O_T1} to C_{O_R1} is maximized in all cases. On the other hand, the desired power transmitted from C_{O_T1} to C_{O_R2} shows the minimum values among all cases.

For the cases with a merged coil, the desired transmitted power is approximately 5 dB lower compared to that of the overlaid cases, indicating that the distance between chips can be increased for the proposed coil as compared to the overlaid coil. Additionally, the data transmission error rate can be reduced if the merged coil design is used with WCC technology.

We fabricated a transceiver for WCC technology using the proposed coil structure to verify the feasibility of the coil. The test chip is implemented in the 50-nm digital CMOS process in which two metal layers are provided. The receiver of the test chip is composed of the first buffer, the latch, the second buffer, and the sub-sequential inverters. The latch is designed to restore the received signal, which is a pulse-type signal, to its original digital signal. The transmitter is designed using inverters with a differential structure. The impedances of the coil are matched to the transceiver circuits. Figure 5 shows the input and output voltage waveforms of the transceiver using the merged coil. The peak-to-peak voltage of the input signal and the

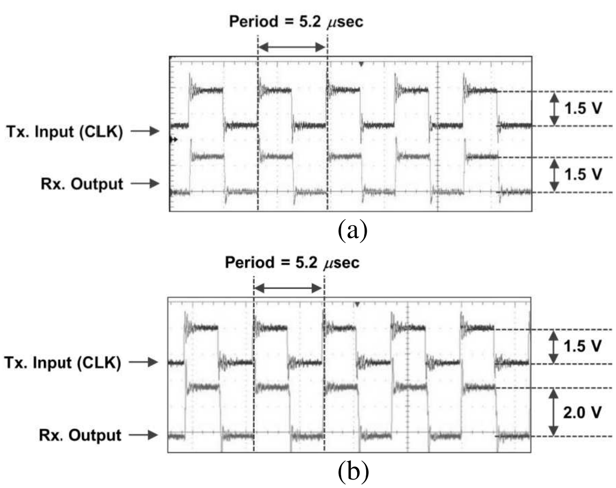

Figure 5. Measured results of wireless chip-to-chip communication technology using the proposed merged coil: (a) peak-to-peak voltage of the input signal = 1.5 V, supply voltage for the transceiver = 1.5 V. (b) Peak-to-peak voltage of the input signal = 1.5 V, supply voltage for the transceiver = 2.0 V.

supply voltage for the transceiver are 1.5 V. From the experimental results, the feasibility of the proposed coil was verified.

Figure 6 shows the input and output voltage waveforms according to the clock period. An under-damping phenomenon occurs because of the parasitic components induced by the measurement equipment.

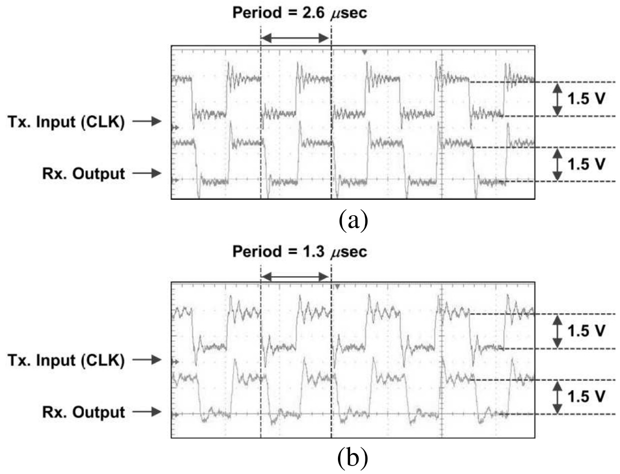

Figure 6. Measured results according to the clock period: (a) clock *period* = 2.6 μsec. (b) Clock period = 1.3 μsec.

5. DISCUSSION

5.1. Eddy Current Effects

The eddy current induced by the AC current at the coil degrades the signal power transmitted from the coil. The eddy currents for the typical and the merged types are shown in Figure 7. The eddy current effects were considered during the EM simulation. The eddy current of the merged type may be higher than that of the typical type because the magnetic flux emanating from C_{O_T1} already links C_{O_R1} in the typical type, unlike in the merged type. However, if we consider the loss including undesired magnetic couplings and eddy current effects, the overall loss of the typical type is higher than that of the merged type as shown in Figure 4.

Although the eddy current of the merged coil with four turns is higher than that of the merged coil with two turns, the desired magnetic coupling of the coil with four turns is higher than that of the coil with two turns. However the excessive turns of coil

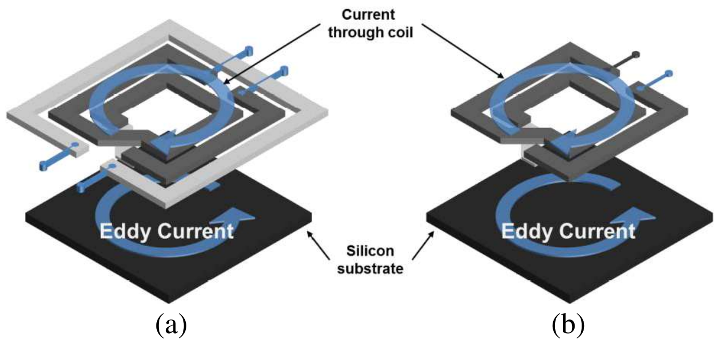

Figure 7. The eddy currents induced by the AC current at the coil of (a) the typical type and (b) the merged type.

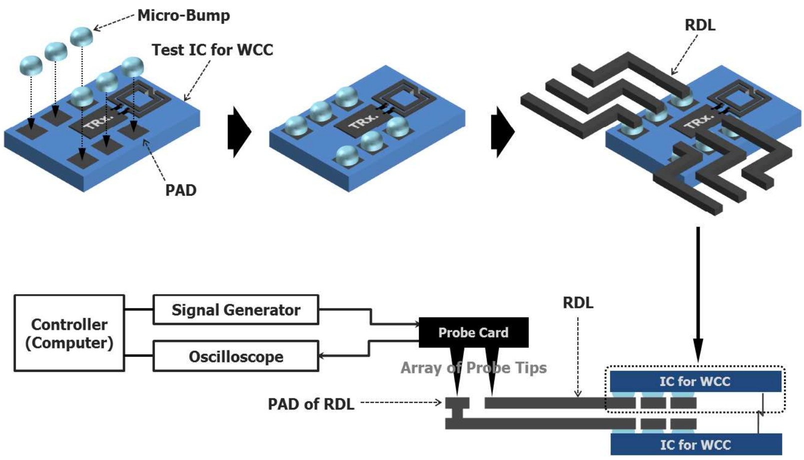

Figure 8. Conceptual diagram of the measurement setup.

may degrade the desired magnetic coupling because of the parasitic resistance induced by the metal lines of the coil and the eddy current.

5.2. Measurement Setup

Figure 8 shows the simplified measurement setup for the designed test-IC. For the measurement, micro-bumps and re-distribution layer (RDL) are used. A signal generator is used to generate the Tx. input signal. The received signal is detected using an oscilloscope. As the measurement setup uses many long RDL, signal cables, and complicate probe card, as shown in Figure 8, the parasitic inductances and capacitances of the measurement setup limit the speed of the measurement signal. Although the speed limit of the designed transceiver could not be measured due to the parasitic components of our measurement setup, we obtained simulation result showing that the system works successfully with a clock period of one nanosecond.

In this work, the target of the distance between the coils is fixed at 50 μm. Although the distance between coils is required to be minimized to maximize the magnetic coupling between the coils, the space between coils is required for the epoxy and micro-bumps to attach the stacked chips, as shown in Figure 8.

6. CONCLUSION

In this work, we proposed a type of merged coil for wireless chip-to-chip communication (WCC) technology as the next generation of 3D semiconductor technology. Additionally, the feasibility of the coil was demonstrated by comparisons with the typical coil that are currently used with WCC technology. To verify the feasibility of the proposed coil, an EM simulation and a MAG simulation were performed. The experimental results also indicated the feasibility of the proposed coil structure.

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