A BROADBAND HIGH LINEARITY CURRENT-REUSE BULK-CONTROLLED MIXER FOR 4G APPLICATIONS

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Abstract—A high linearity down-conversion mixer for the application of the fourth generation (4G) mobile communication systems is presented. The presented 2.3 to 5.8 GHz broadband mixer adopts current-reused and bulk-controlled techniques. The linearized transconductor stage is composed of the CMOS amplifiers and the bulk-controlled compensation (BCC) transistors. The bulk-controlled voltage is applied to adjust the threshold voltage of the BCC transistor. Thus, the equivalent third-order intermodulation (IM3) term of the CMOS amplifiers and the BCC transistors can be mitigated so as to improve the linearity. Furthermore, the current-reused architecture enhances the conversion gain of the proposed mixer and compensates the loss caused by the shunt feedback matching network. The presented mixer consumes 4.8 mA from a 1.5 V power supply. The measurement results of the mixer exhibit the maximum power conversion gain of 11.3 dB. The input third-order intercept point (IIP3) of 4.7 dBm over the entire 2.3–5.8 GHz band is observed.

Received 7 February 2013, Accepted 20 March 2013, Scheduled 26 March 2013

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1. INTRODUCTION

The requirements for the modern mobile internet access in the fourth generation (4G) communication systems has grown recently. There are several proposals for the 4G standards, such as Worldwide Interoperability for Microwave Access (WiMAX) and Long Term Evolution (LTE) systems [1]. In the physical layer design, WiMAX adopts orthogonal frequency division multiplexing (OFDM) access technique for the uplink and the downlink. The downlink of LTE still specified by the OFDM technique. However, the uplink of LTE is depicted in the discrete Fourier transform spread orthogonal frequency-division multiplexing (DFTS-OFDM) technique. The frequency bands from 2.3 GHz to 5.8 GHz are occupied by these applications to provide the 4G service of data transmission including voice, video, and internet.

For wireless system, receivers and transmitters are the front-end parts responsible for receiving and/or transmitting signals. Antennas, low noise amplifiers (LNAs), mixers, filters, voltage controlled oscillators (VCOs), and power amplifiers (PAs) are the main radio frequency (RF) circuits of the transceiver design [2–6]. Mixers in receivers are responsible for down converting the incoming RF signals to intermediate frequency (IF) signals. The linearity of the mixer dominates the overall linearity of the receiver in the RF front-end design. The nonlinearity is induced by the IM3 effect which can not be suppressed by RF filters [7–9]. Up to now, there have been lots of methods proposed to enhance the linearity of the mixer due to the nonlinear of the transconductor stage. The CMOS q_m cell composed of the tanh functions was adopted to suppress IM3 phenomenon and thus improve IIP3 [10]. A charge-injection method utilized current injecting into the drain of the transistors in the transconductor stage [11]. The current of the transconductor stage is increased so as to improve the conversion gain and IIP3 of the mixer. The passive devices connected to the sources of the transconductor stage as source-degeneration was commonly revealed [12]. Owing to the negative feedback mechanism, trade-offs between the linearity and conversion gain are considered.

In this paper, a broadband mixer using both current-reused and bulk-controlled techniques is proposed. Section 2 of this paper describes the linearity analysis of a Gilbert-cell mixer as well as the proposed mixer. Section 3 presents the measurement results of the mixer. Finally, conclusions in Section 4 are summarized.

2. DESIGN METHODOLOGY OF MIXERS

2.1. Linearity Analysis of the Gilbert Cell Mixer

The Gilbert-cell mixer for the modern receiver design is illustrated in Figure 1 [13]. The Gilbert cell mixer consists of a class-A transconductor stage, a current commutating stage, and a load stage. M_1 and M_2 are the class-A transconductor stage which affects the conversion gain and the linearity of the mixer. The current commutating stage composed of M_3-M_6 provides small signal current switching according to the high local oscillator (LO) power. The load stage consisted of R_1 and R_2 provides the conversion gain and the voltage headroom. In general, the CMOS Gilbert-cell mixer reveals high conversion gain and appropriate isolation but poor linearity. The nonlinearity is based on the *I-V* characteristics of MOSFETs which operated in the saturation region. The relationship between the input differential voltage (v_{RF}) and the drain current (i_{DS}) of a transconductor stage is depicted as follows:

$$i_{DS} = I_{ds} + g_m v_{RF} + \frac{g'_m}{2!} v_{RF}^2 + \frac{g''_m}{3!} v_{RF}^3 + \frac{g'''_m}{4!} v_{RF}^4 + \dots, \qquad (1)$$



Figure 1. Schematic of the Gilbert cell mixer.

where g_m is the transconductance of the MOSFET and dominates the gain performance. g'_m represents the second-order intermodulation (IM2) phenomenon. g''_m denotes the IM3 phenomenon. I_{ds} denotes DC current. From (1), the IM3 phenomenon can be mitigated by reducing g''_m . Figure 2 illustrates the relationship between g_m and v_{RF} in the class-A transconductor stage. The transconductor stage provides a constant g_m response with an input range of $\pm 15 \text{ mV}$. Figure 3 shows the g''_m characteristic. The nonzero g''_m will deteriorate the i_{DS} so as to degrade the linearity of the transconductor stage. The negative peak of g''_m can be neutralized by adopting multiple gated transistors. Nevertheless, the techniques still suffer from the additional noise source and power consumption [14]. Moreover, the additional bias resistors and multiple gate transistors also increase the overall chip area.



 $\begin{array}{c} 3 \\ 2 \\ -1 \\ -2 \\ -0.6 \\ -0.4 \\ -0.2 \\ -0.6 \\ -0.4 \\ -0.2 \\ -0.6 \\ -0.4 \\ -0.2 \\ 0.0 \\ 0.2 \\ 0.4 \\ 0.6 \\ 0.4 \\ 0$

Figure 2. g_m characteristic of the Gilbert cell mixer.

Figure 3. g''_m phenomenon of the Gilbert cell mixer.

2.2. Current-reuse Bulk-controlled Mixer

Figure 4 illustrates the compensation technique of a multiple gated transistors. The transconductance linearization by using such a compensation method is depicted in [15]. M_1 is the main transistor and M_2 denotes the compensated transistor. V_{GS1} and V_{GS2} represent the gate-source voltage of M_1 and M_2 , respectively. While $V_{GS2} =$ $V_{GS1} - \Delta V$, the IM3 term of M_1 is compensated by the shift of the IM3 term of M_2 . Thus, the IM3 of the overall transconductor which composed of M_1 and M_2 in the appropriate bias region is near zero. The linearity of the transconductor can therefore be improved. Nevertheless, this architecture also leads to more power consumption due to the additional current path. The multiple gated transistors compensation also suffers from more passive devices for the compensated transistor. To adjust the threshold voltage (V_{th}) of the



Figure 4. Schematic of the multiple gated transistors compensation.

compensated transistor was proposed to be a modified compensation method [16]. But the negative bulk-source voltage will complicate the bias circuit design and the power plan.

Due to the proposed circuit is based on the BSIM3v3 MOS Models, the V_{th} model of the non-uniform substrate doping profile is as follows:

$$V_{th} = V_{Tideal} + K_1 \left(\sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s} \right) - K_2 V_{bs}, \tag{2}$$

where

$$K_1 = \gamma_2 - 2K_2 \sqrt{\Phi_s - V_{bm}} \tag{3}$$

$$K_2 = \frac{(\gamma_1 - \gamma_2) \left(\sqrt{\Phi_s - V_{bx} - \sqrt{\Phi_s}}\right)}{2\sqrt{\Phi_s} \left(\sqrt{\Phi_s - V_{bm}} - \sqrt{\Phi_s}\right) + V_{bm}}.$$
(4)

From (2) and (4), V_{Tideal} is the threshold voltage of the long channel device at zero substrate bias, Φ_s denotes the surface potential, γ_1 and γ_2 are body bias coefficients, and V_{bm} represents the maximum substrate bias voltage [17]. The variation of the V_{bs} will cause the variation of V_{th} .

Figure 5 shows the proposed current-reused bulk-controlled high linearity mixer. M_1 and M_3 , M_2 and M_6 denote the CMOS amplifiers. M_4 and M_5 are the IM3 compensation transistors with the adjustable bulk voltage (VB_{CON}). The adjustable bulk voltage is different from [16]. The PMOS architecture avoids the negative bias voltage requirement. M_3-M_6 also exhibit the current-reused characteristic which improve the conversion gain of the mixer. L_1-L_4 , C_1-C_4 , and



Figure 5. Schematic of the current-reuse bulk-controlled mixer.

 R_1-R_4 are the wideband input matching network of RF and LO ports. Due to the feedback matching network of the RF port, the RF port does not require the external bias voltage. VB_{LO} denotes the bias voltage of the LO port. The commutating stage which consists of M_{7-} M_{10} acts as ideal switches when the input LO power is large. The DC operation point and the aspect ratio of the commutating stage will influence the requirement of the driven power for switches. Lower driven powers make M_7-M_{10} act as ideal switches. The transistors are biased in the saturation region close to the triode region. The operation makes M_7-M_{10} to be turned off easily and the RF signal is down-converted by the LO signal. The load stage consisted of R_5 , R_6, M_{11} , and M_{12} provides signal conversion from current signals to voltage signals. The load stage can provide output impedance via the resistive load of R_5 and R_6 , and appropriate voltage swing headroom by the transistors M_{11} and M_{12} . The impedance of the source follower stages, M_{13} , M_{14} , R_7 , and R_8 , are specified to 50 Ω for measurement purpose. The dimensions and values of the devices are summarized in Table 1. Figure 6 illustrates the g_m phenomenon of the proposed mixer. The mixer demonstrates a g_m range of $\pm 200 \,\mathrm{mV}$ more than the





Figure 6. g_m characteristic of the current-reuse bulk-controlled mixer.

Figure 7. g''_m phenomenon of the current-reuse bulk-controlled mixer.

Device Name	Dimension/Value			
$M_1 - M_2$	$90\mu\mathrm{m}/0.35\mu\mathrm{m}$			
$M_3 - M_6$	$48\mu\mathrm{m}/0.35\mu\mathrm{m}$			
$M_7 - M_{10}$	$112\mu{ m m}/0.18\mu{ m m}$			
$M_{11}-M_{12}$	$192\mu{ m m}/0.18\mu{ m m}$			
$M_{13}-M_{14}$	$192\mu{ m m}/0.18\mu{ m m}$			
$R_1 - R_4$	71Ω			
$R_{5}-R_{6}$	$15.1\mathrm{k}\Omega$			
$R_7 - R_8$	572Ω			
$C_1 - C_2$	$3.8\mathrm{pF}$			
C_3-C_4	$2.7\mathrm{pF}$			
L_1-L_4	$3.9\mathrm{nH}$			

 Table 1. Device dimensions/values summary.

Gilbert-cell mixer. The characteristic of g''_m is shown in Figure 7. g''_m is zero in the interval, thus the linearity of the mixer can be improved.

In the simulation of the proposed mixer, the RF is from 2.3 GHz to 5.8 GHz and the LO frequency is from 2.29 GHz to 5.79 GHz. The IF is at a fixed frequency of 10 MHz. The proposed mixer is accomplished by Agilent ADS 2006 simulator and TSMC 0.18 μ m Mixed Signal CMOS RF model. The simulated power consumption is 7.7 mW at a 1.5 V power supply. The return loss (RL) of the RF port on Smith chart is shown in Figure 8. The points are the impedance from 2.3 GHz to 3.5 GHz. Although the RL of RF is more than $-10 \,\text{dB}$





Figure 8. RL of the RF port on Smith chart.

Figure 9. RL of the IF port on Smith chart.

from 3.6–5.8 GHz, the proposed mixer can still operate appropriately. The simulation results of the RL of the IF port on Smith chart are illustrated in Figure 9. The points denote the impedance while frequency is changing from 5 MHz to 100 MHz.

3. MEASUREMENT RESULTS

The proposed mixer were fabricated in TSMC $0.18 \,\mu\text{m}$ Mixed Signal CMOS RF technology. All passive components are implemented on-chip and including the metal-insulator-metal (MIM) capacitors. spiral inductors, and poly resistors. Measurements of the differential RF/LO/IF signals were provided by the measurement systems of the coplanar Ground-Signal-Ground-Signal-Ground (GSGSG) 100 µm pitch on-wafer probes. The differential signals of RF/LO ports were generated by using the KRYTAR 180° hybrid coupler which operated from 1 GHz to 12.4 GHz. A Mini-Circuits 180° hybrid coupler which operated from 1 MHz to 500 MHz was adopted for the differential signal of IF port. The 180° hybrid coupler provides 2-way power split and power combination. The supply and bias voltages are connected by four separate pads for probing through a conventional 7-pin Power-Ground-Power-Power-Ground-Power (PGPPGP) DC probe. The losses of the probes and cables were calibrated by the PNA 5230A network analyzer.

The RF is swept from $2.3 \,\text{GHz}$ to $5.8 \,\text{GHz}$. Because IF is fixed at 10 MHz, LO frequency is 10 MHz less than the frequency of RF signals. The active current of the mixer is about $4.8 \,\text{mA}$ from a $1.5 \,\text{V}$ supply

voltage. The measurement of the conversion gains versus different LO powers at 2.3 GHz, 3.5 GHz and 5.8 GHz are shown in Figure 10. The maximum conversion gains achieve 9.2 dB, 11.3 dB, and 9.8 dB at 2.3 GHz, 3.5 GHz, and 5.8 GHz, respectively. The LO power is set to be -10 dBm in order to optimize the mixer performance.



Figure 10. Conversion gain versus LO power.

Figure 11. IIP3 versus bulkcontrolled voltage.

A two-tone testing is adopted for the IIP3 estimation. The frequency spacing in the two-tone test is set to be 250 kHz which is the channel spacing in a 4G system. The frequencies of the down-converted IF signals are 9.875 MHz and 10.125 MHz, and the frequencies of the IM3 distortions are 9.625 MHz and 10.375 MHz, respectively. The IIP3 of the current-reused bulk-controlled mixer is compensated by the bulkcontrolled voltage. The relationship between the IIP3 and the bulkcontrolled voltage is demonstrated in Figure 11. The squares are the simulated IIP3 and the circles denote the measured IIP3. Owing to the device mismatch and the process variation, the maximum measured IIP3 achieves $4.7 \,\mathrm{dBm}$ when $\mathrm{VB}_{\mathrm{CON}}$ is equal to $0.9 \,\mathrm{V}$. Figure 12 illustrates the measured IIP3 versus RF. The maximum measured IIP3 achieves 4.7 dBm at 2.3 GHz and the minimum measured IIP3 is $-2.6 \,\mathrm{dBm}$ at 3.5 GHz. The noise figure (NF) versus RF measurement is shown in Figure 13. The minimum NF is 12.8 dB at 4 GHz and the maximum NF is 16 dB at 5.8 GHz. Figure 14 demonstrates the LO-RF and LO-IF isolation characteristic versus LO frequency. The LO-RF isolation is better than 66.4 dB, and the LO-IF isolation is higher than 58.7 dB from 2.3 to 5.8 GHz. Figure 15 represents the RF-IF isolation characteristic versus LO frequency. The maximum RF-IF isolation is 69.5 dB at 4.8 GHz and the minimum RF-IF isolation achieves 54 dB at 2.8 GHz. Figure 16 shows the chip micrograph of the mixer. All passive components are implemented on-chip. The symmetrical placement and



Figure 12. IIP3 versus frequency.



Figure 13. NF versus frequency.



Figure 14. LO-RF and LO-IF isolation characteristic.

Figure 15. RF-IF isolation characteristic.

routing can reduce the magnitude mismatch and phase mismatch of the differential signals. The chip micrograph occupies a compact area of $1.27 \times 1.18 \text{ mm}^2$.

A figure of merit (FoM) demonstrates a value from the overall parameters of a mixer for performance comparison. FoM is represented as [18]

$$FoM = 20\log(f_{RF}) + CG - NF + IIP3 - 10\log(P_c).$$
 (5)

where f_{RF} is the frequency of RF signals in Hz. *CG* denotes the conversion gain in dB. *NF* represents the single-sideband (SSB) NF in dB. *IIP3* is the input third order intercept point in dBm. P_c denotes the total power consumption in Watts. The comparison between the measurement results of the proposed high linearity mixer and other mixers are summarized in Table 2. The proposed mixer exhibits excellent properties of the linearity, conversion gain, and the isolation.



Figure 16. Photograph of the current-reuse bulk-controlled mixer.

 Table 2. Performance summary of the high linearity mixers.

Ref.	[19]	[20]	[21]	This work
Process (µm)	0.18	0.18	0.18	0.18
Supply Voltage (V)	1.8	1.8	0.8	1.5
Power Consumption (mW)	0.94	18	10	7.2
RF (GHz)	5.25	2.4	5.801	$2.3\sim 5.8$
Conversion Gain (dB)	8.5	-5.5	-1.6	$3.5 \sim 11.3$
IIP3 (dBm)	-8.42	9.2	3	$-2.6 \sim 4.7$
LO-IF Isolation (dB)	N.A.	N.A.	N.A.	$58.59 \sim 71.7$
LO-RF Isolation (dB)	N.A.	N.A.	54	$45.68 \sim 61.51$
$P_{-1\mathrm{dB}}~(\mathrm{dBm})$	-17.17	2	-3	N.A.
SSB NF (dB)	22.1	20	N.A.	$12.8 \sim 16$
FoM	202.65	188.75	N.A.	$205.86@2.3\mathrm{GHz}$
				$208.76@3.3\mathrm{GHz}$
				$208.75@5.8\mathrm{GHz}$

The mixer also reveals the superior FoM than other mixers at different frequencies.

4. CONCLUSION

A CMOS current-reused bulk-controlled mixer has been designed and fabricated in TSMC 0.18 µm Mixed Signal CMOS RF technology. The proposed mixer achieves 2.3–5.8 GHz wideband performance for WiMAX and LTE applications. The mixer is realized by adopting the linearity compensation method based on the bulk-controlled compensation transistor and CMOS transconductor. The bulkcontrolled compensation transistor and CMOS transconductor also reveals the current-reuse characteristic to improve the conversion gain. The mixer consumes 7.2 mW from a 1.5 V power supply. The overall chip size is $1.27 \times 1.18 \,\mathrm{mm^2}$. The measurement results of the proposed mixer exhibits maximum power conversion gain of 11.3 dB, IIP3 of 4.7 dBm, and single side-band noise figure of 12.8 dB. The LO-RF and LO-IF isolations are 61.5 dB and 71.7 dB, respectively. The proposed architecture which reveals high IIP3, high conversion gain, and good isolation is suitable for 4G applications.

ACKNOWLEDGMENT

The authors wish to thank the Chip Implementation Center (CIC) of the National Applied Research Laboratories, Taiwan, R.O.C., for supporting the chip implementation and measurement.

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