Progress In Electromagnetics Research M, Vol. 30, 51–66, 2013

THERMO-MECHANICAL ANALYSIS OF AN IMPROVED THERMAL THROUGH SILICON VIA (TTSV) STRUCTURE

Lin-Juan Huang* **and Wen-Sheng Zhao**

Center for Optical and Electromagnetic Research, Zhejiang Provincial Key Lab for Sensing Technologies, State Key Lab of MOI, Zhejiang University, Hangzhou 310058, China

Abstract—Temperature and thermal stress responses of an improved TTSV structure under the impact of hotspots are numerically analyzed in this paper. A Fin structure is added to the circular TTSV to strengthen the effect of thermo-mechanical mitigation. The nonlinear finite element method (N-FEM) is presented to obtain the coupled thermal and mechanical fields. Running time of the N-FEM algorithm is compared with that of commercial software to indicate its efficiency. The model of state-of-the-art 3D Dynamic Random Access Memory (DRAM) is adopted in our simulation. Besides the single-layer TTSV and TTSV array, the extended case of multi-layer TTSVs is also investigated. To take into consideration the nonlinear effects, the temperature dependent results for the issues of hotspot alignment and liner materials selection are provided, both of which are compared with the corresponding temperature independent results. This paper is aimed to provide some practical guidance to the design of TTSV for effective thermo-mechanical management.

1. INTRODUCTION

Three-dimensional integrated circuits (3-D ICs) with through silicon vias (TSVs) are well known as a promising technology to address both the "more-Moore" and "more-than-Moore" applications [1–3]. They offer the heterogeneous integration, shorter interconnect length, lower power consumption and so on. However, the ensuing thermal issues and the corresponding thermo-mechanical problems have posed threat to further development of 3-D ICs [4, 5].

Received 22 January 2013, Accepted 13 March 2013, Scheduled 21 March 2013

* Corresponding author: Lin-Juan Huang (huanglinjuan1987@gmail.com).

Thermal management is becoming an indispensable process for 3-D IC design. The reasons are: 1) reduced heat dissipation due to die thinning, 2) the poorly thermally conductive adhesives, 3) higher power density [6–8], 4) inadequate space for cooling channels (i.e., gap for fluid flow), and 5) hotspots possibly occurred in stacked dies, especially for hotspot alignment. One approach to increase heat dissipation is to insert thermal through silicon via (TTSV) [9], which is mainly aimed to suppress the peak temperature by introducing heat path from hotspots to the bottom heat sink. A couple of academic works have focused on TTSV improvement for efficient heat dissipation. In [10], thermal via allocation was studied to mitigate the temperature hotspots of each die, in the process of placement and routing, respectively. Singh et al. [9] simulated the effects of TTSV dimensions and its extension length into silicon substrate on temperature reduction. Further, the author suggested that graphene at the interface between die and ILD layer can help to boost the ability of TTSV to spread heat. Hwang et al. proposed a thermal-aware physical design of TTSV (with Fin structure) in order to solve localized hotspot problems [11], with its thermal resistance circuit model developed for time-efficient calculation. However, the author considered only one device layer, and investigation of three or even more dies [12] including bottom substrate in the package level was not given. Moreover, the nonlinear temperature dependent physical properties, such as thermal conductivity and heat capacity, are not taken into account in [11]. Last but not least, this paper lacks the part of studying thermal induced stress of the improved TTSV structure, which is important for the reliability and performance of 3-D ICs.

Coefficient of thermal expansion (CTE) mismatch between the TSV materials and silicon substrate in the manufacturing process may cause high thermal stresses [13]. These tensile or compressive stresses can lead to crack, delamination and even failure of materials. Numerous studies have been carried out to better understand the thermo-mechanical mechanism of TSVs. The relevant aspects of thermal stress of TSV include: 1) TSV array format, for example, an approach for designing TSV arrays based on thermo-mechanical analysis was proposed in [14], 2) hotspot distribution, and 3) the optimization of TSV geometry, dimension and material properties for the concern of thermal stress-induced crack or delamination. The nonlinear thermal stress of TSVs and some TSV-based components are analyzed [15, 16]. However, these works are mainly based on commercial finite element analysis (FEA) software, and further improvements are still required for thermo-mechanical analysis of TSVs.

In this paper, based on the nonlinear finite element method (N-FEM) [17–20], the 3D temperature and thermal stress distribution of TTSV with Fin structure are captured for thermo-mechanical-aware design. Moreover, the temperature-dependent material properties and three-layer 3D DRAM case are also considered [21]. The rest of paper is organized as follows. In Section 2, a general description of N-FEM is given. In Section 3, single- and three-layer structures with improved TTSVs are investigated, with the 3-D temperature distribution provided to figure out the heat dissipation effects. Further, thermal stress analysis of TSV with and without Fin structure is carried out in Section 4. Finally, some conclusions are drawn in Section 5.

2. NUMERICAL METHODOLOGY

Thermal and mechanical fields are coupled with each other in 3D ICs: thermal stress is caused by the temperature variation and the mechanical properties of materials are temperature dependent; thermal stress can cause deformation to the structure, which affects the temperature distribution. To obtain the temperature and thermal stress distribution of the improved TTSVs, the heat conduction and thermal stress equations should be solved numerically.

2.1. Heat Conduction Equation

The heat conduction equation is described as [18]

$$\begin{cases} \nabla\left[\kappa(T)\nabla T(\vec{r})\right] = f_1(\vec{r}, T) \\ T|_{\Gamma_a} = T_a, \quad \left.\dfrac{\partial T}{\partial n}\right|_{\Gamma_q} = -h(T - T_a)|_{\Gamma_q} \end{cases} \tag{1}$$

where $T(r)$ represents the 3-D temperature distribution, $f_1(r, T)$ the heat generation rate of the heat source, h the convection coefficient (in watts per square meter Kelvin), T_a the ambient temperature, Γ_a the Dirichlet boundary, Γ_q the Neumann boundary, and $\partial/\partial n$ the normal derivative operator along the outward direction of Γ_q. In (1), $f_1(r, T)$ is the Joule heat of TSV produced by electrical field, which is zero for TTSV.

2.2. Thermal Stress Equation

The thermal stress equation is given by [20]

$$\begin{cases} \rho\dfrac{\partial^2\mathbf{u}}{\partial t^2}+\mu\dfrac{\partial\mathbf{u}}{\partial t}+\mathbf{A}\boldsymbol{\sigma}+\mathbf{f}=0 \\ \boldsymbol{\varepsilon}=\mathbf{L}\mathbf{u} \\ \boldsymbol{\sigma}=\mathbf{D}\left(\boldsymbol{\varepsilon}-\boldsymbol{\varepsilon}^{\mathbf{Th}}\right) \\ \boldsymbol{\varepsilon}^{\mathbf{Th}}=\alpha\left(T\right)\Delta T\left[\begin{array}{cccccc}1 & 1 & 1 & 0 & 0 & 0\end{array}\right]^T \\ \sigma_{ij}n_j|_{\Gamma_\sigma}=\bar{T}_i \\ a_i|_{\Gamma_u}=\bar{a}_i \end{cases} \tag{2}$$

where μ is the thermal stress damping coefficient, $\alpha(T)$ the temperature dependent thermal expansion coefficient, ΔT the change of temperature distribution, $\boldsymbol{\varepsilon}^{\mathbf{Th}}$ the thermal strain component, $\mathbf{u}$ the displacement vector, and $\mathbf{D}$ the elasticity matrix [16]. Γ_σ and Γ_u are Dirichlet boundaries of stress and displacement, respectively, $\mathbf{A}$ and $\mathbf{L}$ the differential operators, $\boldsymbol{\varepsilon}$ and $\boldsymbol{\sigma}$ the strain and stress vectors. The stress equation can be discretized using Galerkin's method,

$$\mathbf{M}_F\frac{\partial^2\mathbf{a}\left(\mathbf{r},t\right)}{\partial t^2}+\mathbf{H}_F\frac{\partial\mathbf{a}\left(\mathbf{r},t\right)}{\partial t}+\mathbf{K}_F\mathbf{a}\left(\mathbf{r},t\right)=\mathbf{Q}_F\left(\mathbf{r},t\right) \tag{3}$$

where $\mathbf{a}(\mathbf{r},\ t)$ is the displacement of all nodes in the model, $\partial\mathbf{a}(\mathbf{r},\ t)/\partial t$ the nodal velocity, and $\partial^2\mathbf{a}(\mathbf{r},\ t)/\partial t^2$ the nodal acceleration. $\mathbf{M}_F$, $\mathbf{H}_F$, $\mathbf{K}_F$, and $\mathbf{Q}_F(\mathbf{r},\ t)$ are the mass matrix, the damping matrix, the stiffness matrix, and the load vector subject to the power of injected pulse, respectively. The global matrices can be written as

$$\mathbf{M}_F\left(T\right)=\sum_{e=1}^{N_{ele}}\mathbf{m}_F^e\left(T\right) \tag{4a}$$

$$\mathbf{H}_F\left(T\right)=\sum_{e=1}^{N_{ele}}\mathbf{h}_F^e\left(T\right) \tag{4b}$$

$$\mathbf{K}_F\left(T\right)=\sum_{e=1}^{N_{ele}}\mathbf{k}_F^e\left(T\right) \tag{4c}$$

$$\mathbf{Q}_F\left(T,t\right)=\sum_{e=1}^{N_{ele}}\mathbf{q}_F^e\left(T,t\right) \tag{4d}$$

where N_{ele} is the number of total elements, and the elements can be written as

$$\mathbf{m}_F^e = \int_{V^{(e)}} \rho \mathbf{N}^T \mathbf{N} dV \tag{5a}$$

$$\mathbf{h}_F^e = \int_{V^{(e)}} \mu \mathbf{N}^T \mathbf{N} dV \tag{5b}$$

$$\mathbf{k}_F^e(T) = \int_{V^{(e)}} \mathbf{B}^T \mathbf{D}(T) \mathbf{B} dV \tag{5c}$$

$$\mathbf{q}_F^e(t) = \int_{V^{(e)}} \left[\mathbf{B}^T \mathbf{D}(T) \boldsymbol{\varepsilon}^{\mathbf{Th}} + \mathbf{N}^T \mathbf{f}(T,t) \right] dV - \int_{\Gamma_\sigma^e} \mathbf{N}^T \bar{T} d\Gamma \tag{5d}$$

where $V^{(e)}$ is the volume of the eth element, $\mathbf{B} = \mathbf{LN}$ the strain matrix, $\mathbf{N} = [N_1 \quad N_2 \ldots N_{nod}]^T$ the vector of element-shape function, and N_{nod} the number of discrete nodes in every element. Note that for heat conduction equation, $\mathbf{M}$ equals to zero and (3) can be simplified. By finite difference approach, (3) can be written as matrix equation $\mathbf{Ax} = \mathbf{b}$, i.e.,

$$\mathbf{A} = \frac{1}{\theta \Delta t_i} \mathbf{M} + \mathbf{H} + \theta \Delta t_i \mathbf{K} \tag{6a}$$

$$\mathbf{x} = \mathbf{a}_i \tag{6b}$$

$$\mathbf{b} = \left[\frac{1}{\theta \Delta t_i} \mathbf{M} + \mathbf{H} - (1-\theta) \Delta t_i \mathbf{K} \right] \mathbf{a}_{i-1} + (1-\theta) \Delta t_i \mathbf{Q}_{i-1} + \theta \Delta t_i \mathbf{Q}_i + \frac{1}{\theta} \mathbf{M} \frac{\partial \mathbf{a}_{i-1}}{\partial t} \tag{6c}$$

where $\theta = 0.5$ is chosen to achieve the second-order accuracy and the unconditional stability, and the matrix $\mathbf{A}$ is symmetric and positive-definite.

FEM has a high computing precision. However, it can also be time-consuming. Both our N-FEM code and commercial FEM software ANSYS are run for the case of single-layer TTSVs with Fin mentioned below. The running time of our code is 2 min 20 sec, while ANSYS takes 17 min 44 sec to finish the calculation. It indicates that our code is more efficiency than commercial software.

3. MODEL DESCRIPTION AND THERMAL NUMERICAL RESULTS

Due to the reduced lateral cooling capability of thinned die and poor thermal conductivity of adhesives in the vertical integration, more confined and hotter hotspots may be produced. Fig. 1 shows the

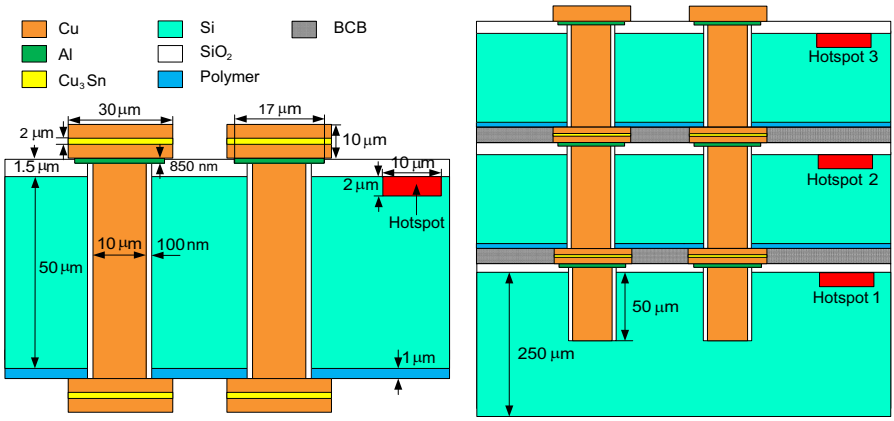

Figure 1. Cross-sectional view of single- and three-layer TTSVs in 3D integrated DRAM.

Table 1. Temperature-dependent material properties in our model.

$\sum_{n=0}^{4} c_n T^n$	Cu [19]				Polymer [23]			Al [16, 22]			Cu_3Sn [23]
	$\sigma(T)$	$\kappa(T)$	$E(T)$	$\alpha(T)$	$\kappa(T)$	$E(T)$	$\alpha(T)$	$\alpha(T)$	$\kappa(T)$	$E(T)$	$\alpha(T)$
c_0	2.91e8	420.33	141.594	17.2597	1.368	2.29e4	266.17	-3.743	1401	1 1.3	-588.12
c_1	-1.56e6	-0.0681	-0.0184	1.44e-4	4.4e-4	-211.9	-1.56	2.14e-1	-8.84	-3e-3	6.255
c_2	3.7e3	0	0	7.03e-6	9.1e-7	0.666	2.3e-3	6.04e-4	2.23e-2	-5.4e-6	-2.41e-2
c_3	-3.935	0	0	-9.03e-9	0	-7e-4	0	7.7e-7	2.3e-5	0	4.1e-5
c_4	1.56e-3	0	0	4.85e-12	0	0	0	-3.5e-10	8.2e-9	0	-2.6e-8
Temperature Range (K)	(200, 900)	(200, 1200)	(200, 1000)	(300, 900)	(296, 473)	N/A	(290, 336)	(293, 1073)	(293, 1073)	(73, 477)	(333, 423)

$\sum_{n=0}^{4} c_n T^n$	Si [19]				SiO_2 [19]			BCB [23]		
	$\sigma(T)$	$\kappa(T)$	$E(T)$	$\alpha(T)$	$\kappa(T)$	$E(T)$	$\alpha(T)$	$\kappa(T)$	$E(T)$	$\alpha(T)$
c_0	1200	332.14	162.60	-0.8972	0.54335	68.64	0.51	8.511e-2	2.9	4.729
c_1	0	-1.078	-0.135	1.721e-2	1.05e-3	9.2e-3	0	6.97e-4	0	0.127
c_2	0	1.58e-3	2.299e-4	-2.46e-5	0	0	0	0	0	0
c_3	0	-1.09e-6	-1.874e-7	1.816e-8	0	0	0	0	0	0
c_4	0	2.81e-10	5.89e-11	-5.15e-12	0	0	0	0	0	0
Temperature Range (K)	N/A	(300, 1300)	(300, 1000)	(300, 1000)	(273, 1000)	(300, 800)	N/A	(297, 339)	N/A	(300, 900)

schematic of single-layer TTSVs and extended three-layer TTSVs [18]. Although the number of layers of state-of-the-art 3D DRAM can reach 8 or even 10, here, three-layer case is considered for simplicity. The geometrical size is given in Fig. 1. The temperature dependence of materials in our model can be described by the interpolation polynomial,

$$x(T) = \sum_{n=0}^{4} c_n T^n, \quad T_0 \leq T \leq T_1 \tag{7}$$

where c_n ($n = 0$, 1, 2, 3 and 4) are the fitting coefficients as listed in Table 1. As shown in Fig. 1, each die is subjected to a heat source with a uniform thermal power. The heat dissipated from the hotspots in 3-D IC is generated either by self-heating in active devices or interconnects. The corresponding heat sources are located at the top of Si layer or within SiO_2 layer. The temperature of bottom heat sink is set to be uniformly 300 K. Adiabatic boundary condition is applied on other surfaces.

To verify our N-FEM code, the maximum temperatures of TTSV with Fin structure are captured by our code and ANSYS, respectively. As shown in Table 2, the results can be reasonably considered consistent with each other. Top view of Fin structure added to the circular TTSV is shown in Fig. 2. Here each Fin is placed right under the Al pad.

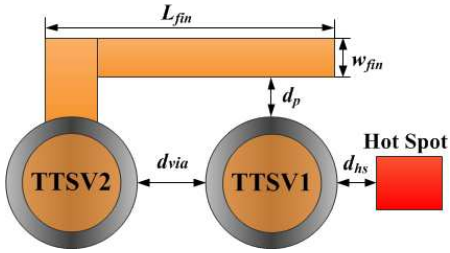

Figure 2. Top view of Fin structure ($d_{via} = 5\,\mu m$, $d_p = 5\,\mu m$, $w_{fin} = 5\,\mu m$, t_{fin} is the depth of Fin).

Table 2. Comparison between results by [11] and our code.

Number of Vias and Fin	1	3	6	6/Fin	9	9/Fin
T_{max} (K) (our code)	332.042	328.581	328.021	327.895	327.914	327.657
T_{max} (K) [11]	332.135	328.368	328.111	327.926	328.101	327.737
ΔT (K)	0.093	−0.213	0.09	0.031	0.187	0.08

Utilizing HFSS, we calculated the Noise Coupling Transfer Function of single-layer structure with and without TTSV. As shown in Fig. 3(a), the signal integrity will be affected by TTSVs, which may lead to inaccurate prediction of the IC performance. It is better to pull away TTSVs from the active devices (i.e., hotspots). Adding Fin to TTSV will not affect the signal integrity while reducing the temperature of the whole IC. Hence, we can conclude that using the Fin structure, the TTSVs can be moved farther from the heat source, as shown in Fig. 3(b).

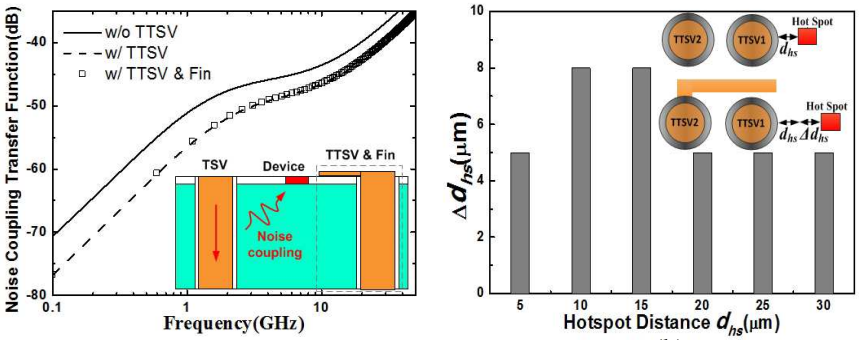

Figure 3. (a) Noise coupling transfer function of single-layer structure. (b) Compared to the case of TTSV without Fin, the distance that hotspot can be pulled away from the heat source when Fin structure is added to TTSV.

To investigate the cooling effect of Fin structure, the case of hotspots and Fin in the BEOL layer, which is located in middle of SiO_2 layer, is considered. As the TTSVs with Fin structure get closer to the hotspot, the corresponding maximum temperature of single-layer TTSVs is obtained, as shown in Fig. 4. Here, the depth of Fin structure is 8 μm, and thermal power density of the hotspot is set to $1.24 \times 10^{14}\,\mathrm{W/m^3}$. An obvious reduction in the maximum temperature can be observed after Fin is added to the TTSV. For example, the temperature is suppressed by about 20 degree when $d_{hs} = 0.5\,\mu\mathrm{m}$. Additionally, the temperature can be reduced more obviously when hotspot is closer to the Fin. Practically, with fixed hotspots encountered in 3-D IC design, Fin structure can be appropriately placed to strengthen its effect.

For the case of hotspots in active devices, to study the effect of dimension of the Fin structure, we varied Fin width from 4 μm to 6 μm and Fin thickness from 2 μm to 10 μm. Fig. 5 illustrates the corresponding peak temperature of single-layer TTSVs. As is shown, the thicker and wider the Fin, more heat in TTSV layer can be dissipated, which is due to the reduced thermal resistance R_{fin}, i.e., [11]

$$R_{fin} = \frac{1}{\kappa_{\mathrm{Cu}}} \frac{L_{fin} + d_p}{w_{fin} \cdot t_{fin}} \tag{8}$$

where L_{fin}, w_{fin}, and t_{fin} denote the length, width and depth of the Fin. d_n describes the distance between TTSV1 and Fin, and κ_{Cu} is thermal conductivity of Cu.

To further suppress the temperature, it is proposed to split single TTSV into TTSV array [24]. The schematic of single-layer TTSV

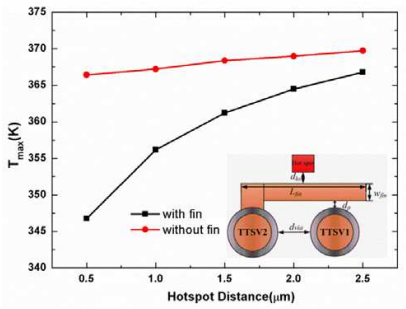

Figure 4. The maximum temperature of single-layer TTSVs varied with hotspot distance.

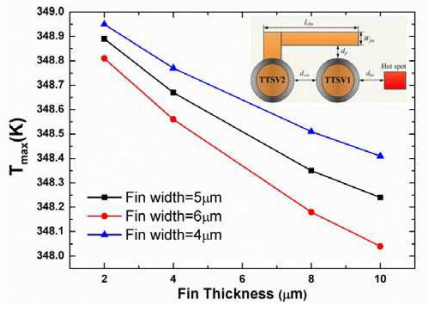

Figure 5. Maximum temperature of single-layer TTSV, with variation of Fin width and thickness.

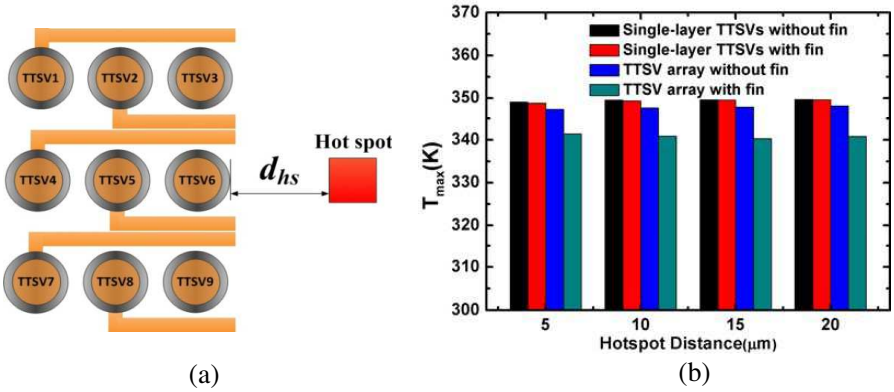

Figure 6. (a) Top view of single-layer TTSV array with fin (t_{fin} = 2.65 μm, w_{fin} = 5 μm). (b) Maximum temperature of single-layer TTSV as a function of distance between hotspot and TTSV, comparing the situation of two TTSVs and TTSV array.

array with fin is presented in Fig. 6(a). What's more, the comparison between the case of two TTSVs and TTSV array is given in Fig. 6(b). What can be inferred include: (1) the farther hotspot is away from TTSV, the hotter TTSV layer is; (2) after adding the Fin structure, the maximum temperature is reduced for both two TTSVs and TTSV array; (3) compared with the case of two TTSVs, the maximum temperature is given another reduction for TTSV array; (4) the cooling effect of Fin for TTSV array is obviously larger than that for two TTSVs.

The 3-D temperature distribution of single-layer and three-layer TTSV models are displayed in Figs. 7(a) and (b), respectively. TTSVs

are supposed to be as close as possible to the hotspot, larger than the scope of keep-out-zone (KOZ). Note that there are two main heat flow path: one through each Si layer, the other through TTSVs directly into the bottom substrate. Fig. 7(b) shows that the uppermost layer suffers the highest temperature, though each hotspot is applied with the same thermal power. This is because that the uppermost hotspot is farthest from heat sink at the bottom of the model. Moreover, as glue material, BCB has a poor thermal conductivity compared with that of Si, which roles as a heat blockage between two dies.

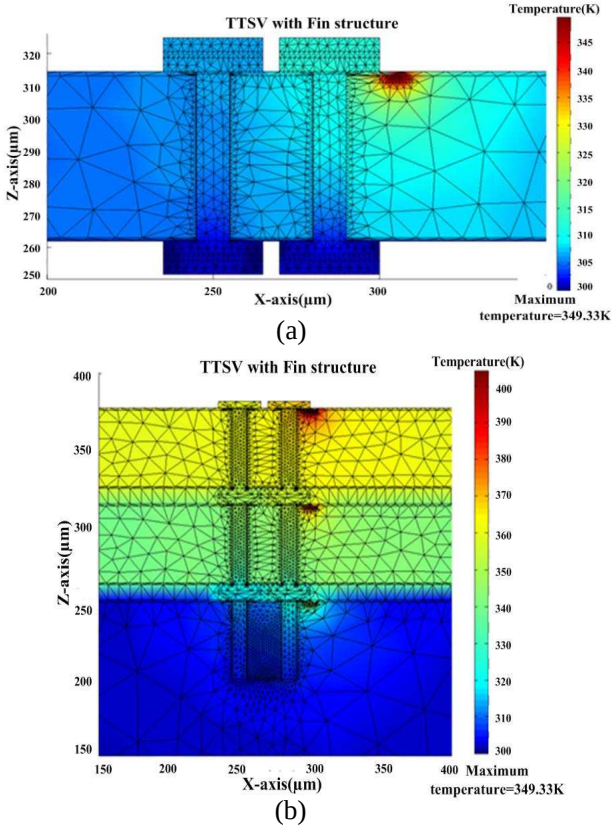

Figure 7. 3-D temperature distribution of (a) single- and (b) three-layer TTSVs. For single-layer TTSV, $w_{fin} = 6\,\mu m$ and $t_{fin} = 10\,\mu m$, $d_{hs} = 10\,\mu m$, while $t_{fin} = 2.65\,\mu m$ and $d_{hs} = 5\,\mu m$ for three-layer case.

Furthermore, we have investigated the problem of hotspot alignment, which poses a great risk on the multi-layer 3-D ICs. Here, three-layer TTSVs are modeled to study thermal coupling among heat

sources in different layers of a 3-D stack. d_{hs} of overlapped hotspots is 10 µm for each layer, while d_{hs} of staggered hotspots from top to bottom layer is 5 µm, 10 µm, 15 µm, respectively. The applied thermal power density is 0.62×10^{14} W/m^3. As shown in Fig. 8(a), the Fins help to pull down the maximum temperature for about 6 degree. Moreover, if the hotspots at each of the three layers happen to be in a straight line in the vertical or horizontal direction, they will strengthen each other in heating up the 3-D stack. And the thicker the dies, hotter the 3-D stacked layers will be. This is due to a longer heat path between hotspots and the bottom heat sink.

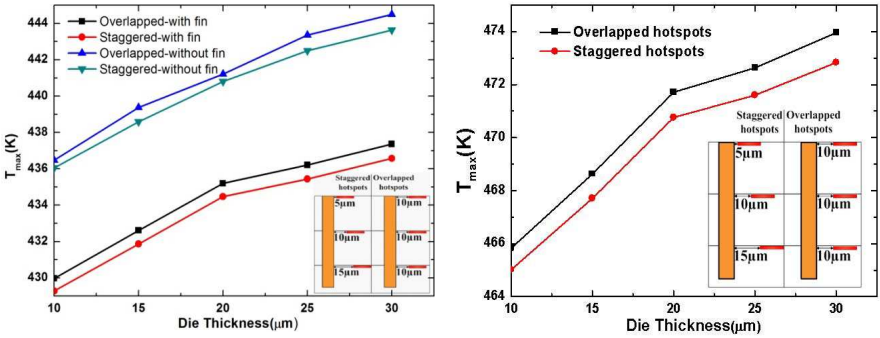

Figure 8. (a) Maximum temperature of three-layer TTSVs with overlapped and staggered hotspots. The case with and without Fin are considered. (b) Added with Fin structure, maximum temperature of three-layer TTSV with overlapped and staggered hotspots. The material properties are temperature dependent.

Utilizing the temperature dependent properties of various materials listed in Table 1, nonlinear maximum temperature of three-layer TTSVs with overlapped hotspots and staggered hotspots are also provided in Fig. 8(b). Compared to the case of linear material properties, the resulting temperature is largely increased. Consequently, for thermal-aware design of TTSV, a conservative strategy should be adopted since the unfriendly nonlinear effect.

4. THERMAL STRESS ANALYSIS

It is predicted that a large proportion of electronic failures (65%) are thermo-mechanically related. According to the von Mises force yield criterion: the von Mises force should be no more than a yielding strength, otherwise, material begins yielding. For

example, the yield strength of Cu varies from 225 MPa to 600 MPa. Therefore, it is necessary to study the thermo-mechanical effect induced by temperature field derived in Section 3. Figs. 9(a) and (b) demonstrate steady-state 3-D thermal stress distribution of single- and three-layer TTSVs, respectively. It can be observed that the thermal stresses concentrate on the interfaces of liner/Si, Cu/Al/liner, polymer/Si/liner, which is caused by the CTE mismatch of different materials. The larger the difference between CTEs, the stronger thermal stress will be. Further, temperature of the right TTSV is higher than that of the left one, according to Fig. 7. Thus the difference between the right TTSV temperature and stress free temperature (here is 27°C) is relatively larger, which means a higher thermal stress for the right TTSV. The maximum von Mises force in Fig. 9(b) exceeds 600 MPa, which indicates a great failure risk. As Fig. 9(c) shows, critical von Mises force appears at sharp corners of Fin and near the interface of Fin/TTSV. This is because that sharp corners are more likely to concentrate thermal stress, which adds the possibility of mechanical failure.

TTSV array can not only reduce the thermal concentration more efficiently, but also lower the probability of thermo-mechanical failure. TTSV array contains 9 TTSVs, so more thermal stress can be canceled out. The maximum von Mises force as a function of distance between hotspot and the nearest TTSV is displayed in Fig. 10, comparing the cases of single TTSV and TTSV array. Figs. 10(a) and (b) show the

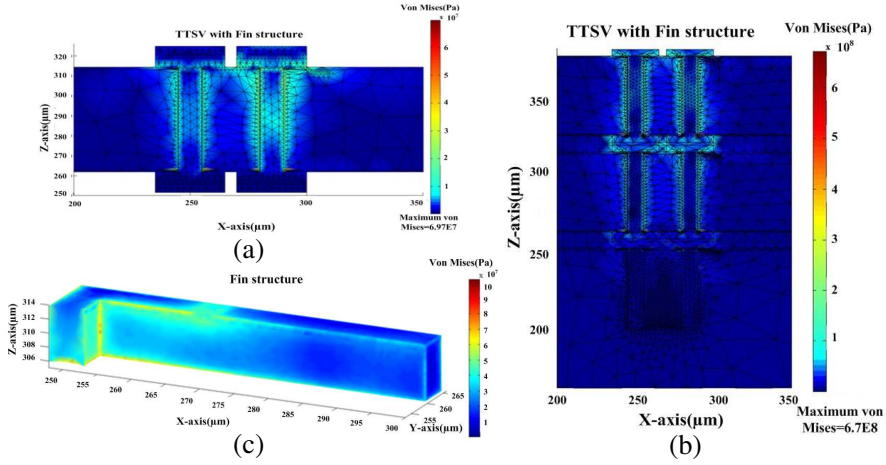

Figure 9. 3-D thermal stress distribution of (a) single- and (b) three-layer TTSVs. The geometry information and applied condition is the same as that in Fig. 7. The detailed thermal stress distribution of (c) Fin for single-layer TTSVs is provided, too.

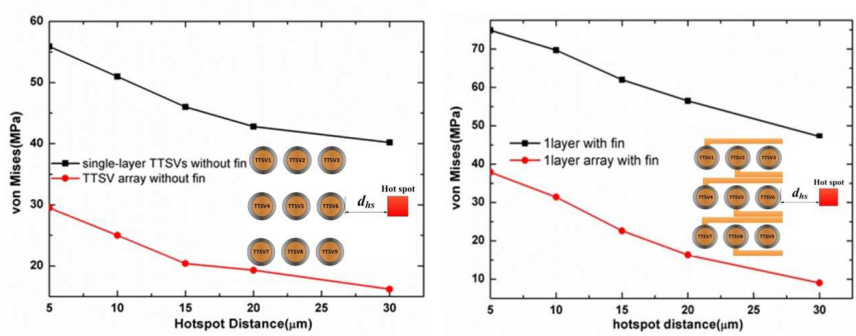

Figure 10. The maximum von Mises force of single TTSV and TTSV array (a) without and (b) with Fin.

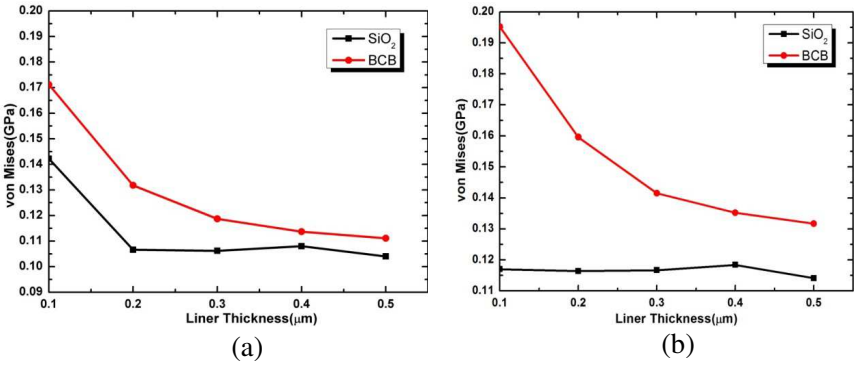

Figure 11. Maximum von Mises force of single-layer TTSV with SiO_2 and BCB liner utilizing (a) temperature-independent and (b) temperature-dependent physical parameters.

situation of TTSV without and with Fin, respectively. As can be seen, TTSV array will significantly diminish von Mises force, if not concerning about the occupied area in 3-D ICs. And when hotspot is farther away from TTSVs, von Mises force is reduced. With Fin structure, von Mises force will be increased, which is partly because of large von Mises force on the interface of Cu Fin and low-κ liner insulator.

In our Fin structure model, Fin is connected to the liner of TTSVs. By replacing SiO_2 of liner with BCB, we get the maximum thermal stress for SiO_2 and BCB depending on the thickness of liner in Fig. 11. Note that contrary to the potential thermal stress mitigation effect of BCB proposed in other papers, SiO_2 can better reduce thermal

stress actually in our models. This is because that the CTE mismatch between BCB and Si is larger than that between SiO_2 and Si. As can be observed from Figs. 11(a) and (b), the thicker liner can absorb more thermal stress. Maximum von Mises force of single-layer TTSVs with BCB liner utilizing temperature-dependent physical parameters is given in Fig. 11(b). The TTSV layer with BCB liner suffers a higher thermal stress compared with the temperature independent situation.

5. CONCLUSION

In summary, a novel Fin structure is added to TTSVs in 3-D integrated DRAM to investigate the improved thermal and thermo-mechanical performance. The models of single-layer TTSV, TTSV array and three-layer TTSVs are established. To give a practical and comprehensive study of the thermal effect of Fin on 3-D IC, we discuss the issues of hotspot location optimization, Fin size variation and hotspot alignment. The thermal and thermo-mechanical effects of TTSV array with Fin are also provided. Additionally, 3-D temperature and thermal stress distribution of single-layer and three-layer TTSV are plotted and discussed. In addition, temperature dependent results of hotspot alignment and liner materials are given. It is found that although BCB has a lower Young's module, SiO_2 can mitigate more thermal stress in our model actually. Further study may be conducted about other liner materials with better thermal and mechanical performance. All the results mentioned above are based on our N-FEM code, which deals with the problem of thermal and mechanical field coupling. This paper will offer some practical guidance of applying Fin structure to 3-D ICs to mitigate the temperature and thermal stress.

ACKNOWLEDGMENT

The authors appreciate the financial support of the State Key Lab of MOI, Zhejiang University, China and the National Natural Science Foundation of China (NSFC) under Grants 60821062, Y1100706, and 2009CB320204.

REFERENCES

1. Banerjee, K., S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and system-on-chip integration," *Proc. IEEE*, Vol. 89, No. 5, 602–633, 2001.

2. Kang, U., H.-J. Chung, et al., "8 Gb 3-D DDR3 DRAM using through-silicon-via technology," *IEEE J. Solid-State Circuits*, Vol. 45, No. 1, 111–119, 2010.
3. Zhao, W. S., W. Y. Yin, and Y. X. Guo, "Electromagnetic compatibility-oriented study on through silicon single-walled carbon nanotube bundle via (TS-SWCNTBV) arrays," *IEEE Trans. on Electromagn. Compat.*, Vol. 54, No. 1, 149–157, 2012.
4. Van der Plas, G., P. Limaye, et al., "Design issues and considerations for low-cost 3-D TSV IC technology," *IEEE J. Solid-State Circuits*, Vol. 46, No. 1, 293–306, 2011.
5. Selvanayagam, C., X. Zhang, R. Rajoo, and D. Pinjala, "Modeling stress in silicon with TSVs and its effect on mobility," *IEEE Trans. on Compon. Packag. Manufac. Technol.*, Vol. 1, No. 9, 1328–1335, 2011.
6. Wu, B. and L. Tsang, "Full-wave modeling of multiple vias using differential signaling and shared antipad in multilayered high speed vertical interconnects," *Progress In Electromagnetics Research*, Vol. 97, 129–139, 2009.
7. Chaibi, M., T. Fernandez, et al., "Nonlinear modeling of trapping and thermal effects on GaAs and GaN MESFET/HEMT devices," *Progress In Electromagnetics Research*, Vol. 124, 163–186, 2012.
8. Faiz, J., B. M. Ebrahimi, and M. B. B. Sharifian, "Time stepping finite element analysis of broken bars fault in a three-phase squirrel-cage induction motor," *Progress In Electromagnetics Research*, Vol. 68, 53–70, 2007.
9. Singh, S. G. and C. S. Tan, "Thermal mitigation using thermal through silicon via (TTSV) in 3D ICs," *Int. Microsyst. Packag. Assembly Circuits Technol. (IMPACT) Conf.*, 182–185, 2009.
10. Lee, Y.-J. and S. K. Lim, "Co-optimization and analysis of signal, power, and thermal interconnects in 3-D ICs," *IEEE Trans. on CAD of ICs and Systems*, Vol. 30, No. 11, 1635–1648, 2011.
11. Hwang, L., K. L. Lin, and M. D. F. Wong, "Thermal via structural design in three-dimensional integrated circuits," *Int. Symp. Quality Electron. Des. (ISQED)*, 103–108, 2012.
12. Thein, T. T., C. L. Law, and K. Fu, "Frequency domain dynamic thermal analysis in GaAs HBT for power amplifier application," *Progress In Electromagnetics Research*, Vol. 118, 71–87, 2011.
13. Zhang, J., M. O. Bloomfield, J. Q. Lu, R. J. Gutmann, and T. S. Cale. "Modeling thermal stresses in 3-D IC interwafer interconnects," *IEEE Trans. on Semiconductor Manufacturing*, 2006.

14. Zhang, C. B. and L. J. Li, "Characterization and design of through-silicon via arrays in three-dimensional ICs based on thermomechanical modeling," *IEEE Trans. on Electron. Devices*, Vol. 58, No. 2, 278–287, Feb. 2011.
15. Selvanayagam, C. S., J. H. Lau, et al., "Nonlinear thermal stress/strain analysis of copper filled TSV (through silicon via) and their flip-chip microbumps," *Electron. Compon. Technol. Conf. (ECTC)*, 1073–1081, 2008.
16. Wang, X. P., W. Y. Yin, and S. He, "Multiphysics characterization of transient electrothermomechanical responses of through-silicon vias applied with a periodic voltage pulse," *IEEE Trans. on Electron. Devices*, Vol. 57, No. 6, 1382–1389, 2010.
17. Bedrosian, G., "High-performance computing for finite element methods in low-frequency electro-magnetics," *Progress In Electromagnetics Research*, Vol. 7, 57–110, 1993.
18. Zhao, W. S., W. Y. Yin, X. P. Wang, and X. L. Xu, "Frequency- and temperature-dependent modeling of coaxial through-silicon via for 3-D ICs," *IEEE Trans. on Electron. Devices*, Vol. 58, No. 10, 3358–3368, 2011.
19. Shi, Y. B., W. Y. Yin, J. F. Mao, P. G. Liu, and Q. H. Liu, "Transient electrothermal analysis of multilevel interconnects in the presence of ESD pulse using the nonlinear time-domain finite element method," *IEEE Trans. on Electromagn. Compat.*, Vol. 51, No.3, 774–783, 2009.
20. Kong, F. Z., W. Y. Yin, J. F. Mao, and Q. H. Liu, "Electro-thermo-mechanical characterizations of various wire bonding interconnects illuminated by an electromagnetic pulse," *IEEE Trans. on Advanced Pack.*, Vol. 33, No. 3, 729-737, 2010.
21. Irsigler, R. and S. AG, Available online: http://www.sematech.org/meetings/archiv es/3d/8946/pres/Irsigler.pdf.
22. Nix, F. C. and D. MacNair, "The thermal expansion of pure metals: copper, gold, aluminum, nickel, and iron," *Phys. Rev.*, Vol. 60, 597–605, 1941.
23. http://www.sematech.org/meetings/archives/3d/8946/pres/Irsigler.pdf.
24. Zhao, W. S., X. P. Wang, and W. Y. Yin, "Electrothermal effects in high density through silicon via (TSV) arrays," *Progress In Electromagnetics Research*, Vol. 110, 125–145, 2010.