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A LOW POWER LOW PHASE NOISE LC VOLTAGE-CONTROLLED OSCILLATOR

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Abstract—A low phase noise CMOS complementary cross-coupled LC-tank voltage-controlled oscillator (VCO), implemented with TSMC 0.18 µm 1P6M CMOS technology, is presented. Double pair pseudo-resistance transistors biased by the tapped center of the inductor are utilized to reduce the DC bias current. The circuit consumes 1.55 mA from a 1.5 V supply voltage which saves up to 52.4% power, compared with the conventional one. Furthermore, an adaptive body biasing technique (ABB) is used to overcome the effect of PVT variations. The VCO is tunable from 2.58 to 3.07 GHz and has a phase noise −122.7 dBc/Hz at 1 MHz offset from the 3 GHz carrier. The Figure of Merit (FOM) of the proposed VCO is −188.8 dBc, and the figure of merit including the tuning range (FOM_T) is −193.5 dBc.

1. INTRODUCTION

The rapid development of wireless communication technology calls for the need of low-cost, low-power and high-performance integrated circuits. In an RF transceiver, phase noise of the local oscillator is a critical parameter for performance evaluation. The design complexities of low phase noise oscillator carry various challenges due to the conflicting requirements for achieving simultaneous low phase noise and low power [1, 2]. In addition, LC-VCO is highly sensitive to process, voltage and temperature (PVT) variations. To guarantee stable operation over the PVT variations, the VCO is typically designed for the worst case, which leads to high power consumption.

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In this paper, an improved VCO operating at 1.5 V supply voltage and 2.33 mW low power core is proposed. The adaptive body bias and double-pseudo resistances in series with the cross-coupled pairs which are biased by the tapped node of the inductor are used to reduce the power consumption and phase noise. Measured phase noise of −122.7 dBc/Hz at 1 MHz offset from 3.07 GHz is achieved. The measured tuning range is 17.3%. The rest of this paper is organized as follows. Section 2 describes the design approach of the LC-VCO which includes the topology and circuit structure used in the design. Section 3 gives the results and analysis. Comparisons with other published works are also provided in this section. Finally, a conclusion is drawn in Section 4.

2. ANALYSIS OF VCO ARCHITECTURE

In a typical LC-VCO, the cross-coupled transistor can be formed either by using all NMOS transistors, all PMOS transistors or a combination of both NMOS and PMOS transistors pairs (Fig. 1(a)). The later structure is a popular configuration employed in the VCO design since it provides higher trans-conductance at a given current, which results in faster switching and larger output amplitude [3]. In addition, it demonstrates superior rise- and fall-time symmetry resulting in less up-conversion of $1/f$ noise. Generally, the LC tank is composed of four

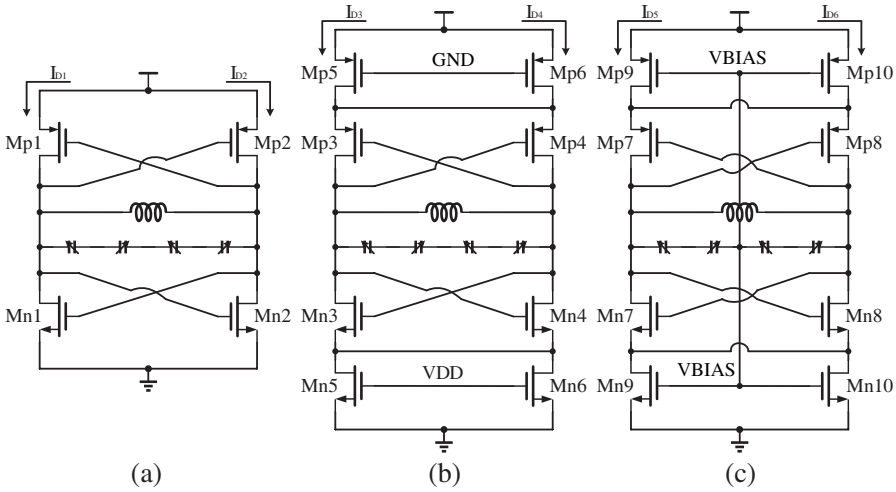

Figure 1. Schematic diagrams of VCOs: (a) Case 1: Conventional; (b) Case 2: Ref. [5]; (c) Case 3: Proposed design.

accumulation-mode MOS-varactors arranged in a back-to-back series (BBS) configuration and an inductor, which resonates at a frequency f_o. The RF modulation effect is eliminated in the BBS configuration, which minimizes the AM-to-PM noise conversion [4]. The resonant frequency, also known as the oscillation frequency of the VCO, f_o, can be calculated as: $f_o = 1\Big/\left(2\pi\sqrt{LC}\right)$. It should be noted that the capacitance consists of not only those of the varactors, but also the parasitic capacitance of the inductor, the active devices in the VCO core and the parasitic of the connection lines.

In contrast to the power consumption, bias is a key parameter in a low power VCO design. In order to simplify the schematic, we don't show the ABB technique in the figure, although it is used in all these three cases. To lessen the power consumption of the conventional complementary differential architecture, a double-pseudo-resistance is proposed in [5] and the configuration is shown in Fig. 1(b). To further reduce the power consumption, a new configuration is proposed as shown in Fig. 1(c). The difference in our design is the PMOS and NMOS pairs are biased by the tapped node $VBIAS$ from the center-tapped spiral. Therefore, the same biased voltage is applied to the double-pseudo-resistance simultaneously. When the output amplitudes are different, a voltage will be induced at $VBIAS$ and changes the gate voltages of (Mn9, Mn10) and (Mp9, Mp10) by the opposite amount. So these transistors act as variable resistors to equalize the output amplitudes; meanwhile, they decrease the power consumption. By assuming an equal supply voltage, the currents I_{D1}, I_{D3} and I_{D5} flow in the circuit (a), (b) and (c), respectively, in Fig. 1. It is easy to obtain that

$$\begin{aligned} V_{DD} = V_{SGp1} + V_{GSn1} &= I_{D3}R_5 + V_{SGp3} + V_{GSn3} + I_{D3}R_6 \\ &= I_{D5}R_9 + V_{SGp7} + V_{GSn7} + I_{D5}R_{10} \end{aligned} \quad (1)$$

where (R_5, R_6) and (R_9, R_{10}) are the equivalent resistances of case 2 and case 3, respectively. All the cross-coupled transistors work in saturation region with the same size, and the tail transistors work in triode region. For simplicity, we assume that:

$$R_{eq2} = R_5 + R_6 \propto 1/(V_{GSn5} - V_{tn}) + 1/(V_{SGp5} - |V_{tp}|) \quad (2)$$

$$R_{eq3} = R_9 + R_{10} \propto 1/(V_{GSn9} - V_{tn}) + 1/(V_{SGp9} - |V_{tp}|) \quad (3)$$

Because $V_{GSn9} \approx V_{DD}/2 = V_{GSn5}/2$, $R_{eq3} > R_{eq2}$. The drain currents are expressed as the follows:

$$I_{D1} = K_{p1}(V_{SGp1} - |V_{tp}|)^2 = K_{n1}(V_{GSn1} - V_{tn})^2 \quad (4)$$

$$I_{D3} = K_{p3}(V_{SGp3} - |V_{tp}|)^2 = K_{n3}(V_{GSn3} - V_{tn})^2 \quad (5)$$

$$I_{D5} = K_{p7}(V_{SGp7} - |V_{tp}|)^2 = K_{n7}(V_{GSn7} - V_{tn})^2 \quad (6)$$

Let $K_{p1} = K_{p3} = K_{p7} = K_p$, $K_{n1} = K_{n3} = K_{n7} = K_n$, and

$$\left(\sqrt{I_{D1}} - \sqrt{I_{D3}}\right)\left(1\Big/\sqrt{K_p} + 1\Big/\sqrt{K_n}\right) = I_{D3}R_{eq2} > 0 \quad (7)$$

$$\left(\sqrt{I_{D1}} - \sqrt{I_{D5}}\right)\left(1\Big/\sqrt{K_p} + 1\Big/\sqrt{K_n}\right) = I_{D5}R_{eq3} > 0 \quad (8)$$

$$I_{D1} > I_{D3} > I_{D5} \quad (9)$$

It is obvious that the lowest current consumption in the proposed cross-coupled oscillator is achieved. Meanwhile, this biasing method still makes the tail transistors operate at triode region. It has little impact on the source-drain voltage of tail transistors and the transconductances of the cross-coupled transistors, and so does the amplitude of the output signal. For these reasons, it gives a performance boost to the proposed VCO.

As previously mentioned, the adaptive body biasing technique (ABB) is applied in these three cases, in order to compensate the effect of PVT variations. In [6] the ABB is implemented by NMOS only, but in the proposed circuit, the ABB is implemented by both NMOS and

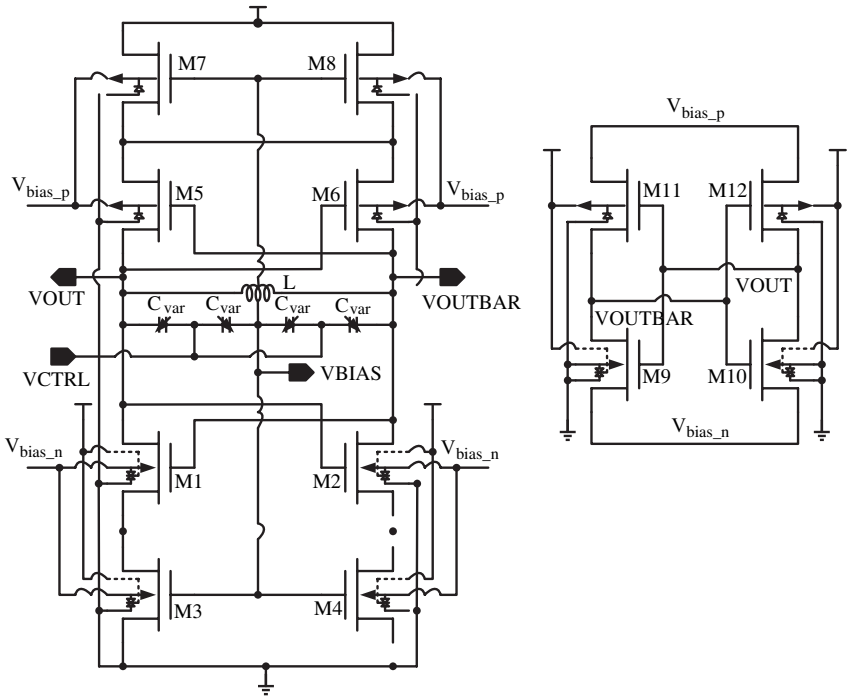

Figure 2. The detail of the proposed VCO, the right hand part shows the ABB structure.

PMOSs and the capacitor used to store the feedback voltage is replaced by the parasitic capacitors. M9 and M10 are symmetric NMOS pairs. Initially, the VCO does not oscillate. The drain and gate voltage of M9 and M10 in the ABB is initially at $V_{DD}/2$. M9 and M10 are turned on in this state, they charge the parasitic capacitors at node V_{bias_n} to slightly bigger than the minimum of the output voltage. M11 and M12 operate in the same way. They make the node V_{bias_p} to slightly less than the maximum of the output voltage as shown in Fig. 2. By setting the body bias voltages V_{bias_n} and V_{bias_p}, it reduces the threshold voltages of the core transistors. Therefore, the proposed VCO can operate at 1.5 V supply voltage.

3. PROTOTYPE DESIGN AND MEASUREMENTS

The proposed VCO has been designed and simulated by Cadence in TSMC 0.18 µm CMOS process. To evaluate the performance of the adaptive body biasing technique, the transient simulation is performed. Fig. 3 shows the increased V_{bias_n} and decreased V_{bias_p} lower the threshold voltage of the cross-coupled pairs. This feedback technique can also provide some margin for the PVT variation. With the same supply voltage, the circuit without the double-pseudo-resistance (case 1) has a current of 2.823 mA and with the same technique but biased by VDD/GND as suggested in [5] (case 2) is 2.02 mA. In contrast, the proposed basis method (case 3) has a current of 1.345 mA (simulated by Spectre, different from the measured result), which indicates a 52.4% improvement in power consumption when compared to case 1 and 33.4% compared to case 2. Thus, the proposed VCO current consumption is much lower than the other two cases. The phase noise performance of these three VCOs is shown in Fig. 4. As it

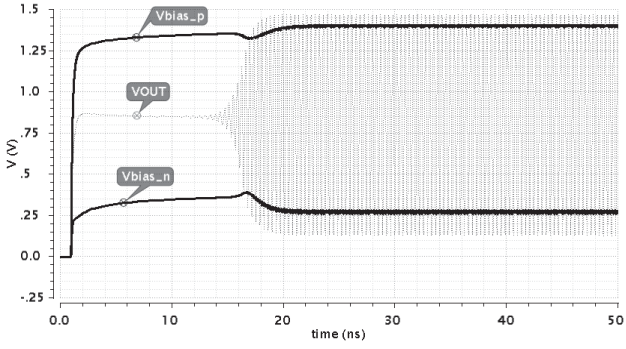

Figure 3. Simulation results of the adaptive body-biasing technique.

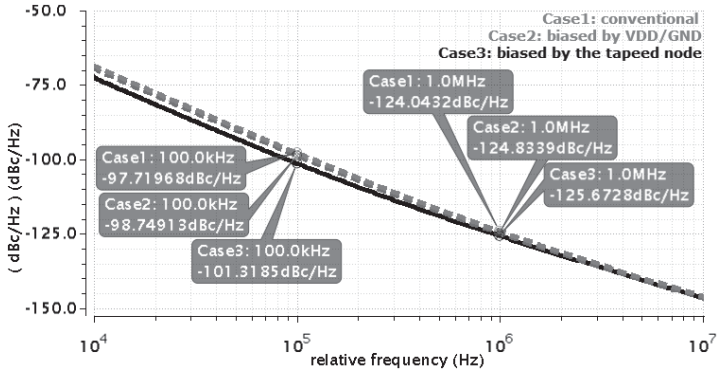

Figure 4. Phase noise of the three cases.

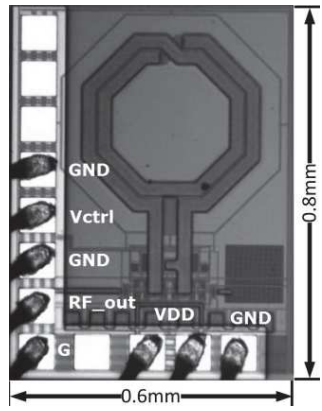

Figure 5. Microphotograph of the proposed VCO ($0.6 \times 0.8\,\mathrm{mm}^2$).

can be seen, using the center-tapped point of the tank inductor to bias the double pseudo resistances without any draw back when compared with [5].

The design was fabricated and its performances were measured. The microphotograph of the proposed LC VCO is shown in Fig. 5. The chip area including the test pads is $0.6 \times 0.8\,\mathrm{mm}^2$. The buffer structure of the VCO use an open drain NMOS, which size is half of the cross coupled NMOS pair. Then in the test board, we design an bias-T to achieve 50 ohm. The tuning range of the VCO is from 2.58 to 3.07 GHz while the tuning voltage is from 0 to 1.5 V as shown in Fig. 6. The measured power consumption is 2.33 mW and the phase noise is -122.7 dBc/Hz@1 MHz as shown in Fig. 7. The output power variation is from 1.32 dBm to 4.93 dBm and the phase noise variation is from -119.51 to -123.78 dBc/Hz@1 MHz as the control voltage was tuned

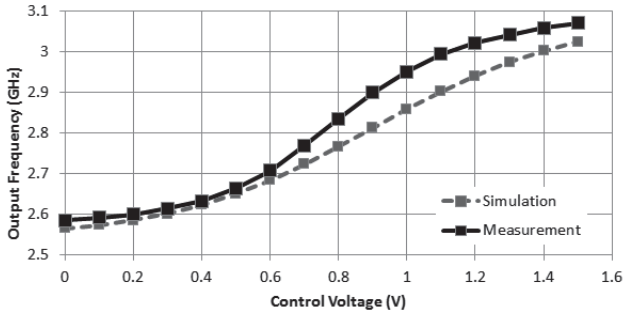

Figure 6. Measured output frequency against the control voltage.

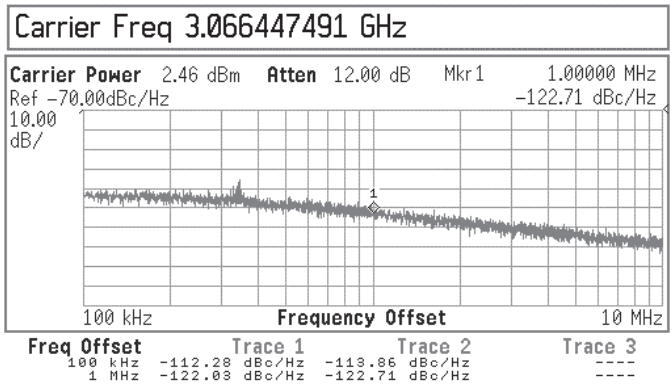

Figure 7. Measured phase noise at 3 GHz.

Table 1. Comparison of VCOs performance in 0.18 µm CMOS.

Ref.	Power (mW)	f_{osc} (GHz)	TR (%)	Phase Noise (dBc/Hz)	FOM[1]	FOM$_T$[2]
[6][3]	1.9	2.28–2.59	13	−125.5@1 M	−190.8	−193.1
[8]	3	4.25–5.12	17	−115.7@1 M	−184.9	−189.5
[9]	2.88	9.5–10.1	6	−106.9@1 M	−182.4	−178
[10]	3.92	4.57–5.83	24	−116.7@1 M	−183.8	−191.4
[11]	3.63	1.48–1.83	21	−123.3@1 M	−184	−190.4
[12]	4.1	2.33–2.62	11.7	−125.8@1 M	−187.1	−187.8
This Work	2.33	2.59–3.08	17	−122.7@1 M	−188.8	−193.5

1 FOM $= L(\Delta f) - 20\log(f_O/\Delta f) + 10\log(P_{DC}/1\,\text{mW})$

2 FOM$_T$ = FOM $- 20\log(TR/10)$

3 Simulation results

from 0 to 1.5 V. The measured performance is summarized in Table 1. The results demonstrate the improvement of the power consumption by the proposed biasing method. It can be seen that the proposed VCO can simultaneously achieve low phase noise, low power dissipation, and wide tuning range, leading to better FOM and FOM_T [7].

4. CONCLUSION

Low power consumption VCO using the adaptive body-biasing technique in 0.18 μm CMOS technology is presented. The adaptive body bias technique increases the oscillation amplitude and decreases the power consumption. The double-pseudo-resistance in series with the cross-coupled pairs which are biased by the tapped node of the inductor is introduced to reduce the power consumption. The power consumption is as low as 2.33 mW from a 1.5 V supply. The output frequency tuning range of the proposed VCO is 2.59–3.08 GHz and the phase noise is −122.7 dBc/Hz@1 MHz.

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