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A NOISE SUPPRESSION TECHNIQUE USING DUAL LAYER SPIRALS WITH VARIOUS GROUND STRUCTURE FOR HIGH-SPEED PCBS

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Abstract—In this paper, small dual layer spirals with several various ground structure are applied in the vicinity of the DDR3 high-speed circuit to achieve noise suppression characteristics up to 3.2 GHz region. For wider noise suppression bandwidth, the dual layer spirals with various ground structure, which provide high self resonance frequency (SRF) as well as inductance value, are implemented. The proposed dual layer spiral with various ground clearance dimension exhibits greater than 9 dB power noise suppression characteristics in the frequency range of interests and achieve about 50% voltage fluctuation reduction in time domain compare to the reference case model. To validate the effectiveness of the proposed model, sample PCB are fabricated and measured. It shows good agreement between the measured and simulated results up to 3.2 GHz.

1. INTRODUCTION

As a clock frequency of high performance mixed signal circuits and systems become faster and faster, the ground bounce noise (GBN) and simultaneous switching noise (SSN) on a power distribution network (PDN) have been one of the most important issues, since these cause significant problems in the signal integrity (SI), power integrity (PI), as well as electromagnetic interference (EMI) [1].

In the off-chip signaling, charging and discharging transmission lines induce return current on PDN, it plays a critical role in SI and PI. To achieve a return current path and eliminate the return path discontinuity (RPD) there are several solution to resolve the

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problem [2, 3]. In addition, there are also studies on chip/package level noise reduction methods and organization of power ground stack-up to enhance the SI [4, 5]. Various noise suppression techniques have been introduced in the previous documents for stable operation of the PDN [5–15]. Conventional suppression methods have adapted decoupling capacitors or embedded capacitors, split power/ground planes, and other techniques. Applying decoupling capacitors between the power and ground planes is well known method as a typical approach to suppress the SSN [6, 7]. However, they cannot effectively suppress the SSN above a few hundred megahertz (MHz) due to parasitic inductances and resulting resonance of the decoupling capacitor. Although using a moat on the power/ground planes can be useful to reduce the SSN in high frequency region [8]; however, this approach is a narrowband solution. Recently, to eliminate the SSN in gigahertz (GHz) frequency ranges, electromagnetic bandgap (EBG) structures have been proposed as an effective solution [9–12]. Even further there are practical improvements of the suppression bandwidth and signal integrity using localized EBG structures in conjunction with decoupling capacitors [13]. Specifically, a localized spiral resonator geometry on a power plane is proposed for noise filtering from 0.2 to 12.5 GHz frequency range [14]. The practical implementations of the spiral have also been studied regarding the relation between the noise suppression level, inductance, and self resonance frequency (SRF) of the DDR3-1600 PCB [15].

The main purpose of this paper is to enhance the noise suppression characteristics with very small dual layer spirals with various ground clearance hole dimensions. This paper is organized as follows: analysis of the several spirals and noise suppression characteristics of the proposed structures are investigated in Section 2. In addition, to obtain more wideband noise suppression characteristics, the dual layer spirals with various ground clearance dimensions are introduced in Section 3. In Section 4, the proposed results are verified with experiments and the conclusion is followed.

2. POWER NOISE SUPPRESSION USING THE DUAL LAYER SPIRALS

As Fig. 1(a) shows the overall configuration to analyze the noise suppression characteristics by spiral inductor. In general, the low impedance PDN is preferred to achieve small voltage droop in PDN; however, in this paper high impedance filter such as spiral inductor is applied in the noisy part of PDN to prevent the noise coupling. A decoupling capacitor is closely located to the driver power port working

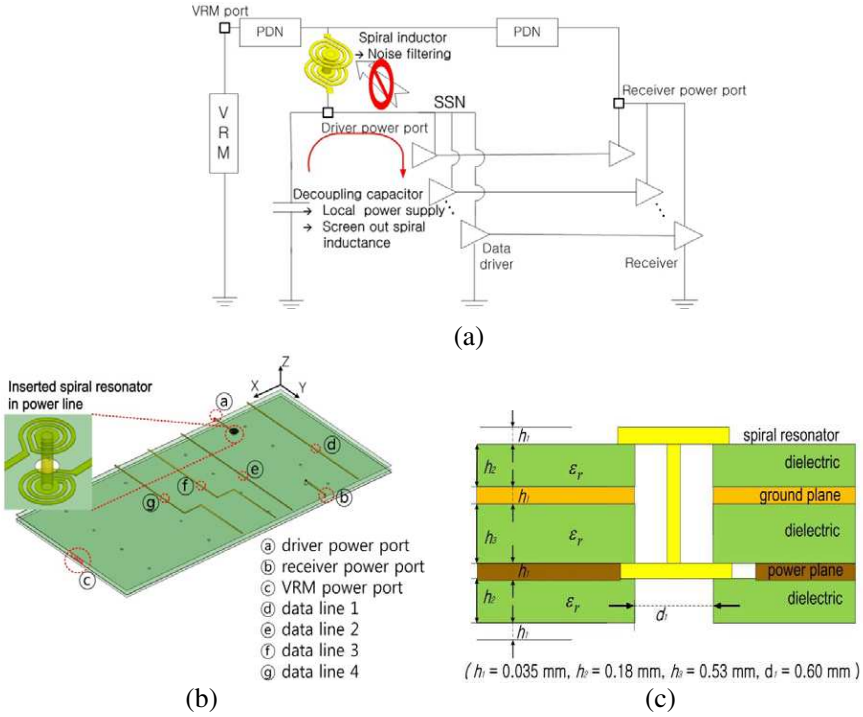


Figure 1. SSN suppression by spiral inductor in PCB. (a) Noise filtering by spiral inductor on driver power port. (b) Three-dimensional view of the PCB with spiral inductor. (c) Cross-sectional view of the PCB.

as a local power supplier to the driver IC and screen out the inductance of the spiral inductor to achieve the low impedance PDN at driver IC. When drivers are switching simultaneously, the SSN is generated and coupled to other PDNs. The spiral on the driver power line operates as a low pass filter to suppress the high frequency noise in PDN. Thus, the decoupling capacitor should be placed closer to driver power port than spiral inductor, since the decoupling capacitor make low impedance at driver power port and the spiral inductor make high impedance to filtering SSN noise.

The overall power network with spiral design procedure is illustrated in Fig. 2. From the S-parameter and high-speed signal specification of PCB, frequency range of suppression band can be achieved considering the channel of signal. To control the impedance of power/ground plane over the desired frequency band, proper spiral inductor is selected considering SRF and inductance. And the voltage fluctuation levels are checked using time domain simulation.

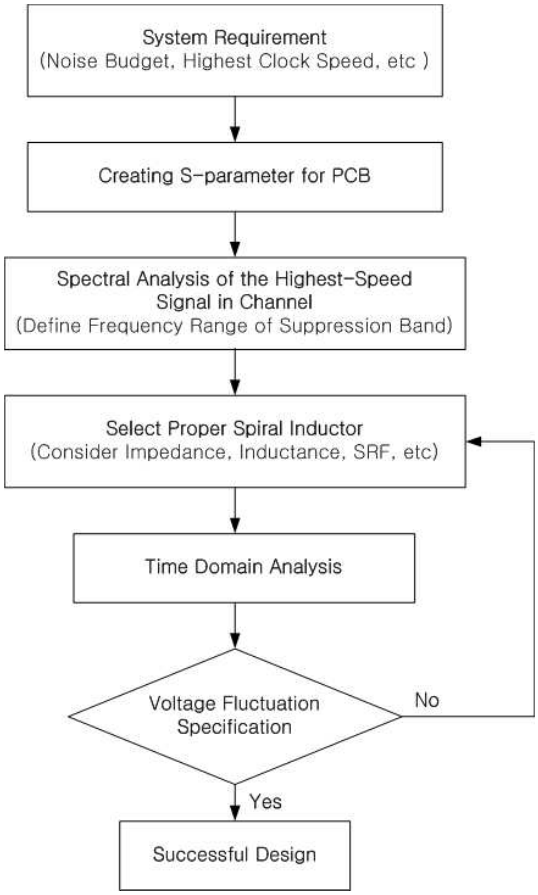


Figure 2. Design flow for PDN with proper spiral inductor.

2.1. Power Spectrum Analysis of the DDR3-1600 PCB

As shown in Figs. 1(b) and (c), a four-layer PCB is designed for DDR3-1600 memory chip. The PCB has two solid parallel planes; one is a ground plane placed in the second layer and the other is a power plane in the third layer. The size of the plane is $400 \times 800 \times 1\,\text{mm}^3$. The substrate of the designed PCB is FR-4 of which the relative dielectric constant is 4.4 and the loss tangent is 0.02. On the top layer four microstrip transmission lines are placed to be used as data lines.

In addition, there are two power lines used as driver/receiver power net. Three ports are placed as indicated in Fig. 1(b); the first ⓐ for driver power port of the driver integrated circuit (IC), the second ⓑ for the receiver power port of the receiver IC, and the third ⓒ for the voltage regulator module (VRM) supplying the power

to the board. Using three dimensional electromagnetic (3D EM) field solver, transmission characteristics of the PCB with signal distribution network (SDN) and PDN are computed. The input/output buffer information specification (IBIS) model of DDR3-1600 data driver is placed at the signal port, then spectral densities of the signals are computed under the circuit simulation condition as shown in Fig. 3. As summarized in Table 1, the cumulative power of a periodic clock as well as random signals contains about 99% of its power under 2.4 GHz. This result is quite consistent with the knee frequency (f_{knee}) approach given [16],

$$f_{knee} = \frac{1}{\pi T_r} \quad [\text{Hz}] \tag{1}$$

where T_r is the rising time of the signal. In the DDR3-1600 data signal, the T_r is one tenth of the signal period, 125 ps, thus f_{knee} is about

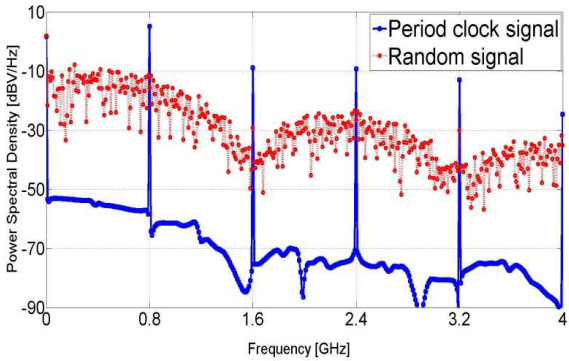


Figure 3. Spectral density of the DDR3-1600 clock and random signal.

Table 1. Spectrum level and accumulated power of the DDR3-1600 data signal.

Frequency [GHz]	Periodic Signal		Random Singal	
	Spectrum level [dBV/Hz]	Accumulated power ratio [%]	Spectrum level [dBV/Hz]	Accumulated power ratio [%]
DC	−7.5	26.28	−7.8	26.37
0.8	−3.3	95.70	−24.2	85.15
1.6	−24.1	96.28	−35.1	97.26
2.4	−17.0	99.20	−33.9	98.70
3.2	−26.2	99.55	−34.6	99.57
4.0	−26.4	99.89	−40.6	99.80

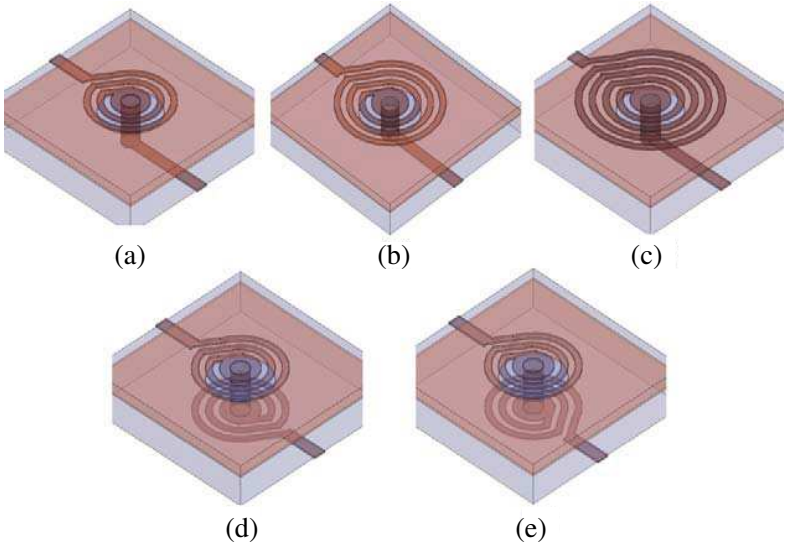


Figure 4. Several types of spiral. (a) Case 1: 2-turn single spiral. (b) Case 2: 3-turn single spiral. (c) Case 3: 4-turn single spiral. (d) Case 4: 2-turn contra-directional current flow dual layer spirals. (e) Case 5: 2-turn co-directional current flow dual layer spirals.

2.5 GHz. Therefore, in this paper, the maximum frequency range of the suppression noise band with reasonable margin is determined as 3.2 GHz.

2.2. Characteristic of the Spiral Inductor

As shown in Fig. 4, several different configurations of the spirals are designed and inserted in driver power line to analyze the characteristic of the proposed structures. The case 1 is a two-turn spiral, the case 2 is three-turn spiral, and the case 3 is a four-turn spiral in the power line. Meanwhile, the case 4 is a two-turn opposite directional (contra-directional) dual layer spirals and the case 5 is a two-turn dual layer spirals having identical current flow direction (co-directional) in the upper and lower layer spirals. All spirals have the identical width and gap of 0.1 mm with same 0.6 mm ground clearance diameter. The areas of dual layer spirals of the cases 4 and 5 are decreased to $1.6 \times 1.6\,\text{mm}^2$, which is 64% smaller compared to the one of the three-turn single spiral having the area of $2.0 \times 2.0\,\text{mm}^2$.

Analysis of spiral inductor is done in time domain and impedance characteristic in addition to frequency domain noise suppression analysis. Moreover, dual spiral with patterned ground structure (PGS)

are applied to enhance the mutual inductance of top and bottom spiral and to reduce the shunt capacitance of spiral resonator, causing almost identical SRF value. As a result more high level of noise suppression characteristic can be achieved in the desired frequency band.

The inductance and SRF of the spirals can be numerically predicted. The inductance value of each spiral is calculate by [17, 18] as,

$$\text{Inductance}(L) = \frac{\text{imag}[-1/Y_{11}]}{2\pi f} \quad [\text{H}] \tag{2}$$

where $\text{imag}[-1/Y_{11}]$ denotes the imaginary part of $[-1/Y_{11}]$ and Y_{11} is the self admittance at port 1. The SRF of the spiral can be obtained using Y-parameters [18, 19]. The resonance occurs when the imaginary part of self admittance, $\text{imag}[Y_{11}]$, becomes zero. The spiral inductor works as an inductor before the SRF region and over that resonance frequency it works as a capacitor. The driver power port is set as a port 1, at the port 1 Y-parameter is obtained and the inductance and the first SRF are computed and summarized in Table 2. As the turn of spiral increases from 2 to 4, the inductance also increase in proportional to the length of spiral. The case 1 shows the smallest inductance value, 7.3 nH, causing the lowest level of noise suppression characteristics. However, it has the highest SRF, 2.5 GHz, making it suitable for wideband noise suppression. The case 3 reveals the largest inductance value, 16.7 nH, providing high level of noise suppression characteristics. Of cause, it has the lowest SRF, 1.4 GHz, due to the longest length of spiral resulting narrow band characteristics. The case 2 shows the middle of cases 1 and 3. Though the spiral length of case 2 is shorter than that of cases 4 and 5, the inductance of the case 2 turns out similar to the that of case 4 and case 5, since it has more mutual inductance in 2-turn and 3-turn in case 2. The

Table 2. Inductance and SRF of various spiral.

Cases	Turns of spiral	Length of spiral [mm]	Inductance at 100 MHz [nH]	First SRF [GHz]
Case 1	Single 2-turn	8.4	7.3	2.5
Case 2	Single 3-turn	13.9	11.2	1.8
Case 3	Single 4-turn	20.5	16.7	1.4
Case 4	Dual contra-dir. 2-turn	15.8	11.2	1.7
Case 5	Dual co-dir. 2-turn	15.8	11.1	1.7

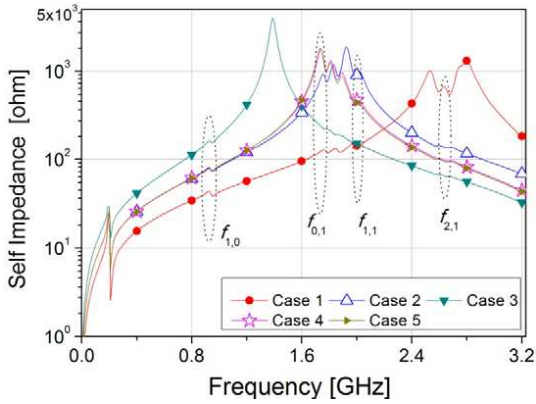


Figure 5. Self impedance characteristics of several spirals at driver power port.

noise suppression level and bandwidth can be estimated using these inductances and SRFs of the spirals [15].

To investigate the noise suppression characteristics of the spirals on the PCB, the self impedance at the driver power port is analyzed in Fig. 5 to assess the noise filtering efficiency of the proposed spirals on the condition of VRM connect. It is interesting to note that the peak point of the self impedance matches with the SRF in each case. The impedance values increase up to SRF region and decrease after that frequency range. The self impedance of the cases 1 to 3 show that as the spiral turn increases from 2 to 4 the impedance value increases up to the SRF range. Both of the cases 4 and 5 having dual layer spirals reveal identical level of noise suppression characteristics with the case 2 up to SRF range. The performance of case 1 shows the low self impedance value below 2.0 GHz, causing low level of suppression characteristics in these region. The performance of case 3 shows the highest self impedance up to 1.4 GHz region, making it suitable for high level of noise suppression characteristics; however, it decreases rapidly above 1.6 GHz region. The cases 2, 4 and 5 reveal peak impedance level in 1.8 GHz region, which is almost the center of the frequency range of interest in the suppression noise band, thus these geometry are suitable for the frequency range of 3.6 GHz. There are also fluctuation phenomenon of the self impedance which are quite consistent with the parallel plate resonance frequency between the power and ground planes such as $f_{1,0}$, $f_{0,1}$, $f_{1,1}$, and $f_{2,1}$. The resonance frequency of each mode can be calculated as follows [20]:

$$f_{mn} = \frac{v}{2}\sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2} \text{ [Hz]} \tag{3}$$

where m and n is mode number and a and b is the length of the PCB, and v is wave velocity in PCB.

2.3. Power Noise Suppression

As shown in Fig. 6, the power noise suppressions are analyzed using these circuit simulation configurations. A decoupling capacitor is placed near the power port which has the value of the equivalent series resistance (ESR), capacitance (ESC), and inductance (ESL) as 1.0 ohm, 33.0 nF, and 1.0 nH, respectively. The data signals of DDR3-1600 are excited to the signal lines, generating SSN at the driver power port [3, 21]. The SSN are suppressed by the spiral inductor and the suppression levels are measured at the receiver power port.

To compare the noise suppression characteristic, the reference model is designed having low impedance PDN with power/ground plane and no spiral on the power net. Six different cases including

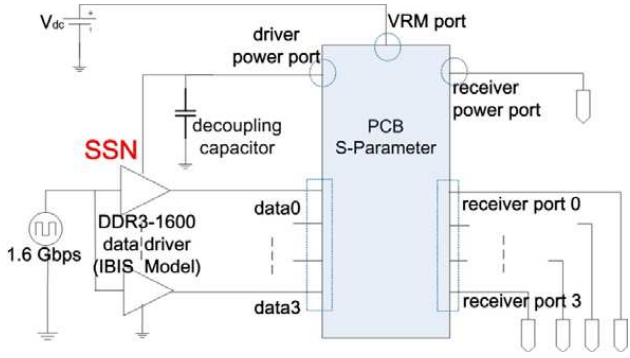


Figure 6. Configuration of SSN circuit simulation.

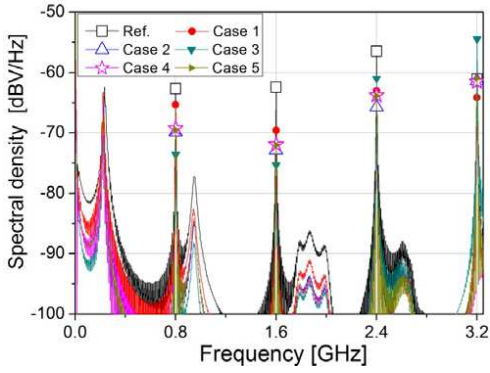


Figure 7. Noise suppression characteristics by various spirals.

reference model having no spiral in power line are simulated and the spectral densities at the receiver power port are shown in Fig. 7. The reference case which has no spiral inductor shows the highest power noise coupling into the receiver power port up to the third harmonics (2.4 GHz). The case 1 turns out to be wideband noise suppression characteristics with relatively low suppression level compared with the other cases. The case 3 has good noise suppression characteristics up to the second harmonics (1.6 GHz); however, the performance is rapidly degraded as the frequency increases above 2.4 GHz. The cases 2, 4 and 5 show effective broad band noise suppression characteristics up to the third harmonics (2.4 GHz); however, at the fourth harmonics (3.2 GHz) the suppression of the noise worse than case 1 owing to lower SRF value of the spirals. It is important to note that there are strong causal relationship between the noise suppression level and the self impedance at each frequency region. Therefore, it makes sense to

Table 3. Peak-to-peak voltage fluctuation comparison by various spirals.

Cases	The peak-to-peak voltage level
Reference	73 mV (1.539 ∼ 1.466 V)
Case 1	68 mV (1.537 ∼ 1.469 V)
Case 2	51 mV (1.527 ∼ 1.476 V)
Case 3	45 mV (1.524 ∼ 1.479 V)
Case 4	48 mV (1.529 ∼ 1.481 V)
Case 5	49 mV (1.529 ∼ 1.480 V)

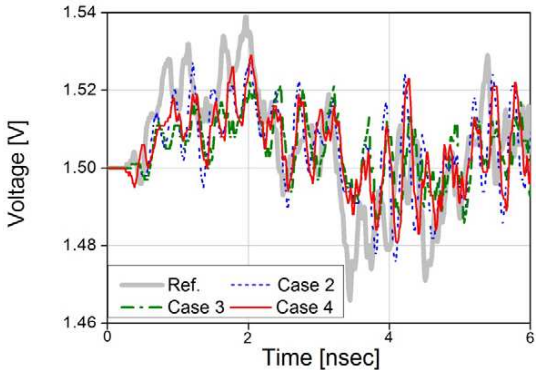


Figure 8. Noise voltage level comparisons: reference, case 2, case 3, and case 4.

evaluate the self-impedance of spiral for determining the appropriate spirals to suppress the noise in frequency range of interest. As shown in Table 3 and Fig. 8, the peak-to-peak voltage levels at the receiver power port of the reference and cases 1 to 5 are 73, 68, 51, 45, 48, and 49 mV, respectively. Although the margin of VDD swing ratio of DDR3-1600 is 10% (1.425 $\sim$ 1.575 V) by JEDEC Standard, all structures satisfy the specification; however, the proposed cases 3, 4, and 5 achieve more than 30% noise-reduction ratio compared with the reference case PCB having no spiral inductor.

3. POWER NOISE SUPPRESSION BY THE DUAL LAYER SPIRALS WITH VARIOUS GROUND CLEARANCE DIMENSIONS

3.1. Characteristics of the Dual Layer Spirals with Various Ground Clearance Dimensions

Usually, the spirals with PGS are used to achieve high Q resonators in chip level circuit [22, 23]. However, in this paper, the PGS is applied for multilayer PCBs environment to obtain robust noise suppression characteristics in high frequency regime. As shown in Fig. 9, a dual spiral can be modeled as two π-equivalent circuit [24]. The L_s and R_s represent the series inductance and resistance of the conducting metal path. The series capacitance between the spiral and center-tap is characterized by the C_s. The C_{sh} represents the capacitance between the spiral and ground layer. Various approaches have been reported in the literature to estimate C_s, L_s, and C_{sh} values, such as Greenhouse

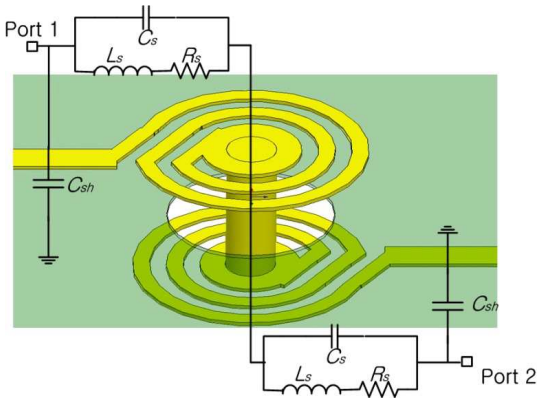


Figure 9. Two π-equivalent circuit model of a spiral inductor.

formula [25], modified Wheeler method [26], and modified coupled line method [27]. From the equivalent circuit model of the spiral, under the condition of ideal (infinite) electrical conductivity ($R_s \rightarrow 0$), the following relations are established:

$$Y_{11} = \left.\frac{i_1}{v_1}\right|_{v_2=0} = j\omega C_{sh} + \frac{1}{2}\left(j\omega C_s + \frac{1}{j\omega L_s}\right), \tag{4}$$

where i_1 and v_1 are current and voltage defined in port 1. When imag[Y_{11}] becomes zero, the resonance occurs [18,19] and the resonance frequency of the spiral, f_{res}, can be expressed as follows:

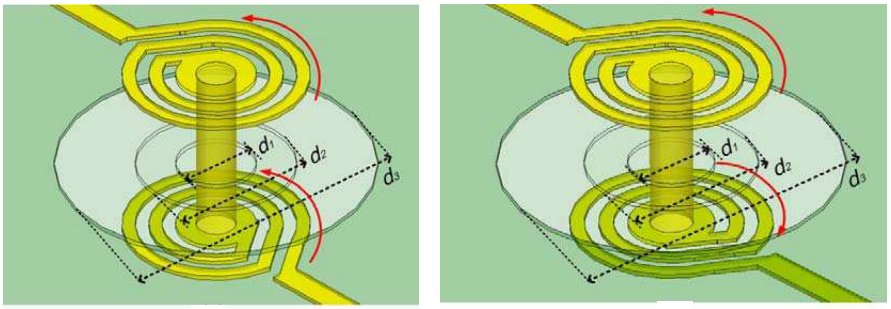
$$f_{res} = \frac{1}{2\pi\sqrt{L_s(C_s + 2C_{sh})}}\ [\text{Hz}]. \tag{5}$$

Usually the C_{sh} is much larger than C_s, thus it is important to notice that C_{sh} is dominant factor of resonance frequency and inversely proportional to the ground clearance diameter [27] such as

$$C_{sh} = \frac{1}{\text{Diameter of clearance hole}}. \tag{6}$$

As the size of the ground clearance increases, the C_{sh} rapidly decreases, while the L_s increases due to the extended return current path, so the value of f_{res} is determined by both L_s and C_{sh} value in Equation (5). In addition, capacitance of via is also inversely proportional to the diameter of clearance hole in ground plane [28] and affect f_{res}.

As shown in Fig. 10, a few different sizes of the clearance holes are designed and its effects are evaluated in the dual layer spirals. The



(a) (b)

(d_1=0.6mm, d_2=1.2mm, d_3=2.4mm, Current path: ⟶)

Figure 10. Variation of ground clearance diameter for the optimized ground structure. (a) Co-directional current flow dual layer spirals. (b) Contra-directional current flow dual layer spirals.

Table 4. Inductance and SRF of the dual layer spirals with various ground clearance dimensions.

Cases	Spiral current direction	Ground clearance diameter [mm]	Inductance at 200 MHz [nH]	First SRF [GHz]
Case 6	Same	1.2	11.4	1.7
Case 7	Same	2.4	13.7	1.8
Case 8	Opposite	1.2	11.7	1.8
Case 9	Opposite	2.4	12.7	1.8

cases 6 and 7 are designated as co-directional dual layer spirals having 1.2 mm and 2.4 mm clearance hole diameter, respectively. On the other hand, the cases 8 and 9 are allocated for contra-directional dual layer spirals having 1.2 mm and 2.4 mm clearance holes dimensions, respectively.

Inductance and SRF values of four cases are computed and summarized in Table 4. As the size of the ground clearance holes increase from 1.2 to 2.4 mm, the inductance increases from 11.4 to 13.7 nH for the co-directional cases, while it becomes 11.7 to 12.7 nH for contra directional current flow cases. The reason of higher inductance of co-directional case, case 7, than one of contra-directional case, case 9, is that mutual inductances of top and bottom spirals are fully added in 2.4 mm clearance hole dimension. Note that as the clearance hole size increase the inductances of the spiral also increase, causing high noise suppression characteristic, while providing almost identical SRFs.

Figure 11 shows the self impedance of the cases 6 to 9. As the clearance size increases from 1.2 to 2.4 mm the self impedance value and bandwidth are increase in both of co- as well as contradirectional current flow cases. The self impedance value increase from 174 to 220 ohm for the co-directional case and from 192 to 243 ohm for the contra-directional case, at third harmonics (2.4 GHz). Also, both of the cases 7 and 9 having 2.4 mm clearance hole size exhibit improved higher self impedance at the fourth harmonics (3.2 GHz) allowing better noise suppression performance.

3.2. Power Noise Suppression by the Dual Layer Spirals with Various Ground Clearance

A noise suppression characteristics by the dual layer spirals with various ground clearance hole dimensions are shown in Fig. 12. The cases 7 and 9 show excellent noise suppression up to the fourth

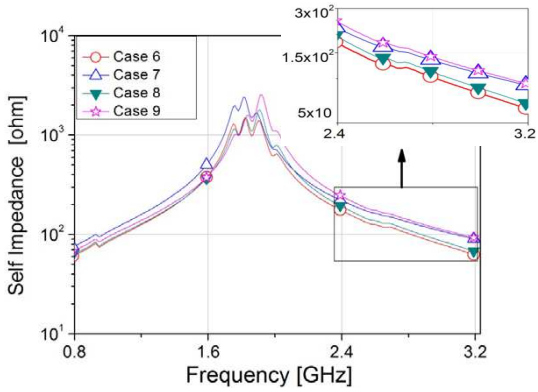


Figure 11. Self impedance at driver power port of several dual layer spirals with different clearance diameter.

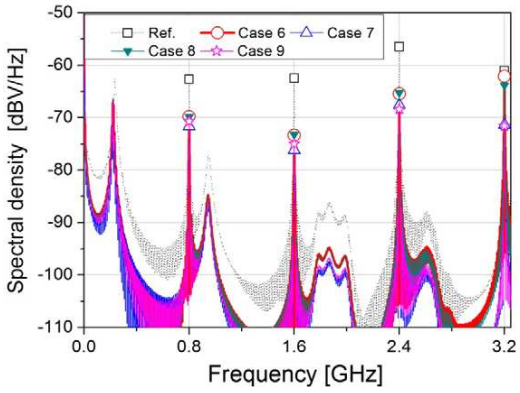


Figure 12. Noise suppression characteristics by various dual layer spirals with different clearance diameter.

harmonics (3.2 GHz). As the clearance hole diameters increase from 1.2 to 2.4 mm, the noise suppression characteristics are improved from 1.0 to 10.3 dB for the co-directional case and from 2.8 to 10.5 dB for the contra-directional case at the fourth harmonics (3.2 GHz). The advantages of using the dual layer spirals with large clearance hole dimension are broad-band noise suppression characteristics due to both of the large inductances and high SRFs, which result in effective noise suppression at high frequency region. For example the case 7 reveals 9.0, 13.7, 11.0, and 10.3 dB and case 9 turns out 8.0, 12.5, 11.9, and 10.5 dB power noise suppression performances at the first, second, third, and fourth harmonics, respectively, compared with the reference

Table 5. Peak-to-peak voltage fluctuation comparison by spirals with various ground clearance.

Cases	The peak-to-peak voltage level
Reference	73 mV (1.539 ∼ 1.466 V)
Case 2	51 mV (1.527 ∼ 1.476 V)
Case 6	41 mV (1.524 ∼ 1.483 V)
Case 7	35 mV (1.521 ∼ 1.486 V)
Case 8	42 mV (1.524 ∼ 1.482 V)
Case 9	37 mV (1.523 ∼ 1.486 V)

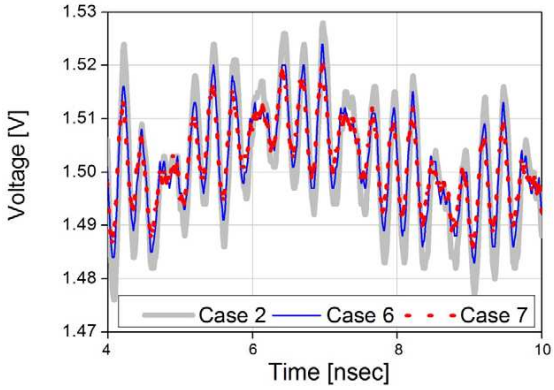


Figure 13. Noise voltage level comparisons: case 2, case 6, and case 7.

model.

As shown in Table 5 and Fig. 13, the peak-to-peak voltage levels decrease as the clearance hole size increase. The peak-to-peak voltage level at receiver power port of the cases 7 and 9 are 35 and 37 mV, respectively, achieving about 50% voltage noise fluctuation reduction in time domain compare to the reference case.

4. EXPERIMENTAL VERIFICATION

The suppression characteristics of power noises can be confirmed by using the transmission coefficients between the ports in the frequency domain. To validate the effectiveness of the proposed dual layer spirals, ten different cases of the PCB are fabricated and measured including reference model which does not have spiral on the power net. Fig. 14 shows the photograph of the fabricated PCB, each type of the

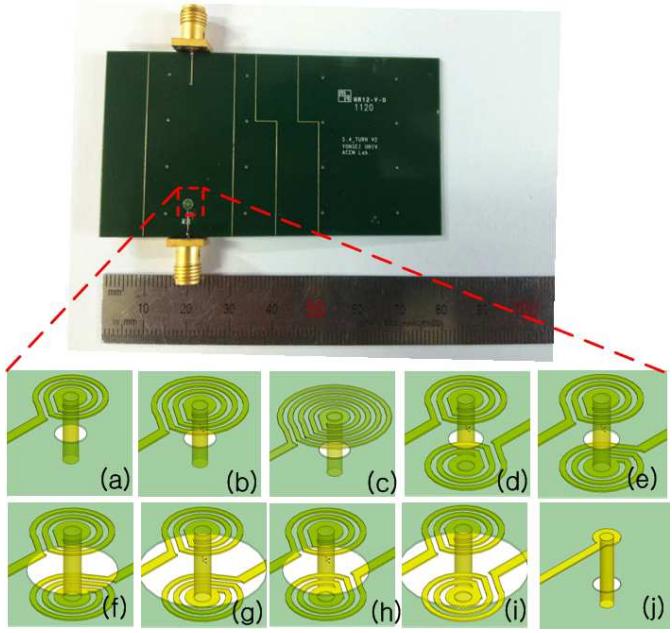


Figure 14. Fabricated PCB. (a) Case 1: 2-turn single spiral. (b) Case 2: 3-turn single spiral. (c) Case 3: 4-turn single spiral. (d) Case 4: 2-turn contra-directional dual layer spirals with 0.6 mm clearance. (e) Case 5: 2-turn co-directional dual layer spirals with 0.6 mm clearance. (f) Case 6: 2-turn co-directional dual layer spirals with 1.2 mm clearance. (g) Case 7: 2-turn co-directional dual layer spirals with 2.4 mm clearance. (h) Case 8: 2-turn contra-directional dual layer spirals with 1.2 mm clearance. (i) Case 9: 2-turn contra-directional dual layer spirals with 2.4 mm clearance. (j) Reference case: No spiral in power net.

spiral is inserted in the power line of the PCB. A three-dimensional electromagnetic field solver and vector network analyzer (Agilent E5071B) have been used to obtain the transmission coefficients between the driver and receiver power ports. Since the dual layer spirals with 2.4 mm ground clearance, the case 9, is predicted to exhibit excellent noise suppression characteristics, these transmission coefficients are compared with the cases 1, 2, and 8. Fig. 15 shows the simulated and measured transmission coefficients for the cases. Even though there are slight differences between the measured and simulated data at high frequency region; however, the overall agreement between the measurement and simulation is excellent up to 3.2 GHz.

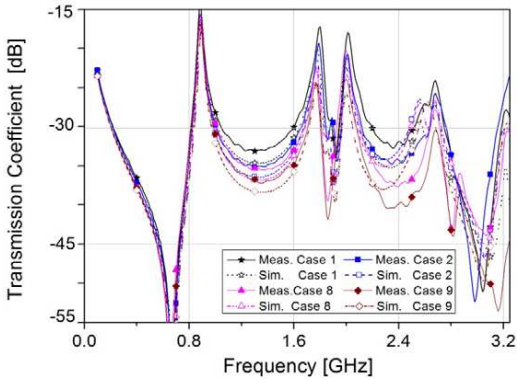


Figure 15. Comparison of simulated and measured transmission coefficients for various dual layer spirals.

5. CONCLUSION

In this paper, power noise suppression method has been thoroughly studied by introducing dual layer spirals on the power distribution network. For wider noise suppression bandwidth, the dual layer spirals with various ground clearance, which provide high SRF as well as inductance, are implemented. The proposed co-directional current follow dual layer spirals with 2.4 mm ground clearance dimension exhibits greater than 9 dB power noise suppression characteristics up to 3.2 GHz region and achieve about 50% voltage fluctuation reduction in time domain compare to the reference model. The same principle of dual layer spirals with various ground clearance dimensions can be applied to even higher frequency PCB.

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