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HIGH PERFORMANCES LOCAL OSCILLATOR SIGNAL DRIVER FOR 60 GHz I/Q SYSTEMS IN 65 nm CMOS TECHNOLOGY

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Abstract—This paper shows the design of a reduced size system that drives local oscillator (LO) signal generated by a voltage controlled oscillator (VCO) in the transceiver system, which is based on I and Q architecture. The aim of this work is to obtain a small system capable to drive two differential mixers and one phase locked loop block with high power efficiency. The entire system drives two differential outputs to their respective mixers with a minimum differential LO power of −1 dBm and a maximum of 0 dBm between 56.5 and 60 GHz. The system furnishes −7 dBm to the PLL, allowing the control of the carrier. The output ports are matched at 50 Ω and they achieve a reflection loss under 10 dB in the whole band of interest. The power consumption of the entire system is 58 mW. The size including RF and DC pads is $0.6 \times 0.7\,\text{mm}^2$.

1. INTRODUCTION

The 60 GHz unlicensed band with his wide channels and relatively high power emission has raised great interest in these years. Various and interesting applications have been proposed and a lot of investments have been delivered to give the opportunity to open this new market at the ultra-wideband applications. The principal areas of application are oriented to mass production as the wireless high definition video and ultra wideband personal area network (WPAN). The limited distance of transmission of the 60 GHz band offers an intrinsic advantage in terms of security: the atmospheric oxygen absorption (about

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10 dB/km) limits the transmission below 100 meters and the high absorption value of concrete and wood limits the field to only one room in a house. Hence the limited distance of transmission guarantees very low interferences between different transceivers that employ the same transmission band in the same building. Others applications for this technology are wireless sensor networks (WSN). Many sensors (tens or hundreds, depending in the data rate acquisition) will be placed into a device under test (it could be a plane, a car, an engine or a human as well) and with them it is possible to acquire an enormous number of data without fall into the known problem of the wired connections. To increase the attractiveness of this band and to favorite an environment of application as wide as possible, cheaper technology are needed. CMOS bulk technology allows this feature and permits a mass production of component at very low costs. Another important aspect for this market is the power consumption. Applications like WSNs require very low power consumption to increase their lifetime. Energy efficient transceiver must be designed to satisfy this constraint. This paper talks about a design of high efficiency systems to drive local oscillator signal into I/Q differential transceiver. In Section 3, it will be explained the architecture and the blocks that constitute the component with their characteristics and Section 3 shows the obtained results.

2. POWER SPLITTING SYSTEM DESIGN

Homodyne architectures are requested to reduce the power dissipation on the transceiver. Hence, only one carrier signal is necessary to allow frequency conversion. The VCO provides the carrier in the 60 GHz band. The path of the LO signal delivered by the VCO towards the mixers should suffer losses as lowest as possible. In this paper, the structure took as example is a receiver adopting I/Q differential architecture. The complexity of the I/Q differential signals requires the implementation of a sophisticate structure to drive the carriers. Figure 1 describes the complete I/Q receiver in which the LO power driver system will be employed. The critical point to consider during the design of the circuit are the minimization of losses and parasitic couplings along the I/Q differential lines. Another critical issue is the accurate control of the LO phase. All of these constraints have to be satisfied during the design process in order to avoid undesired response of the system. To the best of authors' knowledge, previous works on this domain was presented by Mo et al. in [1]and Pei et al. [2].

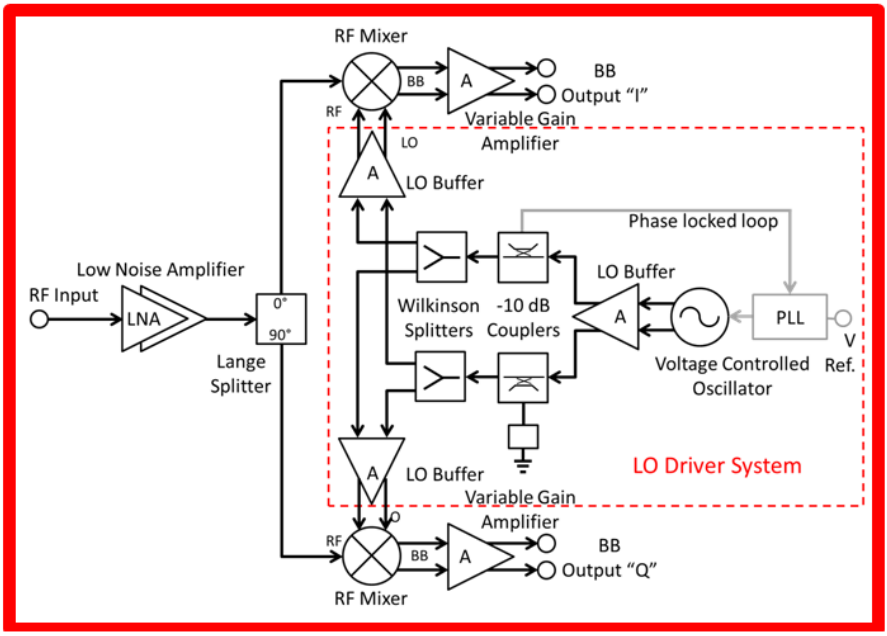

Figure 1. Schematic block for the I/Q receiver circuit with, in the dashed square, the VCO signal divider is highlighted.

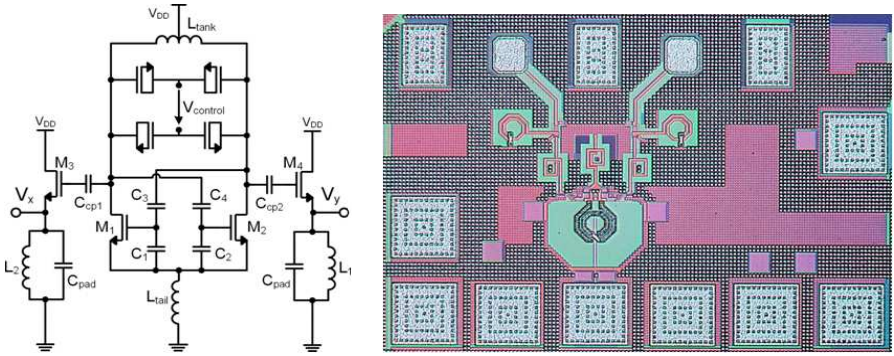

Figure 2. Schematic block for the VCO and microphotography of the realized die.

2.1. VCO

The voltage controlled oscillator furnishes the carrier of the system. The first version of proposed VCO has been developed in our group

by Kraemer et al. [3] the oscillator is based on Colpitts architecture to increase the power efficiency. The VCO schematic and the microphotography of the standalone circuit are shown in Figure 2. The complete oscillator, accurately explained in [3], is composed by a core of four accumulator MOS varactors (AMOS) and a high quality factor tank inductor that constitute the resonator for the oscillator. The LO carrier is extracted from the oscillator core by a source follower buffer. This latter operates as an isolation stage between the VCO core and the rest of the chain and increases the LO power output. The VCO block delivers a maximum of −0.9 dB in differential mode at 60 GHz and a −5 dBm at 57.5 GHz. The power dissipation is 16.5 mW at 1.2 V.

2.2. Coupled-line Coupler

A part of LO signal must be extract from the common source buffer of VCO to drive the frequency divider into PLL circuit. This operation must be done without increase the loads on the buffers. The power needed to drive the frequency divider of the PLL is estimated smaller than −5 to −7 dBm. To achieve this task a small coupled-line coupler has been done. The coupler showed in Figure 3 extracts −12 dB from the direct line. The coupled-line coupler was done employing Metal 7 for the direct output and Metal 8 (ALUCAP) for the coupled output. This is done to minimize the losses in the principal lines and to minimize the variation of the main line impedance. The shape of the coupler is expressly designed to connect the VCO with the input of the pairs of power splitters that send the LO signal on the two mixers. Due to its small size, the coupled branch is not perfectly matched with 50 Ω at the coupled output and a small matching network composed by a 30 pH series inductance is needed. However, the presence of inductance does not cause problem of space; instead, it helps the placement of PLL

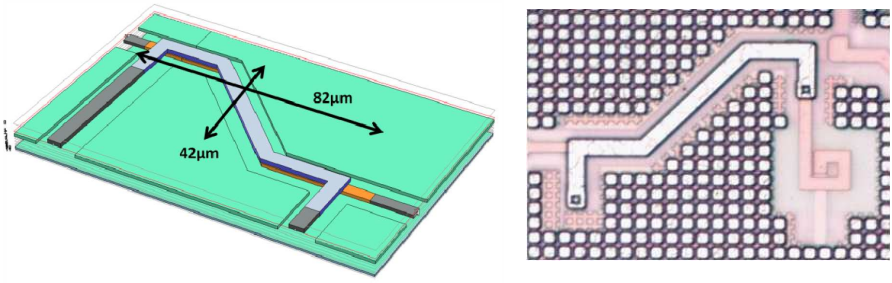

Figure 3. Coupled lines coupler: 3D representation of the coupler simulated by Sonnet 12.52 and microphotography of the device into the complete system.

output buffers. The isolated branch of the coupler is closed to ground with a 50 Ω resistor. An identical coupler is placed also on the other side of VCO output to maintain a high symmetry of the design. This procedure permits to maintain the same phase and amplitude for the differential signal paths.

2.3. Wilkinson Power Splitter

To drive the pair of mixers in the I/Q architecture it is necessary to divide the power delivered by the VCO in two parallel ways. To accomplish this task an efficient and reduced size power splitter is needed. In [4], it was presented a very low losses reduced size Wilkinson power splitter. The compactness of its dimensions is due to the lumped component representation of his $\lambda/4$ lines. Employing a Π representation for the lines and a new R-C network to build the isolation network at the output, the component shows extremely high performances. The bandwidth is over 50 GHz, the return loss in fact is over than −10 dB from 10 to 67 GHz (measured values). Figure 4 shows the realized circuit and the insertion loss and the power balancing in the whole of interested band. The insertion loss is better than 0.8 dB in the whole band. The output isolation is under −20 dB on 60 GHz Band (53 to 67 GHz). These performances are reached with an occupied area of only 0.0055 mm^2 of silicon surface.

2.4. Grounded Coplanar Lines

At the outputs of the pair of Wilkinson splitters there are a couple of differential signals. To conduct the power from the splitters to the output buffer it is necessary to design low losses lines. Grounded

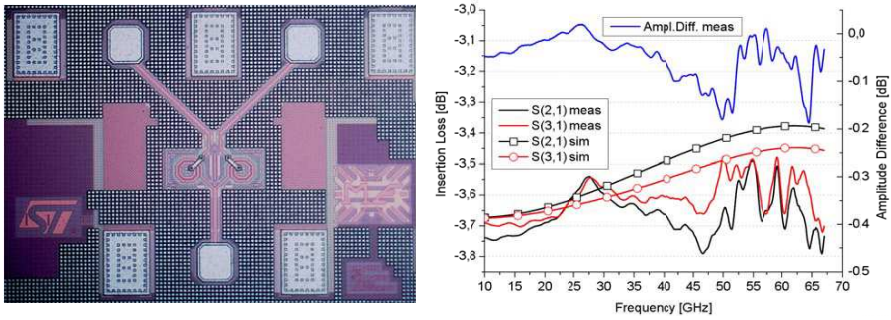

Figure 4. Wilkinson power splitter, microphotography of the test bench circuit realized and insertion loss and amplitude balancing measurements.

coplanar lines are chosen to satisfy this need. These lines are designed to have lowest losses and to maintain as close as possible the phase delay among the four lines. Figure 3 shows the simulation of the phase shift for the four lines and the built circuit. The phase difference remains under 0.3 deg. The synthesis and the simulations are done using Sonnet V12. The lines are built on metal 7 with 4 μm width, and the free space between the line and the coplanar ground is 3 μm. The ground plane is composed by a net of metal 2 and metal 1 line crossed and connected by vias; it is placed on the bottom of the coplanar line to reduce the losses into the silicon substrate. The losses of the lines are 0.26 dB ± 0.02 dB. The return loss instead is lower than −27 dB at 60 GHz. The line crossing, highlighted by a circle at the center of Figure 3, is necessary to permit the exchange of the 0° and 180° signal. The crossing has been simulated and the coupling value between the two lines results lower than −36 dB. This low value is principally due to the low superposed area (only 16 μm square in metal 7/metal 6) and from the reduced area around the lines. This low parasitic contribution does not interfere with the good behavior of the entire system.

2.5. Differential Output Buffers

The last blocks that compose the LO driver system are composed by a pair of differential buffers. The amplifiers are composed by a single stage cell in Cascode configuration with 22 μm transistor width and a 1 μm of finger length, as shown in Figure 6. A common mode inductor of 120 pH and high quality factor is placed at the source of the differential pair to increase the common mode rejection of the buffer. A 80 pH inductor is placed in the middle of the transistor cascade to work as transmission lines. The inductance cancels the parasitic capacitance on the mosfet with a consequent increasing the total f_T. The input and output impedances for the buffer are 50 Ω in accord with the impedance of lines.

The matching networks for the structure have been done employing lumped component inductors and metal on metal (MoM) capacitors. This is done to reduce the occupied area as much as possible. The buffer has a gain of 9.9 dB at 58 GHz and its −3 dB band is from 50.8 to 69.47 GHz. The wideband is obtained with a different frequency matching at the input with respect to the one at the output. Figure 6 shows the reflection coefficient for the IN/OUT ports. The central frequency for the input matching is 54 GHz, instead for the output the frequency matching is obtained at 64 GHz. The maximum gain of the buffer is reached at 58 GHz. This is done to meet the response of the VCO which central frequency is 58 GHz [3]. Each differential buffer absorbs only 12.5 mA with 1.2 V of power supply and

the buffer for the PLL out absorbs only 6.4 mA.

2.6. Complete System Block

The entire system is shown in Figure 5 the total size is $700 \times 600\,\mu m^2$ including RF and DC bias pads. For this version of power driver no current mirror are employed to control bias currents into the buffer. This task is accomplished by DC bias pad placed on top and on bottom in the chip in Figure 7. The total power dissipation for the entire structure is 49 mA at 1.2 V. This value includes the 16 mA of the VCO and the current needed for the 5 buffers (2 differentials and one single ended) present on the chip. The power dissipation is small compared to the level of LO power output delivered from the respective outputs. The values of this power will be shown in the next section.

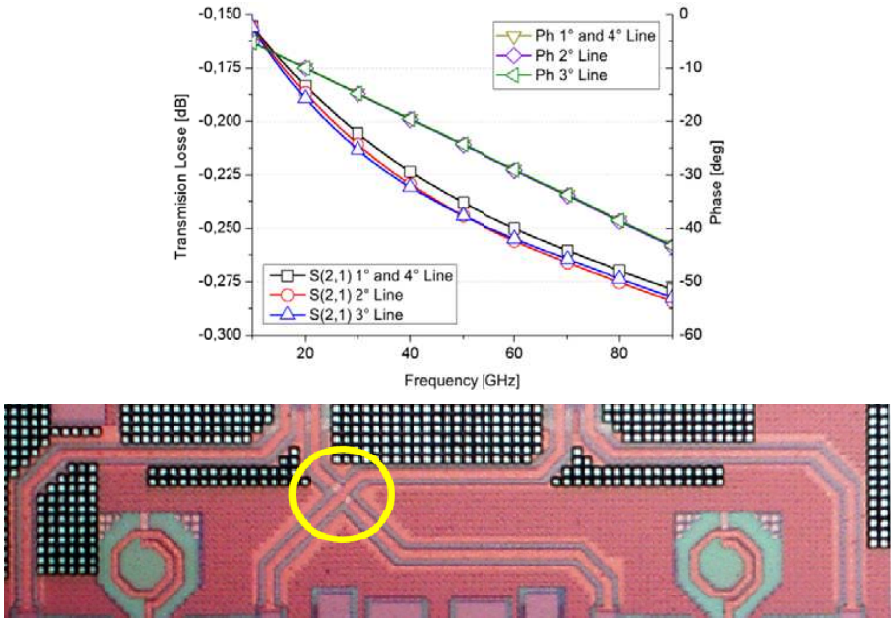

Figure 5. Behavior of the four lines that connect the Wilkinson power splitters and the differential buffer. In the microphotography is highlighted the line crossing between the differential lines paths.

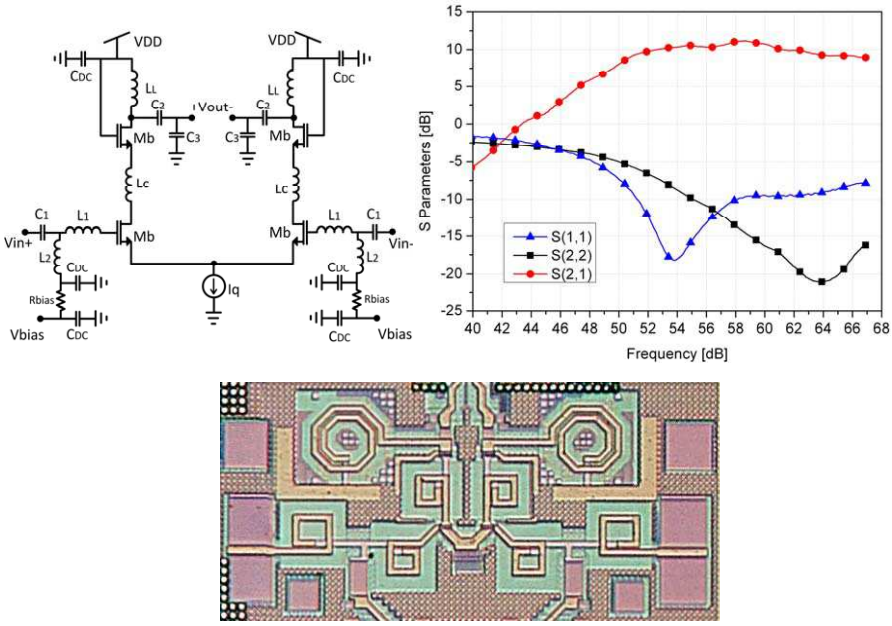

Figure 6. Lumped component scheme of the differential buffer, simulated results for the circuit and microphotography of the realized amplifier.

3. MEASUREMENTS

3.1. Instrumentation and Measurement Constraint

The system has been measured using an Agilent N5247A PNA-X with 4 port VNA to estimate the return loss at the ports. A 20 kHz–67 GHz Rhode & Schwartz spectrum analyzer is employed to estimate the minimum and maximum frequency swing of the system. Finally a power meter Agilent N1913PM is used to estimate the total power delivered from each port.

The system in the work conditions shows two pairs differential output channels to drive two differential mixers and one single ended output to drive the PLL frequency divider. To minimize the silicon surface for the prototype and to simplify the measurement campaign, two outputs have been closed on 50 Ω loads directly within the circuit. The two loads are accurately simulated and the parasitics are extracted to guarantee as much as possible the real desired value of load. The others two outputs, instead, have been connected to the pads to be measured. However, in these conditions the effective load on the

measured ports is different from the load on the on-chip matched ports. The parasitic capacitances added from the pad are estimated. To equilibrate the behaviors a 24 fF shunt capacitor is placed at the output of the on-chip ports.

3.2. Return Loss

The output port impedance measurements confirm the quality of the design. As it has been described in the previous section, the output matching was centered at 55 GHz and the measurements showed in Figure 8 confirm the simulations results. The −10 dB band for the IQ output is 50.7–60 GHz instead, for the PLL output is 53–63 GHz. Ports I and Q show an identical behavior due to the high symmetry of the circuits. For the PLL output the difference on the output matching is due to the small variation on the topology of buffer. The peak at 58.37 GHz is the VCO carrier that runs during the measurements.

3.3. VCO Frequency Tuning

The VCO [3] shows a frequency tuning range (FTR) from 57.58 to 60.80 GHz. Being the VCO common source buffer not perfectly isolated, a charging effect influences the VCO central frequency. As a consequence, the central frequency shifts at lower frequencies. In particular for the measured system for a voltage sweep from −4.84 to

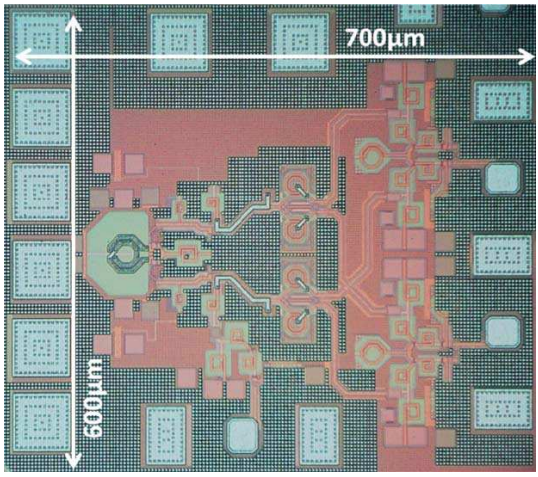

Figure 7. LO power splitter system complete the surface occupied with DC and RF pads is 0.42 mm^2.

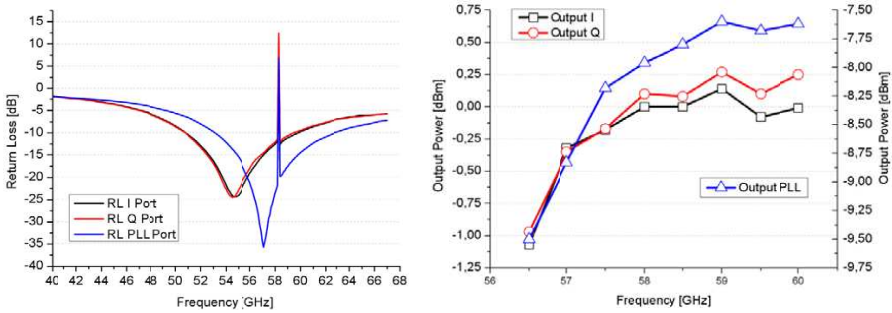

Figure 8. (a) Return loss coefficients. (b) Output power level for differential and single ended ports.

+2 V the FTR is from 56.5 to 60 GHz as shown in Figure 8. The FTR remains the same as the [3] but the capacitive effect on the coupler component and other blocks determines a sensible change on the buffer impedance that causes a shift on the L-C central frequency resonation.

3.4. System Output Power

In [3], the output power delivered from the VCO depends on the frequency. It rises from −5 dBm at 57.58 GHz to −0.9 dBm at 60.52 GHz. This dependence between LO power and frequency influences the mixer behavior's in particular if the mixer is passive. This is partly compensated in the design phase through a buffer with an opposite behavior. The remaining part of the compensation is achieved exploiting the buffer compression point. The saturation of the buffer does not represent a problem because the mixer does not require high linearity signal at LO input port.

The buffer is designed to have an output compression point of +1 dBm. For the high value of input power at 60 GHz a saturation effect is detectable. For lower frequencies instead, this phenomenon is not present. As a consequence, the variation of the total power, shown in Figure 7, is reduced to 1.25 dB, as opposed to the initial 4.1 dB of difference in [3]. The increased flatness of the response improves the control on the mixer. The high power level delivered allows driving easily different type of mixers [5–8]. The small difference between I and Q outputs could be attributed to measurement errors. The difference is limited at only 0.2 dB so the performances of the entire I/Q receiver are not penalized. In Figure 8, the right axis shows power delivered from the buffer at PLL block. The measurements show a lower than

expected value of power. This is probably due to a lower coupling value furnished by the coupled-line coupler. However this drop of power is not considered as a problem, because the minimum power level is still in the range of power accepted for the frequency divider. The power difference in this case is more accentuated. In effect, in this case the low power at the input of buffer does not causes the saturation as on the I/Q output, so the linearity of the characteristic on the buffer does not help to maintain flat the power level at the PLL out. However, as for the absolute power level, the power raise does not affect the good performance of the frequency divider.

4. CONCLUSION

In this paper, it has been shown the design procedure for a high efficiency system to drive local oscillator signal into I/Q differential transceiver. The system shows a high and stable value of LO power at the differential outputs, achieving a maximum of 0.25 dBm in differential mode for a bandwidth of 3.5 GHz (56.5 to 60). The PLL output furnishes a maximum of −7.5 dBm at the frequency divider in order to allow a good control of the carrier. Differently from [1] and [2] the presented power system works to drive an IQ architecture with smaller power dissipation and at 60 GHz frequency instead of 30 GHz. The power consumption of the system is 58 mW. The LO power driver has been used on a complete IQ low power receiver sent at foundry on June 2011.

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