DESIGN AND CHARACTERIZATION OF A W-BAND POWER-COMBINED FREQUENCY TRIPLER FOR HIGH-POWER AND BROADBAND OPERATION

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Abstract—We report on the design, simulation and characterization of a solid-state W-band in-phase power-combined frequency tripler. In order to increase the output power of the frequency tripler without sacrificing efficiency and bandwidth, two mirror-image tripler circuits with four UMS[®] Schottky varistor diode chips are designed and mounted in a waveguide block, which includes a compact double-probe power divider at the input waveguide and a Y-junction power combiner at the output waveguide, respectively. Each circuit chip features four anodes on a 50 mil thick Rogers RT/duroid 5880 substrate. The tripler has $1.2 \sim 3.8\%$ conversion efficiency measured across the $75 \sim 110\,\mathrm{GHz}$ band when driven with 24 dBm of input power at room temperature. With the input power of 27 dBm, $5.5 \sim 11\,\mathrm{dBm}$ of saturated output power is produced over $75 \sim 110\,\mathrm{GHz}$. Suppression of undesired harmonics is greater than 17 dB.

1. INTRODUCTION

Spectrum resources of W-band offer abundant applications including spectroscopy, imaging, communication and radar. One of the most challenging aspects of exploring the spectrum resources is the lacking of compact, reliable, efficient signal sources in this frequency band [1]. A number of technologies can be used to generate millimeter wave signal [2–4], while Schottky diode based frequency multipliers continue to be an ideal solution for the signal generation. From a systems point of view, there are several criteria such as instantaneous bandwidth, DC-to-RF conversion efficiency, spectral purity that can dictate the use of any particular technology, while the output power of the source

is often the single most important criterion. The practical limit of the output power of a frequency multiplier is typically either the power beyond which conversion efficiency drops off due to saturation effects or the device lifetime becoming unacceptably short due to thermal or reverse-breakdown effects. To increase power handling capabilities of the frequency multipliers, one approach is to optimize the nonlinear device doping and transfer the epitaxial layer to a high thermal conductivity substrate, or one can increase the number of anodes per chip [5–9]. However, these two approaches are unrealistic for those who use commercially available discrete Schottky diodes, and the number of anodes will be constrained by the circuit size limit imposed by the narrow transmission waveguide. In the recent years, the use of wide bandgap semiconductors such as GaN-based devices has emerged as a very promising solution for their greatly improved power handling capabilities, but GaN has the disadvantage of a lower electron mobility than GaAs, which results in an increase in the series resistance, and thereby, in lower efficiencies [10]. In order to increase the power handling capability of a frequency multiplication source without sacrificing bandwidth and efficiency, power-combining scheme is proposed. Spatial or Quasi-optical combining is an attractive approach [11–13], but these systems are comparatively bulky, thus not be preferred for a compact design. Since waveguide offers a low loss channel for signal propagation, a waveguide structure has been widely adopted for power-combined frequency multiplication at millimeter or submillimeter wavelength [14–17].

In our former research work implemented at SKLMMW of Southeast University, a microstrip-integrated W-band frequency tripler with single circuit has been developed, but its power handling capability is limited (the diode can be burnt out when pumped with about 25 dBm of input power). In order to increase the output power while keeping its bandwidth and efficiency, an in-phase power-combined version is reported in this paper. At the input waveguide, instead of the Y-junction power divider or branch-line coupler as depicted in [15, 16], a Ka-band double-probe structure is adopted to realize the waveguide to microstrip transition and power divider simultaneously, so the electrical path of fundamental signal can be shortened and the block size can be reduced significantly, which is suitable for compact configuration. At the output waveguide, a compact Y-junction combiner is utilized. Two mirror-image tripler chips with anti-parallel diode pairs are mounted in the transmission channel symmetrically. For efficient power combining, special attention should be paid to minimize the phase error between the two parallel paths despite fabrication and assembly tolerances, and losses in the

dividing and recombining circuits should be reduced as low as possible. The balancing between every Schottky anode has to be precise to achieve high conversion efficiency.

This paper first introduces the design and simulations of power-combined frequency tripler for high power and broadband operation. Then the relevant experiment and analysis are presented. In experiment good results have been obtained, which is consistent with the prediction of the circuit simulation.

2. DESIGN AND SIMULATION OF THE W-BAND POWER-COMBINED FREQUENCY TRIPLER

2.1. Scheme and Design

Figure 1 shows a schematic drawing of the proposed power-combined frequency tripler. The input signal is divided into two parts with equal amplitude and reversed phase. The two signals excite the two anti-parallel diode pairs, respectively. The corresponding output 3rd harmonics are then combined in-phase.

The tripler circuit is based on a 5-mil thin Rogers5880 substrate. Each branch features two UMS$^{\circledR}$ DBES105a diode chips including four Schottky anodes in an anti-parallel configuration. Although this diode is not optimized for frequency multiplying but for mixer operation [17], it is still adopted here for its high cut-off frequency ($f_c = 3\,\text{THz}$). The two E-plane probes located in the input WR28 waveguide couple the signal at the fundamental frequency to their respective microstrip lowpass filters with a phase difference of 180°. The filters are designed to pass the fundamental signal and prevent the 3rd harmonic from leaking into the input. The 3rd harmonic produced by the anti-parallel diode pair is coupled to the output waveguide by second E-plane probes and then combined in phase by a Y-junction combiner.
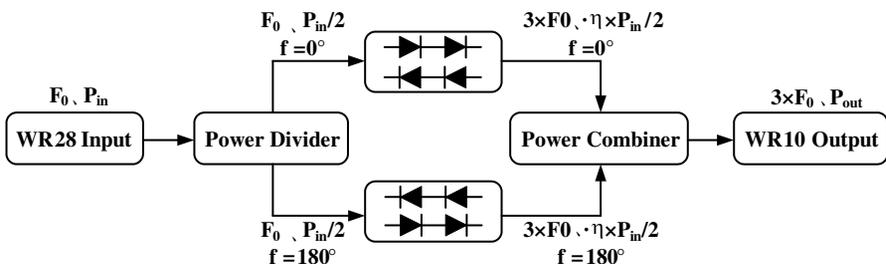
Figure 1. Schematic drawing of the W-band power-combined frequency tripler.

The general method adopted to simulate a frequency multiplier is iterative and consists in decomposing the passive structures in several blocks that are analyzed separately with Ansys[R] High Frequency Structure Simulator (HFSS). The S-parameters corresponding to the different blocks are included in a custom spice model of nonlinear device implemented in Agilent[R] Advanced Design (ADS). The harmonic balance (HBA) simulator of ADS is then used to predict the performance of the frequency multiplier, and the passive embedding networks cascaded with the nonlinear devices are optimized in terms of conversion efficiency and output power. This method is feasible when the operation frequency is comparatively low. As the operation frequency increases, the parasitic effects of the nonlinear diode become significant and the simple spice model of the diode provided by its datasheet is not well enough to characterize its performance. Meanwhile, the coupling between the different blocks will not be included by the simple cascaded S-parameters. However, to predict the performance of the frequency multiplier accurately in high frequency case, this coupling effect can't be neglected. Therefore, a modified method is proposed to avoid these disadvantages. In the modified method, all the embedding networks, the passive parasitic part and the active part of the diode are modeled as a whole structure in the 3-D full-wave solver. The active part of the diode is replaced with lumped port on rectangle between the end of the thin Schottky feed trace and the ohmic GaAs layer [18], so that the diode active part and passive part can be combined. The solved S-parameter matrix is imported into circuit simulator as a multi-port touch-stone file and connected with the ideal Schottky diode to perform harmonic-balance simulation. A number of parameters of circuit related to the performance are optimized and determined. The above mentioned design flow is depicted in Fig. 2.

Figure 3 shows the simulated S-parameters of input double-probe structure with microstrip lowpass filters. It is noteworthy that the broad side of the input WR28 waveguide is extended from 7.12 mm to 7.72 mm near its back-short. This will lower the characteristic impedance of the waveguide and improve the frequency response in the low end of Ka-band. It can be found that S_{11} of the extended double-probe structure is better than that of the unextended one. The simulated insertion loss is $0.2 \sim 0.4$ dB over the $25 \sim 40$ GHz band and the simulated maximum amplitude unbalance is 0.05 dB. The waveguide-to-microstrip transition and power division is realized simultaneously with good performance.

Figure 4 shows the simulated S-parameters of the designed output Y-junction combiner with probe transitions. The simulated insertion
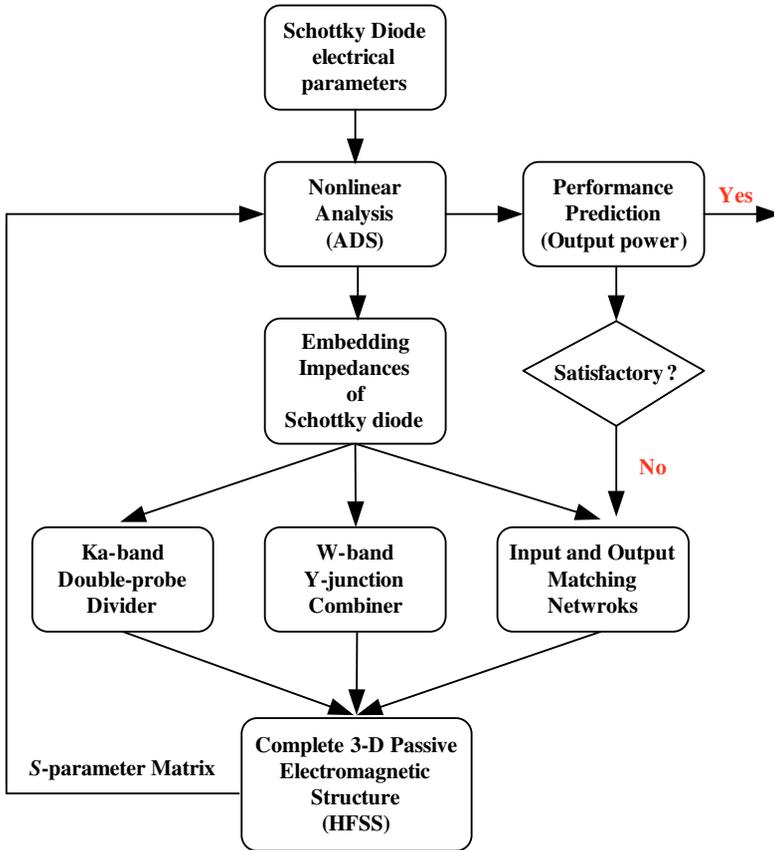
Figure 2. Design flow of the power-combined frequency tripler based on two simulation suites, HFSS and ADS.

loss is about 0.3 dB, and the maximum amplitude unbalance is 0.15 dB.

The main nonlinear spice parameters of DBES105a diode are summarized in Table 1. This is essential to the symbol defined diode model in ADS. Table 2 shows the main physical dimensions of DBES105a, which are required to build the 3-D EM model of the Schottky diode. L_{finger} means length of gold finger, T_{epi} means thickness of epitaxial layer, T_{pav} means thickness of passivation layer, T_{buf} means thickness of buffer layer and T_{sub} means thickness of semi-insulating GaAs substrate.

Generally, high-power frequency multipliers require the use of as many diodes as possible [19, 20]. However, as the number of diodes increases, unbalancing between the diodes may increase, which will
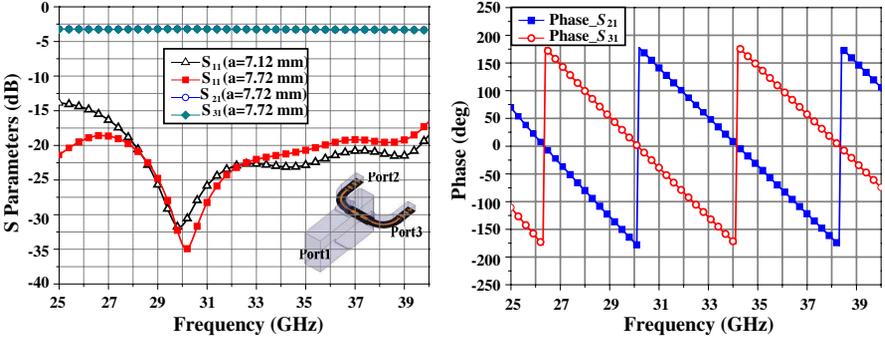
Figure 3. Simulated S-parameters of input double-probe structure.
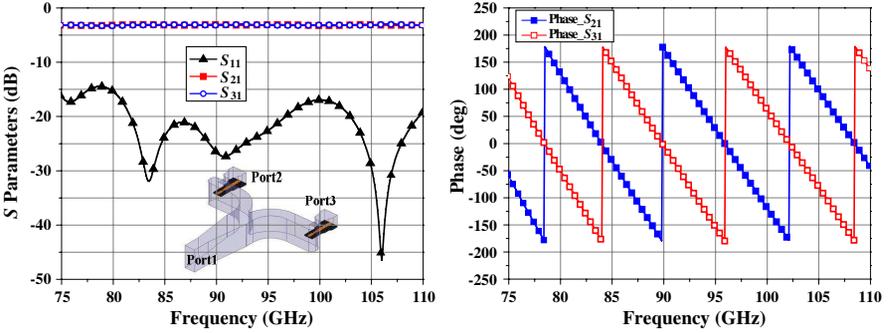
Figure 4. Simulated S-parameters of output Y-junction combiner with probe transitions.

Table 1. Nonlinear spice parameters of DBES105a Schottky diode.

R_s (Ω)	n	I_s (A)	C_{j0} (fF)	V_b (V)	I_{bv} (A)
6.34	1.29	3.80×10^{-14}	9.5	5	0.001

Table 2. Physical dimensions of DBES105a Schottky diode.

L_{finger} (µm)	T_{epi} (nm)	T_{pav} (µm)	T_{buf} (µm)	T_{sub} (µm)
10	100	4	5	110

decrease the conversion efficiency. To achieve high conversion efficiency from the fundamental frequency to the harmonic, special attention should be paid to the balancing between the anodes.

For broadband operation, power nulls should be avoided over the desired bandwidth. In addition to cavity resonance, our group has

revealed that the power cancellation is another crucial factor, which contains fundamental cancellation and 3rd harmonic cancellation, and 3rd harmonic cancellation is more influential than fundamental cancellation. Therefore, the phase characteristics of embedding networks should be optimized carefully to avoid the power cancellation. The related research achievements have been summarized in [21].

2.2. Simulations

Predicted performance of the W-band power-combined frequency tripler is obtained employing the method as above mentioned. The 3-D electromagnetic model of the whole frequency tripler is built with HFSS. Fig. 5 shows the overall model used for simulating the linear response of the frequency tripler. The close-up view of the Schottky diodes with labels for anodes $\#1 \sim \#8$ is also shown.

A 10-port S-parameters file characterizing the linear frequency response of the tripler can be obtained from the 3-D EM model of the tripler shown in Fig. 5, all losses such as waveguide and substrate losses are included in this file. Then, this 10-port file can be exported to ADS and connected with the ideal symbol defined diodes. The nonlinear behaviors of the tripler can be obtained by harmonic-balance simulation based on an integrated model. The schematic drawing of the integrated model used in ADS is shown in Fig. 6.

Among them, the balancing of the anodes at the input frequency is investigated in detail to avoid the risk of overdriving an anode. Fig. 7 shows the input coupling efficiency of each anode in the 25–37 GHz band for a flat input power of 25 dBm. The input coupling efficiency
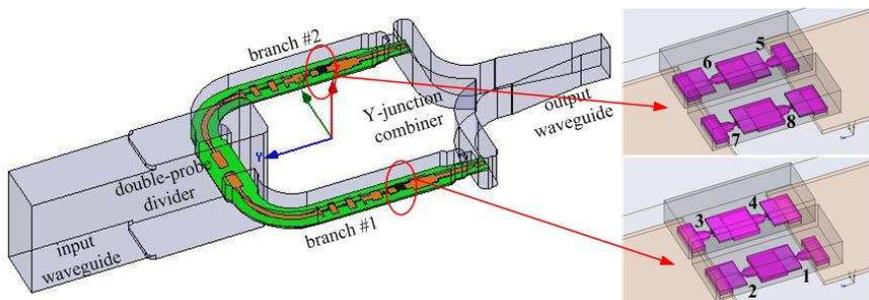
Figure 5. 3-D view of the W-band power-combined frequency tripler as modeled with Ansys® HFSS, including close-up view of the Schottky devices with labels for anodes $\#1 \sim \#8$.
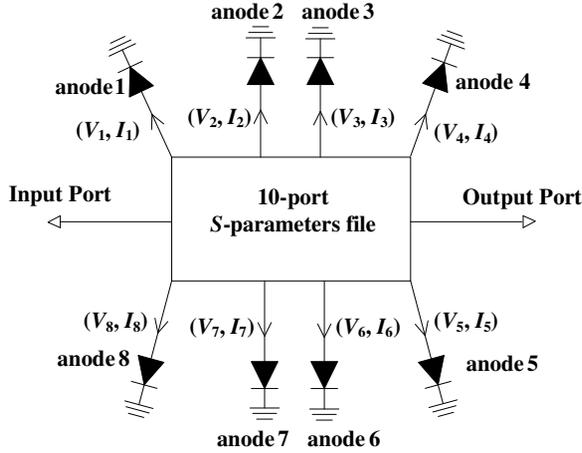
Figure 6. Integrated model for harmonic balance simulation.
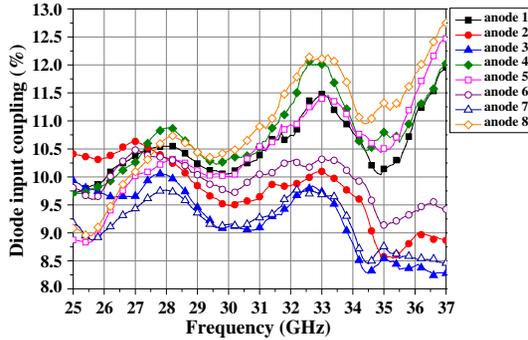
Figure 7. Simulated input coupling efficiency of the W-band power-combined frequency tripler when pumped with 25 dBm of input power.

is defined as following,

$$\text{input coupling efficiency} = \frac{P^1_{anode}}{P_{in}/N} \times 100\% \tag{1}$$

where N is the number of the anodes. Herein, the value of N is 8. P_{in} is the total input power, while $P^1_{anode(j)}$ is the driving power received by each anode, which can be defined as

$$P^1_{anode(j)} = \frac{1}{2}V^1_j \cdot \left(I^1_j\right)^* \tag{2}$$

V^1_j, I^1_j is the fundamental voltage and current across each anode, respectively.

According to the simulation, the balancing at the input frequency is better than 5% for all the anodes. Among them, the balancing between #1, #4, #5 and #8 is better than 1.5% and the balancing between #2, #3, #6 and #7 has the similar performance. It should be noticed that the four anodes (#1, #4, #5, #8) away from the input port receive more driving power than the four anodes (#2, #3, #6, #7) near the input port. This phenomenon indicates that it's not a good choice to increase the power handling capability by increasing the anode numbers in series configuration.

Figure 8 shows the power produced by the same anodes at the output frequency. It is notable that the four anodes (#2, #3, #6 and #7), which receive less input power than the other four anodes (#1, #4, #5, #8) do actually produce more power at the output frequency. This reversal has been also observed by the other researchers [22], and no reasonable explanation has been given. The detailed investigation will be implemented in the subsequent research.

Figure 9 shows the simulated output power and the output coupling efficiency, which is defined as

$$\text{output coupling efficiency} = \frac{P_{out}}{\sum\limits_{j=1}^{N} P^3_{anode(j)}} \times 100\% \qquad (3)$$

P_{out} is the output power of the frequency tripler and $P^3_{anode(j)}$ the power produced individually by the anode $j\#$. All simulations do include the effects of the waveguide losses and are performed with a flat 25 dBm of input power. From 75 to 110 GHz, the output power is $12 \sim 17\,\text{mW}$ from 75 to 105 GHz and decline to almost 4 mW at 110 GHz. The 3-
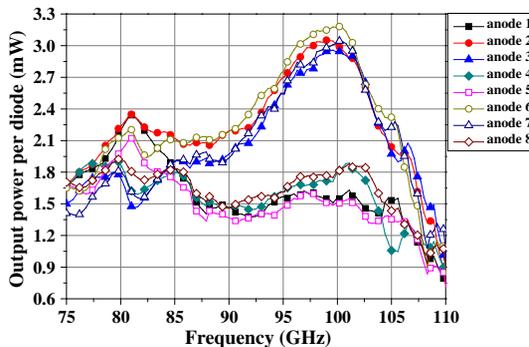
Figure 8. Power produced by each Schottky anode when pumped with 25 dBm of input power.
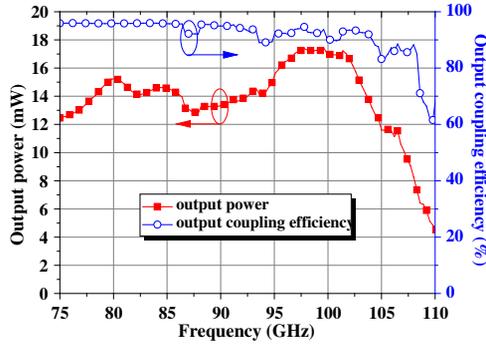
Figure 9. Simulated output power and output coupling efficiency of the W-band power-combined frequency tripler when pumped with 25 dBm of input power.

dB bandwidth extends from approximately 75 to 107 GHz. The output coupling efficiency, however, declines slowly from 95% to 80% from 75 to 108 GHz, and then drops to 60% at 110 GHz.

It can be concluded from Fig. 7 and Fig. 9 that the bandwidth and flatness of tripler has great relation ship with the power balancing between all the anodes. Once the unbalance becomes larger, the flatness of output power is degraded and the bandwidth is limited.

3. FABRICATION AND MEASUREMENT

3.1. Fabrication

Take advantage of standard milling techniques, the cavity of the W-band power-combined frequency tripler is fabricated by brass with two halves and electroplated with gold. The 5 mil thin Rogers5880 circuit chip is located inside a channel with approximately $1.7 \times 1.2 \, \text{mm}^2$ cross section. Schottky diodes are attached to their circuit using silver epoxy (type H20E from Epotek). Symmetry of the circuit and the diodes should be kept to guarantee the balance of the tripler. Therefore, high power-combining efficiency and low even order harmonics can be achieved. An image of the assembled block and complete chip mounted in the waveguide half-block are shown in Fig. 10.
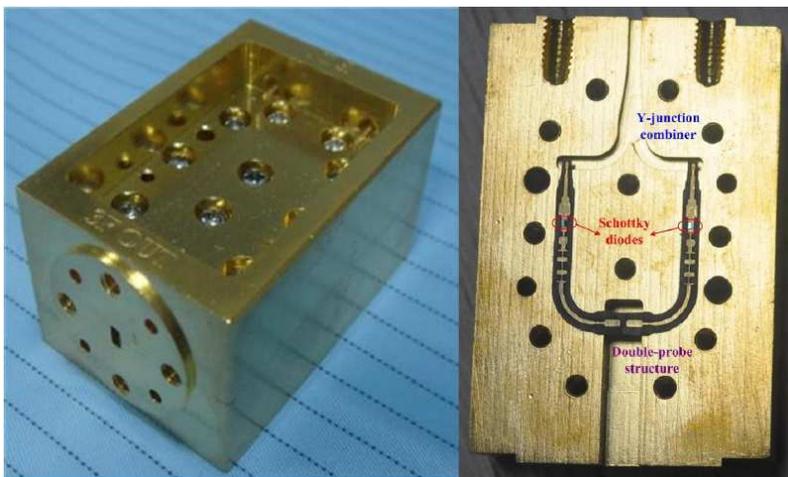
Figure 10. Assembled tripler block and the half-block with circuit mounted in.

3.2. Measurement

3.2.1. Driver Stage and Test Setup

The source used to drive the W-band in-phase power-combined frequency tripler is constituted by an Agilent analog signal generator E8257D followed by a Ka-band power amplifier covering 25–40 GHz. The power amplifier employs two commercially available MMIC chips AMMC6345, fabricated by Avago, Inc. Two signals amplified by AMMC6345 are power combined by a double probe structure. The power delivered by the driver stage at Ka-band is measured using power meter. When pumped with 16 dBm, this amplifier module delivers saturated output power of 27.5 dBm over the 25–40 GHz band, as shown in Fig. 11. This power level is suitable to be handled by the designed frequency tripler.

At room temperature, the output power of the W-band power-combined frequency tripler is measured using PS-28-6 millimeter wave power sensor and DPM-2A power meter. An external WR10 to WR28 waveguide transition is used to match the tripler output waveguide (the measurement of the output power of the tripler is not corrected for waveguide transition loss).

In theory, the even order harmonics can be eliminated by the characteristic of anti-parallel configuration, but they can still be produced by any asymmetry of the circuit. To verify the harmonic content, especially for the 2nd harmonic, which is beyond the cut-off
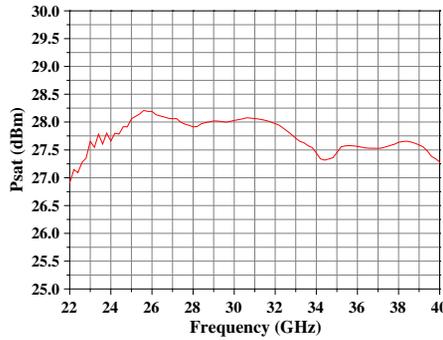
Figure 11. Saturated output power of driving power amplifier.
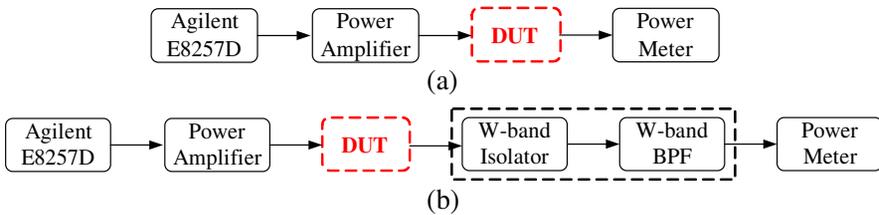
Figure 12. Block diagram of test setup.

frequency of the WR-10 waveguide for fundamental frequencies beyond 30 GHz, a spectrum analyzer is usually required. However, the upper frequency limit of the spectrum analyzer in laboratory is only 26.5 GHz, and there is no proper mixer to down-convert the 2nd harmonic to IF. Therefore, the test setup shown in Fig. 12 is built to measure the output power of the desired 3rd harmonic and the suppression of undesired harmonics.

First, the frequency tripler is measured according to Fig. 12(a) block diagram. Because the power sensor is thermal sensitive, the measured output power may contain the undesired harmonics. Then, as shown in Fig. 12(b), a W-band full-band bandpass filter developed in our laboratory is cascaded to pass through the 3rd harmonic and suppress the undesired harmonics. The measured S-parameters of the filter are depicted in Fig. 13, from which we can find the 2nd harmonic should be greatly attenuated by the bandpass filter, and the desired 3rd harmonics can pass through the BPF with certain insertion loss. It is notable that the upper frequency limit of the VNA is 110 GHz, so the S-parameters above 110 GHz can not be measured at present. In addition, a commercially available W-band full-band isolator is used to alleviate the possible interaction between the tripler and bandpass filter.
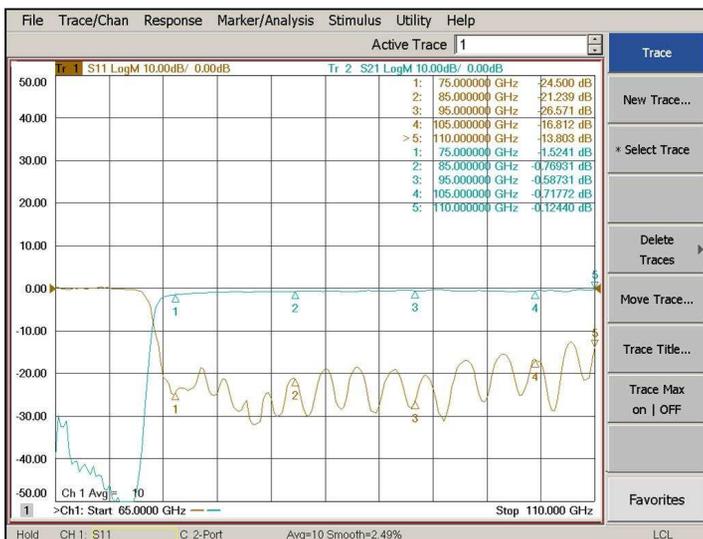
Figure 13. Measured results of the W-band bandpass filter used for harmonic suppression measurement.
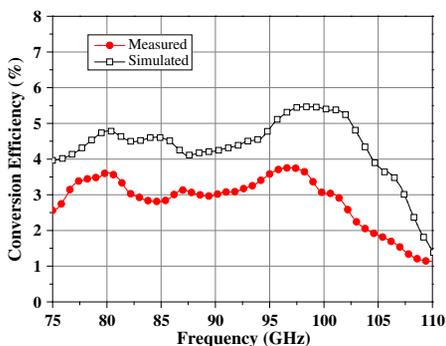
Figure 14. Measured and simulated conversion efficiency (P_{in} = 24 dBm).

3.2.2. Results and Discussion

Figure 14 shows a comparison of the simulated conversion efficiency with the measured one. A flat 24 dBm of input power is assumed for the simulation, and the power level of Agilent E8257D is adjusted so that the power amplifier delivers about 24 dBm of input power, which ensures that no heavy compression will happen. It can be found from measurement that the typical value of efficiency is 3% between

$75 \sim 100\,\text{GHz}$ and gradually drops to 1% at 110 GHz. The maximum conversion efficiency is about 3.8% at 97 GHz.

Figure 15 shows the output power of the power-combined frequency tripler versus input power at Ka-band. A maximum output power of 9.8 dBm is measured at 94 GHz for an input power of 27.5 dBm. At this frequency, the output power increases almost linearly for input power ranging from 18 to 23 dBm. Some compression starts to occur at 24 dBm of input power. At 87 GHz, the tripler behaves almost the same as at 94 GHz, and its maximum output power achieves 10 dBm.

The saturated output power of the Ka-band power amplifier has been shown in Fig. 11, it can be concluded from Fig. 15 that the designed tripler is saturated when pumped with this power level. The total output power measured according to Fig. 12(a) is defined as P_{total}, and the filtering output power measured according to Fig. 12(b) is defined as P_3rd (the insertion loss of bandpass filter and isolator has been calibrated for P_3rd). Therefore, the suppression of the undesired harmonics can be defined based on P_{total} and P_3rd. Corresponding results are shown in Fig. 16. The saturated output power over $75 \sim 105\,\text{GHz}$ band is $8 \sim 11$ dBm and the minimum power is 5.5 dBm at 110 GHz. $17 \sim 23$ dB of the undesired harmonics suppression is measured across $75 \sim 105\,\text{GHz}$.

Table 1 demonstrates the comparison of the designed power-combined W-band frequency tripler with the commercial products and experimental prototypes in laboratory, from which we can found that the W-band frequency tripler developed by our group is comparable to the other frequency triplers.
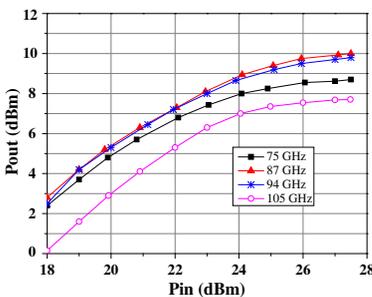
Figure 15. Output power versus input power.
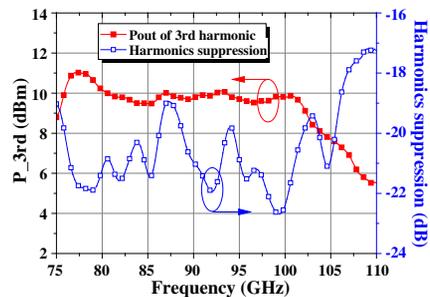
Figure 16. Measured output power and harmonics suppression.

Table 3. Comparison of the commercial products and reported prototypes.

Paper/Corp.	Millitech*	Quinstar	Hittite
Frequency multipliers	×6 (active)	×3	×3
Module Number	AMC-10-RFH00	QPM-W	HMC-XTB110
Devices	Varistor diode	Varistor diode	GaAs Schottky diode MMIC
Output Frequency (GHz)	75 ∼ 110	75 ∼ 110	70 ∼ 90
Output Power(dBm)	5 ∼ 11	−2 (typ)	−8 ∼ −5
Input Power (dBm)	10	20	13
Conversion Loss (dB)	−	22 (typ)	18 ∼ 21
Conversion efficiency (%)	−	1% (typ)	1.6% (max)
Paper/Corp.	M. Morgan [23]	H. Wang [24]	This work
Frequency multipliers	×3	×3	×3
Module Number	−	−	−
Devices	BES Schottky diode	BES Schottky diode	UMS DBES105a
Output Frequency (GHz)	75 ∼ 110	75 ∼ 98	75 ∼ 110
Output Power (dBm)	−3.7 ∼ 2	−5 (min)	5.5 ∼ 11
Input Power (dBm)	19	14 ∼ 18	27
Conversion Loss (dB)	17 ∼ 22.7	12.6 ∼ 21	16 (typ)
Conversion efficiency (%)	2% (max)	5.5% (max)	3% (typ)

*Note. AMC-10-RFH00 is an active frequency sextupler, its conversion loss and efficiency can not be found from its datasheet.

4. CONCLUSION

A W-band solid-state passive frequency tripler with the characteristics of broadband and high output power has been designed and tested. The scheme of in-phase power combining is adopted to increase the power handling capability of the frequency tripler. A reliable design and simulation method is implemented in this work to predict the performance of the tripler. A peak conversion efficiency of 3.8% is obtained at 97 GHz. With the input power of 27 dBm, $5.5 \sim 11$ dBm of saturated output power is produced across the 75–110 GHz band. Suppression of undesired harmonics is greater than 17 dB. Measured results agree well with the simulation.

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