Progress In Electromagnetics Research C, Vol. 34, 99–109, 2013

A TRIPLE-MODULUS FREQUENCY DIVIDER WITH EMBEDDED SWITCHES IN 90-NM CMOS PROCESS

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Abstract—A high-speed triple-modulus frequency divider (FD) is designed and fabricated in a 90-nm CMOS process. With three pairs of nMOS switches inserted in the signal paths of the regenerative divider, the FD can offer three selectable division ratios of 1/2, 1/3, and 1/4. The corresponding behavior model of the proposed divider is utilized to explain the operation principle and analyze the locking range. From the experimental results, the divider consumes 6.8 mW of dc power from a 1.2-V supply voltage, and the locking ranges for the 1/2, 1/3, and 1/4 divide modes are 16–23.8, 12.3–18, and 16.8–22.8 GHz, respectively. The maximum input frequencies of 23.8, 18, and 22.8 GHz for the 1/2, 1/3, and 1/4 division modes are demonstrated that the divider is attractive for application to a frequency synthesizer.

1. INTRODUCTION

Multi-modulus frequency divider (MMFD) is an important component in the frequency synthesizer. It is used for frequency translation with the voltage-controlled oscillator (VCO) [1–3] and designed to be controllable to synthesize the desired output frequencies [4] or synchronize the clock signals [5, 6]. Accordingly, MMFD demands high-speed operation, wide frequency range, and low-power consumption for application to a high performance frequency synthesizer. Several high-speed MMFDs have been published in [7–11]. Their topologies are mainly focused on the phase-switching technique [7, 8] and the injection-locked oscillator [9–11]. There is

Received 11 September 2012, Accepted 25 October 2012, Scheduled 31 October 2012

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rarely discussion on the regenerative divider to generate multi-division ratios. Conventional regenerative frequency divider (RFD) can operate at high frequency with a wide locking range, but it only generates single division ratio [12–14]. This is because the corresponding topology is restricted to a single type of a positive feedback circuit.

In order to overcome the topology limitation of the conventional regenerative divider, three pairs of nMOS switches are used in the regenerative divider. These switches generate a switchable path between a regenerative divider and a current-mode logic (CML) divider; therefore, the proposed divider can offer three division modes of 1/2, 1/3 and 1/4. Furthermore, the divider in these modes still achieves wide locking ranges and low power consumption. The divider's equivalent models and the circuit design are described in the following section. The analysis of the locking range is also given.

2. CIRCUIT DESIGN

The block diagram of the proposed triple-modulus FD is shown in Fig. 1, which consists of RF mixer, bandpass filter (BPF), three switches (SW_1–SW_3), ÷2 CML FD, and output buffer. The circuit schematic of the proposed divider is shown in Fig. 2. A Gilbert cell is used in the topology of the RF mixer. The inductors L_1 and L_2 resonate with the parasitic capacitance of M_3 to M_6 at the mixer IF port, which provides the bandpass filtering function to suppress high-frequency mixing components. Three pairs of nMOS switches (SW_1–SW_3) are inserted between the BPF and the ÷2 CML divider. Each pair of switch consists of two nMOS transistors with the gates connected to the DC control signal (ø). The ÷2 CML FD includes a CML pair with a cross-connection between the output of the second-stage cross-coupled pair and the input of the first-stage differential pair. The output buffer uses a two-stage differential amplifier to drive the measurement equipment.

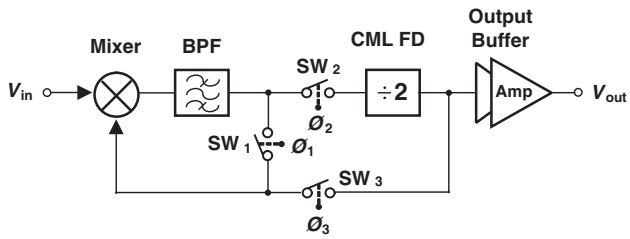

Figure 1. Block diagram of the proposed triple-modulus frequency divider.

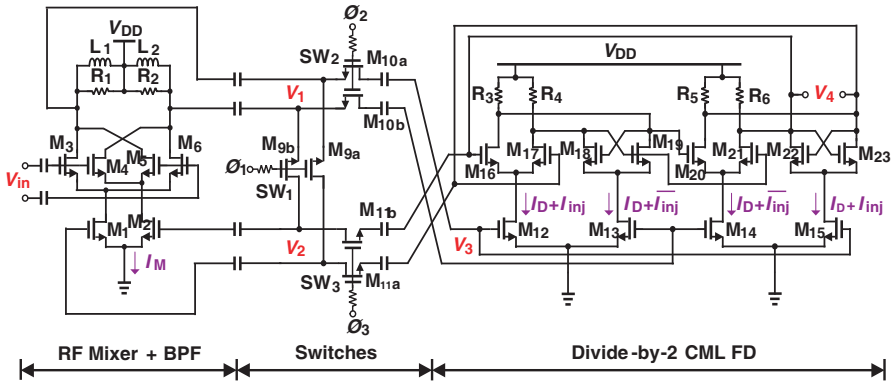

Figure 2. Circuit schematic of the proposed divider.

The division mode is selected by setting the switches (SW_1–SW_3) to either the open or short state. If SW_1 and SW_3 are both in the short state and SW_2 is in the open state, the topology of the proposed divider becomes a divide-by-two Miller FD. If SW_1 is opened and SW_2 is shorted, the circuit works as a divide-by-three RFD. Finally, if SW_1 and SW_2 are shorted and SW_3 is opened, the circuit is equivalent to a divide-by-two Miller divider in series with a CML FD, which provides a divide-by-four function.

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Figure 3 shows the behavior model of the proposed divider where Z_{S1}, Z_{S2}, and Z_{S3} represent the on-state impedances of the SW_1, SW_2, and SW_3, respectively. Z_{RF}, Z_{CML}, and Z_{BUF} are the input impedance of the mixer's RF stage, the CML FD, and the output buffer, respectively. Fig. 3(a) shows the ÷2 behavior model while the SW_1 and SW_3 are in the on state. The model can be equivalent to a Miller FD, and its locking range is determined by the frequency range where the loop gain exceeds one [13]. The loop gain of the ÷2 model can be described as

$$\frac{\beta}{2}\frac{|V_{\mathrm{in}}|\,|H(\omega)|}{|1+Z_{S1}\,[Z_{\mathrm{RF}}//\,(Z_{S3}+Z_{\mathrm{BUF}})]|}>1. \tag{1}$$

where β is the mixer conversion factor, and $H(\omega)$ is the frequency response of the BPF. Consequently, the single-side band of the locking range $\Delta\omega$ can be written as

$$\frac{\Delta\omega}{\omega_o} < \frac{1}{2Q}\sqrt{\left\{\frac{\beta}{2}\frac{R_o|V_{\text{in}}|}{|1+Z_{S1}\left[Z_{\text{RF}}//\left(Z_{S3}+Z_{\text{BUF}}\right)\right]|}\right\}^2 - 1}. \tag{2}$$

where Q is the quality factor of the BPF, R_o the parallel resistance of the BPF, and ω_o its resonant frequency.

Figure 3(b) shows the $\div 3$ behavior model while the SW_2 and SW_3 are in the on state. It can be equivalent to a $\div 3$ regenerative FD, and its operation range depends on the locking range of the CML loop divider [14]. The CML divider can be modeled as an injection-locked ring oscillator with a differential input signal applied to the CML input stage [15]. Thus the injection current is added into the differential pair's and the cross-coupled pair's bias currents with the opposite phase. Using similar approach in [16] to analyze the circuit, the minimum required injection current to lock the output frequency of the CML ring oscillator at half of injection frequency can be derived as

$$|I_{\text{inj}}| \geq \frac{3}{2}I_D\frac{\left|\frac{\omega_{\text{inj}}}{\omega_{\text{osc}}}-1\right|}{\sqrt{1+\left(\frac{\omega_{\text{inj}}}{\omega_{\text{SRF}}}\right)^2}}. \tag{3}$$

where ω_{inj} is the injection frequency, ω_{SRF} the self-resonant frequency, and I_D the bias current of the differential pair and the cross-coupled pair. On the other hand, the amplitude of V_3 at $2\omega_{\text{in}}/3$ can be written as

$$|V_3| = \frac{\beta}{2}|V_{\text{in}}||V_4||H(\omega)|\frac{|Z_{\text{RF}}|}{|Z_{S3}+Z_{\text{RF}}|}\frac{|Z_{\text{CML}}|}{|Z_{S2}+Z_{\text{CML}}|}. \tag{4}$$

Thus the injection current I_{inj} at $2\omega_{\text{in}}/3$ can be given by

$$|I_{\text{inj}}| = g_m|V_3|. \tag{5}$$

where g_m is the transconductance of the CML input stage. Therefore, the locking range of the $\div 3$ mode is within the value of I_{inj} in (5) larger than (3).

Figure 3(c) shows the $\div 4$ behavior model while SW_1 and SW_2 are in the on state. The model can be equivalent to a $\div 2$ Miller FD in series with a $\div 2$ CML FD. Its operation range is determined by the locking range of the Miller divider and the frequency range where the Miller divider's output signal can be injection-locked the CML divider. The locking range of the Miller FD is still determined by the loop gain

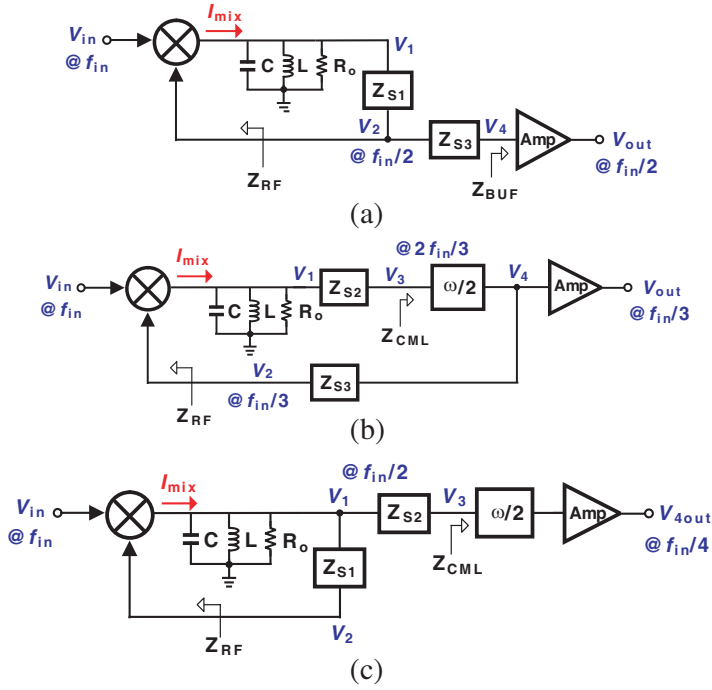

Figure 3. Equivalent behavioral model of the proposed FD. (a) ÷2 mode. (b) ÷3 mode. (c) ÷4 mode.

limitation, and it can be derived as

$$\frac{\Delta\omega}{\omega_o} < \frac{1}{2Q}\sqrt{\left(\frac{\beta}{2}R_o\left|V_{\text{in}}\right|\frac{\left|Z_{\text{RF}}\right|}{\left|Z_{S1}+Z_{\text{RF}}\right|}\right)^2 - 1}. \tag{6}$$

In addition, if the Miller divider works, the amplitude of the output signal V_1 at $\omega_{\text{in}}/2$ can be expressed as [12]

$$\left|V_1\right| = \frac{16}{3\pi^2}I_m\frac{R_o}{\sqrt{1+Q^2\left(\frac{\omega-\omega_o}{\omega_o}\right)^2}}. \tag{7}$$

where I_M is the bias current of the mixer. Therefore, the amplitude of V_3 can be given by

$$\left|V_3\right| = \frac{16}{3\pi^2}\left|V_1\right|\frac{\left|Z_{\text{CML}}\right|}{\left|Z_{S2}+Z_{\text{CML}}\right|}. \tag{8}$$

Substituting (8) into (5), the injection current I_{inj} at $\omega_{\text{in}}/2$ can be found. As explained before, if the value of I_{inj} is large than (3), the CML divider can be injection-locked.

3. CIRCUIT IMPLEMENTATION AND RESULTS

An Agilent ADS corresponding to a Taiwan Semiconductor Manufacturing Company (TSMC) design kit was employed for circuit simulation. The full-wave EM simulation is implemented in ADS momentum. These individual components were combined in a harmonic balance simulator to optimize the divider's performance. The fabricated FDs were attached to the carrier plates for testing. The measurement signals were provided by the coplanar 100-μm pitch GSGSG on a wafer probes measurement system that is based on Agilent E8257D signal generator and E4446A spectrum analyzer.

The proposed FD was fabricated in a TSMC 90-nm CMOS process with a total chip area of $0.81 \times 0.8\,\mathrm{mm}^2$ as the chip micrograph shown in Fig. 4. The FD operates at a 1.2 V of supply voltage. The power consumption of the core circuit and the output buffer is 6.8 and 21 mW, respectively. The dc control voltage of 0 V and 1.2 V are applied to the gate of the nMOS switches to control their operation states and change the divider in the different division modes.

Figure 5 shows the measured output spectrum with applying 2-dBm input power to the divider. Fig. 5(a) shows while the divider works in the ÷2 mode and $f_{\mathrm{in}} = 23.8\,\mathrm{GHz}$, the output power is $-12\,\mathrm{dBm}$ at 11.9 GHz. Fig. 5(b) shows that a $-10\,\mathrm{dBm}$ of the output signal at 6 GHz is obtained when $f_{\mathrm{in}} = 18\,\mathrm{GHz}$, and in the ÷3 mode. Fig. 5(c) shows that the output power of $-6.9\,\mathrm{dBm}$ at 5.7 GHz is also measured when $f_{\mathrm{in}} = 22.8\,\mathrm{GHz}$, and in the ÷4 mode. Fig. 6 shows the

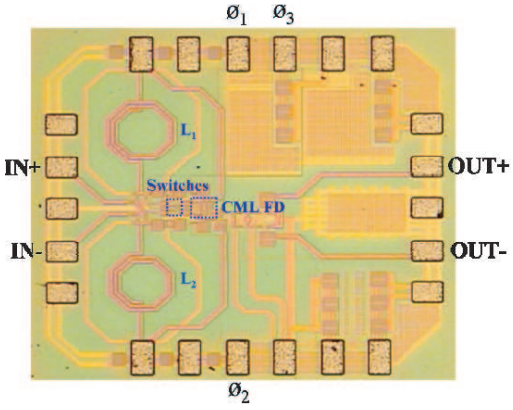

Figure 4. Microphotograph of the fabricated triple-modulus frequency divider. The overall chip dimension including the contact pads is $0.64\,\mathrm{mm}^2$.

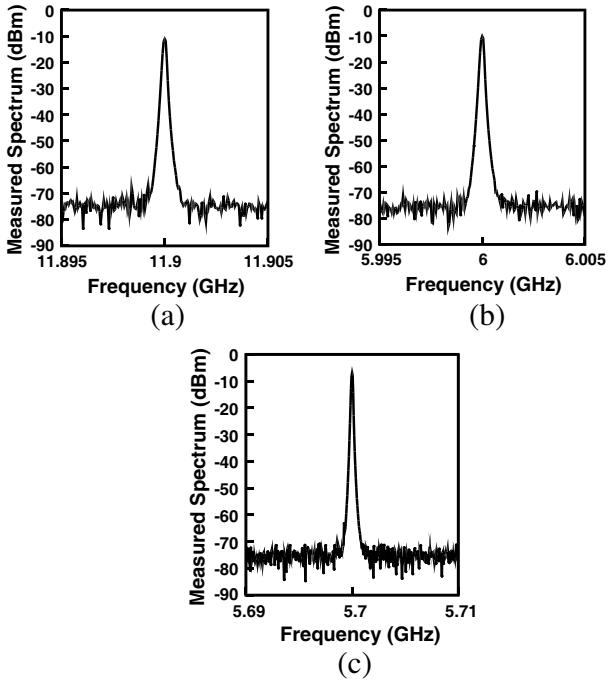

Figure 5. Measured output spectrum with $P_{\text{in}} = 2\,\text{dBm}$. (a) $f_{\text{in}} = 23.8\,\text{GHz}$ and in the $\div 2$ mode. (b) $f_{\text{in}} = 18\,\text{GHz}$ and in the $\div 3$ mode. (c) $f_{\text{in}} = 22.8\,\text{GHz}$ and in the $\div 4$ mode.

theoretical and measured input sensitivities. The theoretical results are tuned to fit the measured ones by estimating the Q value of BPF and $R_o(\beta/2)$ as 9 and 2.5, respectively. Fig. 6(a) shows that when the divider works in the $\div 2$ and $\div 4$ modes, the measured locking range is 16–23.8 and 16.8–22.8 GHz, respectively. If the divider works in the $\div 3$ modes, the measured locking range is 12.3–18 as shown in Fig. 6(b). It can be seen that the experimental upper and lower bounds of the locking range deviate from the theoretical ones. This is because the actual Q and β values vary at different frequencies. On the other hand, the measured locking range of the $\div 3$ mode is narrowest compared with other ones. The reason is that the feedback loop of the $\div 3$ mode includes two switches' conducting impedances, Z_{S2} and Z_{S3}, in the signal path. The two conducting impedances will deteriorate the total loop gain and result the $\div 3$ mode in a narrowest locking range. However, the locking range can be improved in use of a switch with low-conducting impedance.

Figure 7 shows the measured phase noise of the divider and the

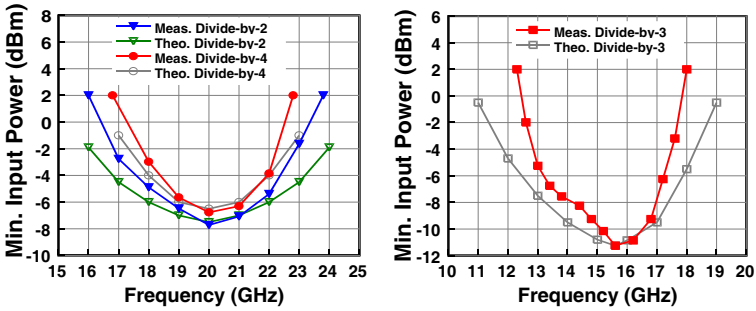

Figure 6. Comparison of the input sensitivity between theory and measurement. (a) ÷2 and ÷4 modes. (b) ÷3 mode.

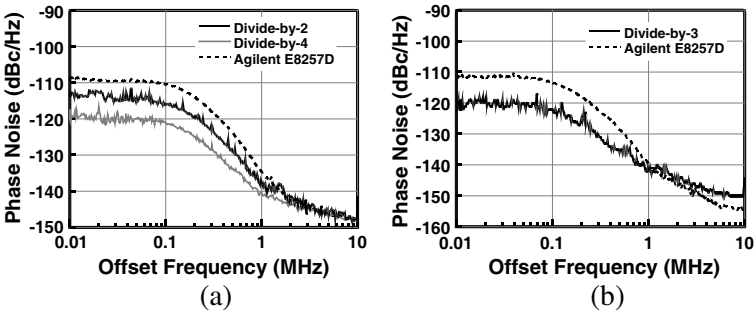

Figure 7. Measured phase noise with $P_{\text{in}} = 2\,\text{dBm}$. (a) $f_{\text{in}} = 21\,\text{GHz}$ and in the ÷2 and ÷4 modes. (b) $f_{\text{in}} = 15\,\text{GHz}$ and in the ÷3 mode.

external injected signal from Agilent E8257D with $P_{\text{in}} = 2\,\text{dBm}$. As shown in Fig. 7(a), while $f_{\text{in}} = 21\,\text{GHz}$, the phase noise at 0.1 MHz offset frequency follows that of the external signal with a 5.7 and 11.1 dB reduction for the ÷2 and ÷4 modes, respectively. Fig. 7(b) shows that if $f_{\text{in}} = 15\,\text{GHz}$, and in the ÷3 mode, the phase noise at 0.1 MHz offset frequency is lower than 8.6 dB compared to that of the external injected signal. As observing the measured phase noise, the noise degradations of the ÷2, ÷3, and ÷4 modes are close to the theoretical values of 6, 9.5, and 12 dB estimated for the frequency division by 2, 3, and 4 [17].

The performance comparisons with published multi-modulus FDs are summarized in Table 1 [6–10]. The proposed divider uses the switches to select the triple division modes and retains the characteristic of the RFD with a high-speed operation and wide locking range. The proposed work presents significant advantages such as a

Table 1. Comparison of reported CMOS multi-modulus frequency dividers.

Ref.	[7]	[8]
Technology	0.18-µm CMOS	0.09-µm CMOS
Division Ratio	6/7/8	6/7
P_{in} (dBm)	0	< 10
Locking Range (GHz)	8.6–16	18.6–22.8
VDD (V)	1.8	1.2
$P_{\text{diss.}}$ (mW)	40	6.7
Chip size (mm^2)	0.04^+	0.005^+
Ref.	[9]	[10]
Technology	0.18-µm CMOS	0.18-µm CMOS
Division Ratio	2/4	2/3/4
P_{in} (dBm)	$< 5/< 0$	0
Locking Range (GHz)	13–25/30–45	7.7–11.5/14–15.5/18.9–20.2
VDD (V)	1.8	1.4/1.4/1.5
$P_{\text{diss.}}$ (mW)	< 24	9/9/10
Chip size (mm^2)	0.003^+	0.4
Ref.	[11]	This work
Technology	0.13-µm CMOS	0.09-µm CMOS
Division Ratio	2/4/6/8	2/3/4
P_{in} (dBm)	$< 2/< 5/< 10/15$	< 2
Locking Range (GHz)	4–6/9–11/14.6–15.3/19.8–20	16–23.8/12.3–18/16.8–22.8
VDD (V)	2	1.2
$P_{\text{diss.}}$ (mW)	< 12.5	6.8
Chip size (mm^2)	0.29	0.64

+ Active area of the core circuit.

high-speed and wide operation range, and low power consumption, as compared to previously reported works.

4. CONCLUSION

A high-speed triple-modulus FD is presented using a 90-nm CMOS process. Given three pairs of nMOS switches into the regenerative divider, the proposed divider achieves not only $\div 2$, $\div 3$, and $\div 4$ division functions but also obtains wide locking ranges and low power consumption. Based on the measurement results, the divider exhibits wide locking ranges of 16–23.8, 12.3–18, and 16.8–22.8 GHz in the $\div 2$,

÷3, and ÷4 division functions, respectively while consuming low power of 6.8 mW from a supply voltage of 1.2 V.

ACKNOWLEDGMENT

This work was supported in part by the National Chip Implementation Center, National Applied Research Laboratories, and the National Science Council of Taiwan under contracts NSC 99-2218-E-168-001, NSC-2221-E-006-141-MY3 and 100CC02.

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