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LOCALIZED DUAL-SIDE MUSHROOM GROUND PLANE STRUCTURE FOR THE SSN SUPPRESSION IN MULTI-LAYER PCBS

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Abstract—A novel dual-side mushroom ground plane (DMGP) structure is proposed for the noise suppression in high-speed multilayer printed circuit boards (PCBs). The proposed method is localized suppression technique where a dual-side mushroom structure is placed below the noise-sensitive device. In multilayer PCBs with DMGP, noise between two ports with large or small ports spacing can be minimized effectively, which is flexible for the layout of mixed-signal system. Wideband noise suppression is achieved for the fabricated boards even though the port spacing is only 3.5 mm.

1. INTRODUCTION

With the trend of high clock frequency and low voltage in high speed circuits, ground bounce noise has received many concerns in the past few years. In modern high-speed printed circuit boards (PCBs), noise will propagate within the power/ground planes when digital devices switch between high and low logical states (switching noise) or high-speed signals transit through the power/ground planes by signal vias (transition noise) [1].

Many methods have been developed to mitigate ground bounce noise [1–17]. Electromagnetic bandgap (EBG) structures [4–14] are the widely studied global topologies for the noise suppression. However, two ports should be separated by several unit cells for significant isolation level in EBG designs. Recently, localized suppression techniques have attracted the interest of some researches [15–17], which are the approaches of designing special structures around the

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two ports needed to isolate, such as designing patterns directly on power/ground planes [15, 16] and introducing mushroom-type ground plane (MGP) structure [17] around susceptible and aggressive devices. Although very low cutoff frequencies are achieved in [15] and [16], large inductances are introduced which may result in power handling problem [13, 17]. MGP is excellent for the suppression of noise excited between the patch of the mushroom and the top plane. Nevertheless, the isolation performance between the port inside localized structures and the port outside localized structures will be not so well in all the designs of [15–17].

Actually, a lot of signal vias and aggressive devices are around susceptible devices in multilayer PCBs, which can excite noise in any place of the PCBs. In fact, some noise sources could be very close to the noise-sensitive devices. Previous localized techniques are not effective to cope with the suppression of a large number of noise sources outside the localized structures, while EBG cannot suppress close range noise significantly. In this letter, we develop a novel dual-side mushroom-type ground plane (DMGP) structure to isolate the noise-sensitive devices from noise excited in any positions of the PCB and achieve close range and wideband noise suppression.

2. DESIGN CONCEPT

The proposed DMGP is composed of 1-via and n-via mushroom structures (named n-via DMGP) which are vertically cascaded with staggered vias, as depicted in Fig. 1(a). In order to minimize the metal layers of multilayer PCBs, the patches of mushroom can be etched on the asymmetrical signal layers (commonly multilayer asymmetrical striplines exist in one plane pair). Susceptible devices are placed between the patch of 1-via mushroom structure and the power plane. Due to the port placement technique of susceptible devices, the 1-via mushroom consists of a low-pass structure and the noise is suppressed significantly [17]. Meanwhile, owing to the small spacing between the patch of n-via mushroom and ground plane, a considerable capacitance is formed and combined with the inductance of vias to constitute a local high-frequency decoupling loop and further improve the high-frequency noise suppression. In Fig. 1(a), ports 1 and 2 represent the susceptible device and the noise excited between power/ground planes, respectively. Figs. 1(a) and (b) show the stack-up and corresponding geometrical parameters of a 9-via DMGP board, with $t1 = 0.05\,\text{mm}$, $h = 0.51\,\text{mm}$ and $d = 0.595\,\text{mm}$. The dielectric substrates are FR4 (ε_{r1}) and RCC65T (ε_{r2}) with a relative permittivity of 4.0 and 3.5 respectively.

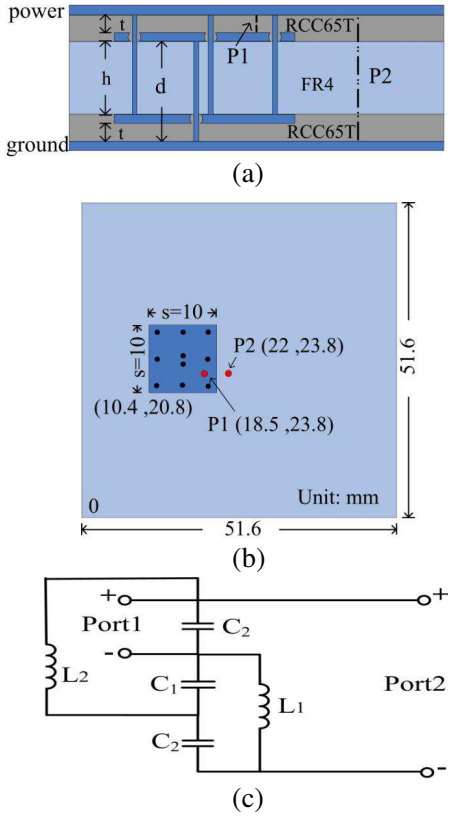

Figure 1. Proposed DMGP. (a) Side view of a 9-via DMGP. (b) Top view of a 9-via DMGP. (c) Simplified model.

In the multilayer PCBs with localized suppression structure, noise suppression mainly contributes to the localized structure. So, the cut-off frequency of multilayer PCBs with n-via DMGP can be approximately predicted by only considering the localized mushroom structure. Fig. 1(c) gives a simplified model of the proposed n-via DMGP for the prediction of cutoff frequency. C_1 is the capacitance between two patches of mushroom, and C_2 is the capacitance between power/ground plane and the patch of mushroom; L_1 and L_2 are the via inductances of 1-via and n-via mushroom. The values of these parameters are calculated by the following equations [14]:

$$C_1 = \frac{\varepsilon_0 \varepsilon_{r1} s^2}{h} \tag{1}$$

$$C_2 = \frac{\varepsilon_0 \varepsilon_{r2} s^2}{t} \tag{2}$$

$$L_1 = \frac{\mu_0 d}{2\pi}\left[\ln\left(\frac{2d}{r} + \sqrt{1+\left(\frac{2d}{r}\right)^2}\right) - \sqrt{1+\left(\frac{r}{2d}\right)^2} + \frac{r}{2d} + \frac{1}{4}\right] \tag{3}$$

$$L_2 = \frac{L_1}{n} \tag{4}$$

where ε_0 and μ_0 are the permittivity and permeability of free space, respectively; r is the radius of vias and n the via number of n-via mushroom.

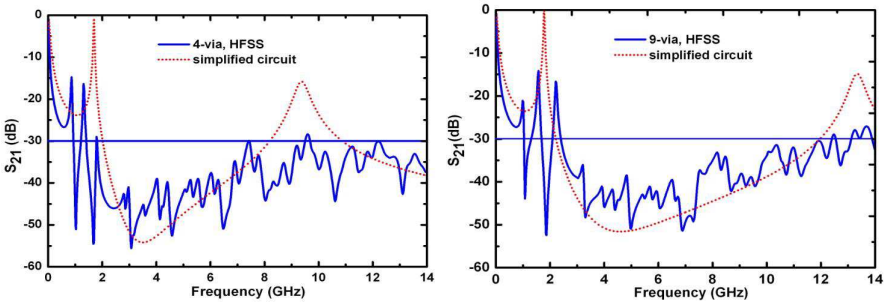

Figure 2. S_{21} of the 4-via DMGP and 9-via DMGP, simulated by HFSS and simplified circuits. (a) 4-via DMGP. (b) 9-via DMGP.

Figure 2 shows the S_{21} of 4-via and 9-via DMGP with geometrical parameters given in Fig. 1, simulated by HFSS and simplified circuits, respectively. The simplified circuit simulation can be quickly achieved by Agilent's Advanced Design System. As can be seen in Fig. 2, -30 dB cutoff frequency predicted by simplified circuit model is very close to the simulated HFSS results. In addition, the suppression level can also be approximately evaluated by the simplified circuit model. Since conductor loss and dielectric loss are not considered in the simplified model, the peak value of S_{21} of the circuit simulation is larger than that of HFSS results.

3. RESULTS AND DISCUSSION

To verify the performance of DMGP, a test board of Fig. 1 is fabricated. Two-port S-parameter measurement is carried out by using GSG microprobes, probe station and vector network analyzer (VNA). Fig. 3 plots the measured transmission coefficient between ports 1 and 2,

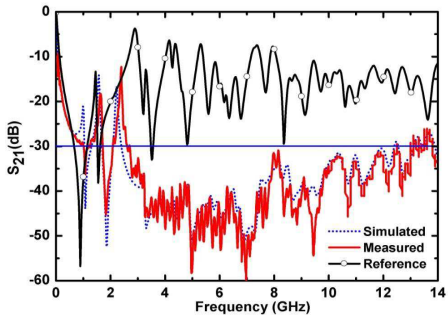

Figure 3. Simulated and measured transmission coefficients of 9-via DMGP.

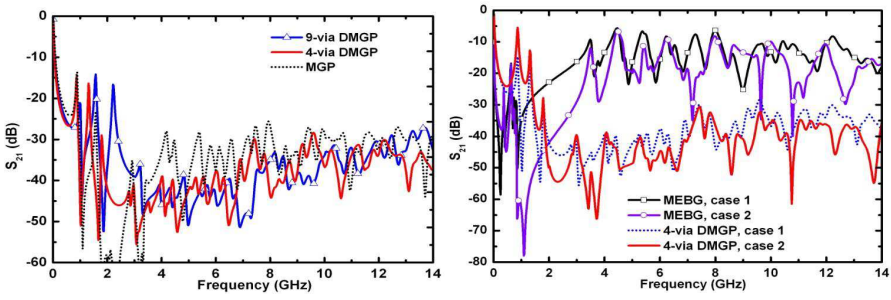

Figure 4. Simulated S_{21} comparison between n-via DMGP and other noise suppression techniques.

which agrees well with simulated HFSS result. The insertion loss of solid planes with same dimensions and FR4 substrate is also given for reference. Measured -30 dB noise suppression bandwidth is from 2.5 GHz to 12.5 GHz when the spacing between two ports is only 3.5 mm.

Simulated transmission coefficients of the same board dimensions with MGP and MEBG are compared with that of 4-via and 9-via DMGP, as shown in Fig. 4. Compared with MGP, significant improvement of noise suppression can be seen in Fig. 4(a) from 3 GHz to 7 GHz and to 8 GHz for the 4-via and 9-via DMGP, respectively. Fig. 4(b) shows the S_{21} of Mushroom-type EBG (MEBG) and 4-via DMGP with two cases of port positions. Two ports of case 1 are (18.5, 23.8) and (22, 23.8), while case 2 are (18.5, 23.8) and (33, 23.8). The patch size of MEBG is 10 mm$\times$10 mm with 5×5 unit cells. Case 2 of MEBG effectively suppresses the noise from 900 MHz to 3 GHz,

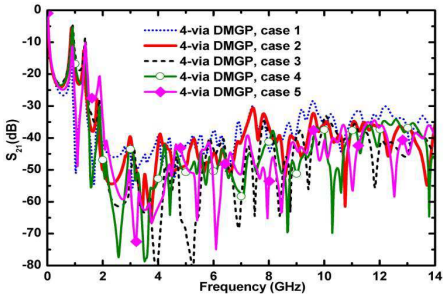

Figure 5. The effect of port position on transmission coefficient.

while case 1 is almost invalid for noise suppression since the port spacing is very small. On the contrary, 4-via DMGP can significantly minimize the noise from 2 GHz to 14 GHz and almost has the same suppression performance no matter how small the port spacing. Fig. 5 further investigates the influence of port position on noise suppression by changing the positions of port 2. Ports 2 of case 3, 4 and 5 are located at (40, 42), (30, 45) and (10, 12) respectively. As expected, noise suppression of DMGP is hardly affected by the port position. Thus, multilayer PCB with n-via DMGP is very flexible for the layout of the mixed-signal system.

4. CONCLUSION

In this letter, a novel localized DMGP is proposed for the noise suppression in multilayer PCBs. Unlike previous localized noise suppression topologies of designing two structures around the susceptible and aggressive devices respectively, only one n-via dual-side mushroom is placed below susceptible devices, and almost all the noise excited in every position of the board can be isolated from the port inside n-via DMGP. The measured -30 dB suppression bandwidth of the fabricated 9-via DMGP is from 2.5 GHz to 12.5 GHz which is consistent with the simulation.

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