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EXPERIMENTAL PERFORMANCE COMPARISON OF SIX-PORT AND CONVENTIONAL ZERO-IF/LOW-IF RECEIVERS FOR SOFTWARE DEFINED RADIO

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Abstract—This paper presents an experimental performance comparison among three RF architectures that are very suitable for Software Defined Radio (SDR) implementation: zero-IF, low-IF, and six-port network. A six-port receiver and a dual zero-IF/low-IF receiver have been developed for this purpose. Six-port receiver is a very promising and flexible RF architecture for the low-cost implementation of integrated microwave and millimeter-wave systems. Competitive advantages such as ultra-broadband behavior, low-cost, reconfigurability, and low power consumption, point to the six-port architecture as a good candidate to implement a SDR. However, two issues on broadband six-port receivers require intensive research: dynamic range extension, and miniaturization. In this paper, two solutions are proposed to solve these problems: the use of biased detector diodes for dynamic range extension, and the use of low temperature co-fired ceramic (LTCC) technology for six-port reduction. The measurement results indicate that the six-port receiver shows high potential benefits and advantages compared to conventional zero-IF and low-IF receivers. In addition, the capability of the six-port architecture to operate as both zero-IF and low-IF receivers has been experimentally demonstrated for the first time.

1. INTRODUCTION

Software Defined Radio (SDR) puts new challenges on radio-frequency (RF) architectures capable of handling several standards and related software implementations [1, 2]. Until now, conventional multi-band

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receivers have consisted of a different reception chain for each standard. This solution is not cost efficient, as it requires specific circuits for each standard, which increase the volume of the radio terminal. On the contrary, a SDR is composed of a single broadband reception stage. All channels are converted to digital domain with a high speed ADC (Analog to Digital Converter), and channel selection is performed by software defined filters. However, the design of a universal general-purpose broadband RF front-end, with multi-mode and reconfiguration features, is not a simple matter. Furthermore, the difficulty increases if other aspects such as volume or cost are also taken into account.

This paper presents a study of the three RF architectures with more possibilities to implement a SDR: zero-IF, low-IF, and six-port network. Since some theoretical [3–5] or simulation-based [6] studies have been published, this paper presents an experimental comparison based on measurement results. Two SDR receiver prototypes have been developed for this purpose: a broadband six-port receiver, described in Section 2, and a dual zero-IF/low-IF receiver, presented in Section 3. Some novel contributions have been introduced in the six-port receiver, which lead to clear benefits in the performance. The first novelty is the extension of the six-port dynamic range, due to a particular detector diode design. The second one is the miniaturization of six-port receivers by using the LTCC technology. Both are contributions of great interest, as they are related to the topics that are currently having more intensive research in six-port networks. Finally, the capability of the six-port receiver to operate as a low-IF receiver has been experimentally demonstrated for the first time.

2. OVERVIEW OF RF ARCHITECTURES FOR SDR

Nowadays, zero-IF and low-IF transceivers are thought to be a serious alternative to classical heterodyne systems for several applications, especially SDR, where high level of integration and low-cost solutions are required. The typical configuration of a zero-IF receiver is represented in Figure 1(a). It is a simple structure, where the RF signal is directly down-converted to zero frequency by means of an I-Q demodulator and a local oscillator (LO) of the same frequency [7]. Next, the I-Q components are low-pass filtered and converted to digital domain with an ADC. In a low-IF receiver, the RF signal is down-converted to an IF closed to zero, thereby its bock diagram — Figure 1(b) — is similar to the zero-IF one, with the exception of low-pass filters, which are here substituted by band-pass filters [8].

The zero-IF architecture comprises clear benefits with respect

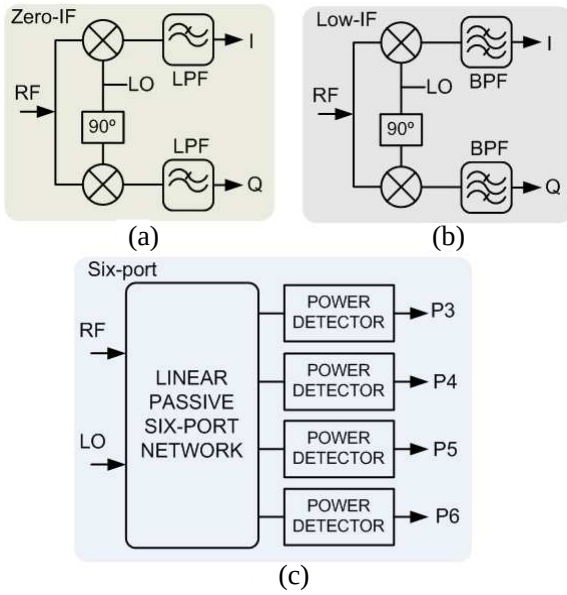

Figure 1. RF architectures for SDR (a) zero-IF, (b) low-IF, (c) six-port.

to the heterodyne. On the one hand, since IF is equal to zero, homodyne receivers does not suffer from the image frequency problem. Therefore, large costly image rejection filters and IF circuits can be eliminated. On the other hand, main operations such as channel selection and amplification are baseband performed, where integration is much easier. All these characteristics entail high level of integration, compact size, simplicity, low-power consumption, flexibility and system reconfigurability. However, this architecture has some important limitations, such as DC-offset, $1/f$ noise, I-Q imbalances, LO leakage, and second-order intermodulation distortion (IMD2) [7].

Low-IF architecture combines the advantages of zero-IF and heterodyne configurations [8]. It has zero-IF advantages such as low-cost, compact size, reconfigurability, and high level of integration, but it is not affected by DC-offset and flicker noise problems. However, the main drawback of the low-IF architecture is the image frequency. As the image frequency is located very closed to RF signal, no RF filters for image rejection can be used. Typical image suppression techniques consist in using image rejection architectures, such as the well known Hartley [9] or Weaver [10]. However, I-Q imbalances cause interference that can not be removed in later stages and so directly

decrease the image-reject capabilities of the front-end. For example, a relative voltage gain mismatch of 5% and a phase imbalance of 5° lead to an image rejection ratio (IRR) approximately equal to 26 dB. The fact is that, in practice, these architectures can hardly achieve an IRR above 40 dB. Therefore, very strict I-Q balance requirements are demanded for low-IF receivers, making difficult its implementation, especially for broadband applications. Furthermore, a low-IF receiver demands the double IF bandwidth compared with a zero-IF receiver, making the I-Q imbalance problem worse.

Moreover, the trend towards high data rates services will require larger bandwidths, which become possible at high frequencies. Nevertheless, I-Q mod/demodulators need a nearly perfect 90° phase shift between their I-Q paths, which cannot be guaranteed over a very broad bandwidth. Therefore, the use of zero-IF and low-IF architectures is limited by these devices.

Six-port network architecture is an innovative and interesting alternative, as it does not use I-Q mixers for the frequency conversion. It is composed of a linear and passive six-port junction, and four power detectors, as shown in Figure 1(c). The principle of operation of the six-port receiver is based on the measurement of four independent powers, when the LO and RF signals are introduced into the remaining two ports [11]. The original I-Q components can be regenerated from these four power observations and some calibration constants, depending on system response. It is also possible to recover the original signal from three power measurements, leading to a five-port receiver [12, 13].

The main characteristic of the six-port architecture is its extremely large bandwidth, which involves multi-band and multi-mode capabilities. Six-port networks can operate at very high frequencies, being a serious alternative for millimetre-wave frequencies and large relative-bandwidth applications. Furthermore, the six-port architecture can perform high data rates, and it can operate with low values of LO power. These and other advantages make this architecture to be considered a good candidate to implement a SDR.

However, some limitations must be taken into account. Six-port receivers are typically direct conversion receivers, hence they suffer from the well known zero-IF problems. In addition, two (or one in a five-port configuration) additional ADCs and a calibration process is required to recover the original I-Q components. The large dimensions of the passive six-port structure, especially for operating frequencies in the lower gigahertz region and broadband designs, is also an important limitation. In fact, the miniaturization of six-port receivers is the focus of current work. Another key topic in six-port architectures that needs

intensive research is the extension of the dynamic range. Multi-port architectures are said to present worse behavior as for dynamic range compared to conventional homodyne and heterodyne architectures, as a consequence of the detector diode limitations. The reason is that all six-port implementations use zero-bias detector diodes. In this paper, it will be demonstrated that the use of a bias current has significant benefits in the dynamic range extension.

3. SIX-PORT RECEIVER PROTOTYPE

The objective is to develop a reconfigurable radio front-end for broadband mobile applications. Nowadays, the aim of a SDR for mobile applications can be reduced to receive every standard up to 6 GHz, as all cellular and WLAN (Wireless Local Area Network) communications are located in that frequency range. Consequently, a 698–5850 MHz six-port receiver prototype has been designed. The receiver can operate with broadband RF signals, up to 100 MHz-wide RF signals, and different modulation schemes [14].

The block diagram of the SDR six-port receiver is presented in Figure 2. It comprises a linear and passive six-port network, four power detectors, four low-pass filters (LPF), four video amplifiers, and four high-pass filters (HPF) for DC-offset rejection. The six-port network is composed of three 90-degrees hybrid couplers and a Wilkinson power divider. This is a typical six-port configuration, where output signals are combinations of the input RF and LO signals with relative phase shifts of 0, $\pi/2$, $-\pi/2$, and π rad. The RF band-pass filter, the LNA (*Low Noise Amplifier*), and the AGC (*Automatic Gain Control*) stage have not been included in the prototype, although these components would be necessary in an industrial SDR front-end.

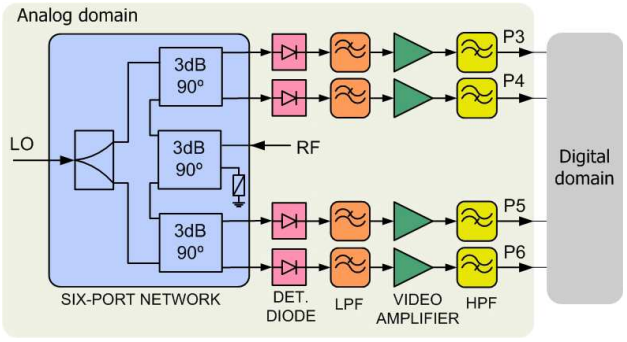

Figure 2. Block diagram of the six-port receiver.

The photograph of the fabricated six-port receiver prototype can be seen in Figure 3. One of the most critical parts of the design has been the 90-degrees hybrid coupler, as it has to cover a three octave bandwidth (698–5850 MHz). This has been achieved through the tandem connection of two seven-section 8.34 dB couplers, implemented with broadside-coupled striplines (Figure 4). Its maximum measured phase and amplitude imbalances are 4° and 1.2 dB over the entire frequency range. The power divider is the LYNX-111.A0214, whose characteristics are: 0.5–6 GHz frequency range, 0.8 dB insertion loss, 18 dB isolation, ±0.2 dB amplitude imbalance, and ±3° phase imbalance. A detailed description of the constructed six-port network is presented in [15].

The remaining components are implemented in microstrip technology with the $\varepsilon_r = 2.17$ Cu-clad substrate. The power detectors are implemented with the HP DC biased HSMS-286 Schottky diode. Mini-Circuits RLP-50+ and MAR-8A+ components are used for the low-pass filter and video amplifier, respectively. The high-pass filter is implemented with a series capacitor (1 kHz cutoff frequency).

The demodulation capability of the developed six-port receiver has been experimentally demonstrated over a four-octave bandwidth (0.3–6 GHz) [14]. The demodulation of up to 15.625 Msymbol/s signals, i.e., 93.6 Mbps for 64-QAM, has been satisfactorily performed, with high quality of the demodulated signal.

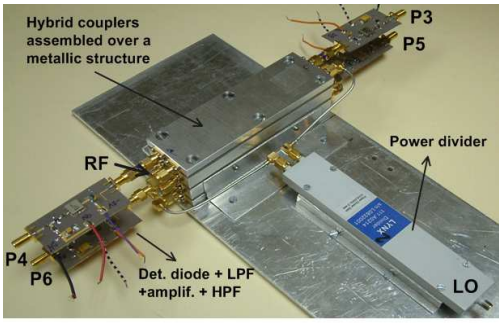

Figure 3. Fabricated six-port receiver prototype.

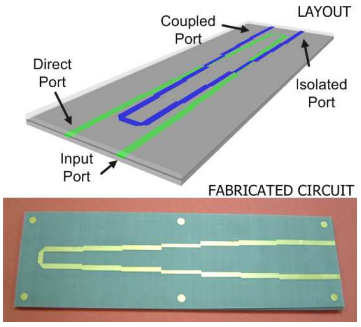

Figure 4. 3-dB tandem coupler.

3.1. Wide Video Bandwidth and High Dynamic Range Detector Design

One of the key points has been the design of the power detector. Our system specifications impose large RF operating range (698–5850 MHz) and a wide video bandwidth (50 MHz). Obviously, such a detector will not have high voltage sensitivity, since sensitivity and video bandwidth are competitive parameters. The detector voltage sensitivity, β_v, assuming a perfect lossless impedance match at the diode's input, can be expressed as [16]

$$\beta_v = \frac{0.5R_L}{(I_S+I_B)\cdot(R_V+R_L)\cdot(1+R_S/R_j)\cdot[(1+R_S/R_j)+(\omega C_j)^2 R_S R_j]} \quad (V/W) \tag{1}$$

where R_L is the video load resistance, I_B the externally applied bias current, I_S the saturation current, R_j and C_j the junction resistance and capacitance, R_S the parasitic series resistor, and $R_V = R_j + R_S$ the video resistance. R_j depends on bias current as follows:

$$R_j = \frac{nkT}{q(I_B + I_S)} \tag{2}$$

where T is the temperature in K, $q = 1.6021917 \cdot 10^{-19} C$ the electron charge, n the diode ideality factor, and $k = 1.38 \cdot 10^{-23}$ Joule/K the Boltzmann's constant. The voltage sensitivity is a parabolic-type function with $I_T = I_S + I_B$, whose maximum value at any particular frequency is given by

$$I_{T,opt} = \frac{\omega C_j}{\alpha}\sqrt{\frac{R_S}{R_L}} \tag{3}$$

where $\alpha = q/nkT$. For highest sensitivity, one requires $R_S \ll R_j$ and $R_L \gg R_j$. For currents greater than $I_{T,opt}$, β_v drops due to the reduced voltage across the diode junction. For currents less than $I_{T,opt}$, R_j gets large relative to R_L (note that R_j increases as I_B decreases), and the voltage sensitivity is reduced due to the $R_L/(R_L+R_V)$ voltage divider. For example, the measured data provided by the manufacturer show an optimal bias current of $I_{T,opt} = 5\,\mu$A for the HSMS-286B diode at 2.45 GHz and a load resistance $R_L = 100\,\text{k}\Omega$.

Consequently, conventional Schottky diode detectors use large load resistance and small bias current in order to maximize voltage sensitivity. Under such conditions, nevertheless, it is not possible to achieve very wide video bandwidths. In effect, the limit on the upper 3 dB cut-off frequency is given by:

$$f_{c3\,\text{dB}} = \frac{1}{2\pi R_T C_b} \tag{4}$$

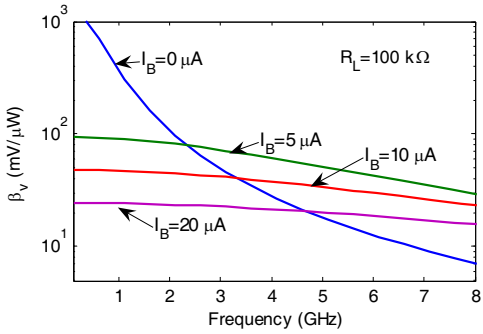

Figure 5. Theoretical detector diode voltage sensitivity, HSMS-286B.

where $R_T = R_V \cdot R_L/(R_V+R_L)$, and C_b is the bypass capacitor required to provide the RF short circuit at the diode output. Therefore, if the video bandwidth is wanted to be maximized, a high load resistance will call for a high value of bias current to reduce R_V and minimize R_T. Detector design is a compromise between video bandwidth and RF sensitivity.

In our case, the maximization of voltage sensitivity is not possible due to the wide video bandwidth requirement (50 MHz). In effect, a bias current higher than that required for maximum voltage sensitivity ($I_{T,opt}$) is needed to achieve the required video bandwidth. However, the use of a bias current involves some advantages especially suitable for SDR: reduction of the voltage sensitivity variation with frequency and temperature, simplification of the RF matching circuit, and extension of the square law dynamic range.

For a typical diode with no bias, the voltage sensitivity shows a strong dependence on frequency. Biasing the diode reduces the variation in voltage sensitivity, as shown in Figure 5, where the theoretical HSMS-286B diode voltage sensitivity is plotted for $R_L = 100\,\mathrm{k}\Omega$. However, it results in a voltage sensitivity reduction at the lower frequencies. The diode voltage sensitivity also varies with temperature, due to the dependence of the junction resistance with temperature. Again, the addition of a bias current reduces this variation in voltage sensitivity [16]. Moreover, the addition of a bias current reduces the diode quality factor, which reduces the complexity of the RF matching circuit. This can be seen from Figure 6, where the HSMS-286 diode input impedance is plotted for different values of bias current. These advantages are very important for a SDR, taking into account the wide RF bandwidth requirements (three octave RF bandwidth in our design).

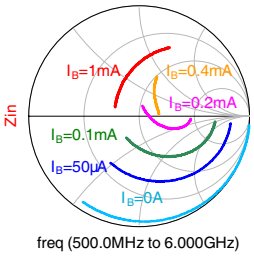

Figure 6. HSMS-286 diode input impedance.

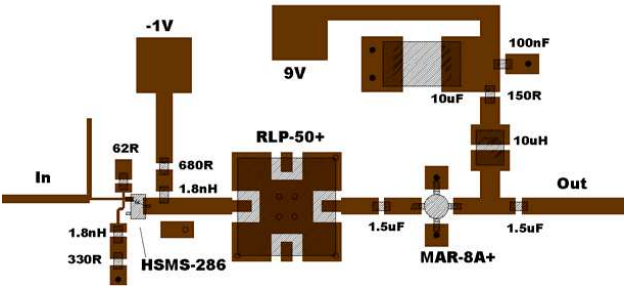

Figure 7. Layout of the circuit composed of the detector diode and the baseband components.

However, when a bias current is used, there is a trade-off in tangential signal sensitivity (TSS) and square law dynamic range [17]. The square law dynamic range can be defined as the difference between the power for 1 dB deviations from the ideal square law response (compression point) and the power input corresponding to the TSS. The compression level can be raised by increasing the bias current, although this degrades the TSS. However, the improvement in compression exceeds the TSS degradation, hence square law dynamic range is increased [16, 17]. A significant dynamic range increment is achieved with high bias currents, as it can be seen in [17].

Therefore, since the maximization of voltage sensitivity is not possible due to the wide video bandwidth requirement, a high bias current has been selected in order to extend the dynamic range: $I_B = 1\,\text{mA}$. As mentioned above, such a high current will provoke large voltage sensitivity degradation, whereby the video amplifier has been included. A shunt $62\,\Omega$ resistor is also used to give broadband input match, but at the expense of detection voltage sensitivity. The layout of the circuit composed of the detector diode and the baseband components is presented in Figure 7.

It is worth to mention that all previously reported six-port receivers use zero-bias detector diodes, matched at narrow band and/or with small video bandwidth. Consequently, no many experimental six-port demodulation results providing both multiband and high-data rate operation have been published up to now. This is the reason why multiport receivers have been traditionally said to have average dynamic range performance. However, it will be demonstrated that the use of a bias current has significant benefits in the dynamic range extension.

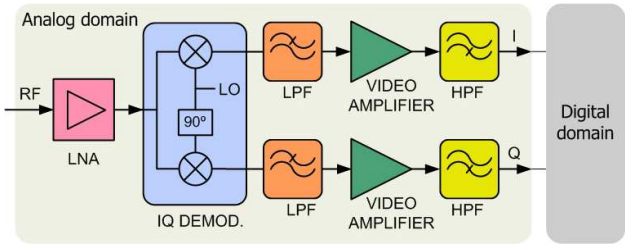

Figure 8. Block diagram of the zero-IF/low-IF receiver.

4. ZERO-IF/LOW-IF RECEIVER PROTOTYPE

As the block diagrams of zero-IF and low-IF configurations are quite similar, a single receiver prototype for both architectures has been developed. The zero-IF/low-IF receiver has been designed to cover the frequency range from 2.5 GHz to 2.69 GHz. The baseband bandwidth can be selected up to 20 MHz. The block diagram of the implemented receiver prototype is shown in Figure 8. The RF signal is amplified by a LNA, and then it is introduced into an I-Q demodulator. A low-pass filter, a video amplifier and a high-pass filter for DC-offset cancellation are located at each output. The RF band-pass filter, and the AGC stages have not been included in the prototype, although these components would be necessary in an industrial SDR front-end.

The prototype, presented in Figure 9, has been implemented in microstrip technology ($\varepsilon_r = 2.17$ Cu-clad substrate). The LNA is the Mini-Circuits PMA-545+ model, and the LT5575I-Q is used for the I-Q demodulator. The bandwidth of the low-pass filter, (SXLP-21.4+ Mini-Circuits) is 22 MHz. Notice that for the zero-IF architecture, a 10 MHz low-pass filter is sufficient to receive 20 MHz-wide channels, but the low-IF receiver requires double bandwidth for the IF stage. The video amplifier is the MAR-8A+. DC-offset cancellation, needed for zero-IF, is achieved by means of high-pass filtering with a series capacitor (1 kHz cut-off frequency).

5. MEASUREMENT RESULTS

The experimental comparison of the developed receiver prototypes will be presented in this section [18]. The configuration of the test-bench is represented in Figure 10. The Agilent E4438C ESG Vector Signal Generator (VSG) generates the RF modulated signal. The local oscillator is the Agilent synthesized sweeper 83752A. Both generators are phase locked. The output signals of the receiver are acquired by

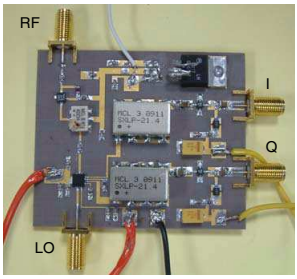

Figure 9. Fabricated zero-IF/low-IF receiver prototype.

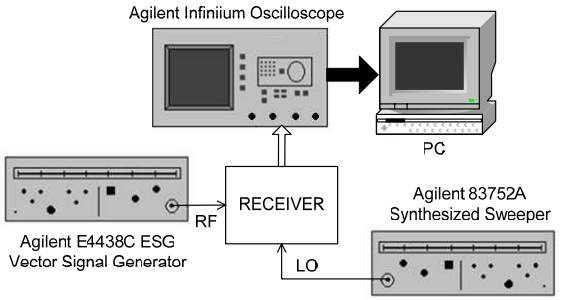

Figure 10. Measurement test-bench.

the Agilent Infiniium Oscilloscope with an over-sampling ratio $OSR = 8$. The software, implemented in Matlab, is applied in a personal computer to regenerate the I-Q components of the original signal. For the six-port receiver calibration, it has been used the conventional six-port auto-calibration method based on training sequence described in [12–19]. The quality of the demodulated signal will be measured in terms of the EVM (Error Vector Magnitude).

5.1. Performance Comparison

Firstly, the EVM will be measured and compared for the three architectures. As the six-port receiver prototype does not include a LNA, it has been bypassed in the zero-IF/low-IF prototype, in order to measure the architectures at the same conditions. A 2595 MHz signal with a filtered 64-QAM modulation (0.3 roll-off square-root-raised cosine filter) is used. The LO power is $P_{LO} = 0$ dBm, and the RF power (P_{in}) varies from -45 to 0 dBm (take into account that the LNA is not included). The LO frequency is 2595 MHz for zero-IF and six-port receivers; in the case of low-IF, it is selected to achieve a lower IF of 2 MHz. EVM is calculated after the acquisition of 1000 symbols (8000 samples, $OSR = 8$).

Figure 11 shows the measured EVM for a symbol rate of 5 Msymbol/s (30 Mbps). On the one hand, six-port receiver has larger dynamic range than the other architectures due to the high dynamic range detector design. The measured values of EVM are bellow 7.5% (BER $\approx 10^{-3}$ for 64-QAM) from -32 dBm to -11.5 dBm for the low-IF receiver, and from -38.5 dBm to -3.5 dBm for the zero-IF receiver. The six-port receiver achieves an EVM below 7.5% from -45 dBm to 0 dBm. This is a higher dynamic range than that obtained with

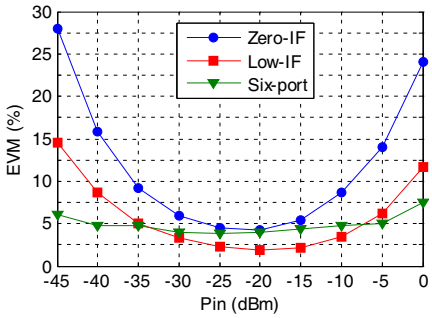

Figure 11. Measured EVM versus P_{in}: 2595 MHz, 30 Mbps 64-QAM, $P_{LO} = 0$ dBm.

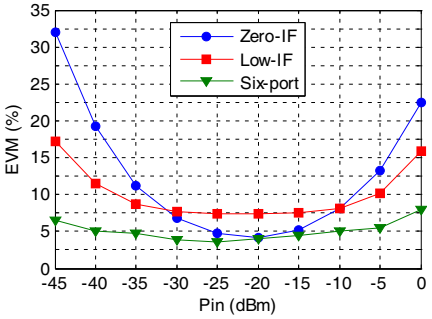

Figure 12. Measured EVM versus P_{in}: 2595 MHz, 75 Mbps 64-QAM, $P_{LO} = 0$ dBm.

six-port receivers based on zero-biased detector diodes. For example, a 37.3 dB dynamic range at $BER = 10^{-3}$ and 2.4 GHz is measured in [20], despite that the response of the detectors has been linearized using software techniques, in order to extend the square law region. On the contrary, we do not use any diode linearization technique. On the other hand, the minimum value of EVM is obtained with the low-IF architecture (2% for $P_{in} = -20$ dBm). Zero-IF receiver has a minimum EVM of 4.2% for $P_{in} = -20$ dBm. For the six-port receiver the minimum value of EVM is 3.8%, obtained with $P_{in} = -25$ dBm. These results are as we expected, as the low-IF architecture does not have DC-offset and flicker noise problems, whereas the 5 Msymbol/s RF signal is down-converted to a 0–3.25 MHz IF in the direct conversion architectures.

The measurement has been repeated for a wider RF signal. The maximum symbol rate that can be obtained with the VSG is 12.5 Msymbol/s (75 Mbps) for an $OSR = 8$, although the zero-IF/low-IF and the six-port receivers theoretically support 20 MHz and 100 MHz channels, respectively. The measured EVM for a data rate of 75 Mbps is presented in Figure 12. In this case, low-IF presents worse results. The reason is that the IF response curves of the zero-IF/low-IF prototype drop from 15 MHz, as it can be seen in Figure 13, and the 12.5 Msymbol/s RF signal is down-converted between 2 MHz and 18.25 MHz in low-IF configuration. For the zero-IF and six-port receivers, where the signal is down-converted to a 0–8.125 MHz IF, the values of EVM are very similar to that obtained with 5 Msymbol/s. This proves that the low-IF architecture demands more bandwidth and stricter I-Q balance requirements than the direct conversion scheme. Digital equalization and I-Q imbalance compensation techniques can be applied to solve these problems.

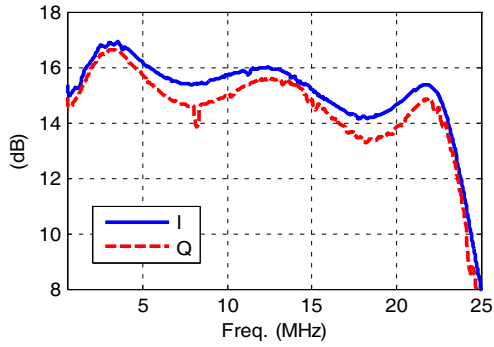

Figure 13. Measured IF response of the zero-IF/low-IF receiver.

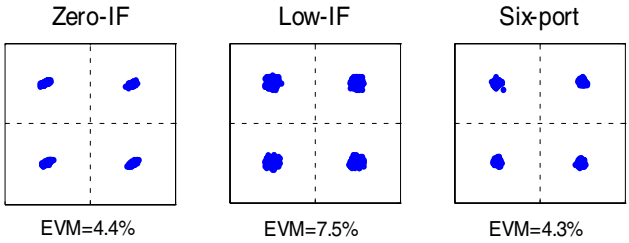

Figure 14. Constellation diagrams: 2595 MHz, 25 Mbps QPSK, $P_{in} = -25$ dBm, $P_{LO} = 0$ dBm.

The receiver prototypes have been also validated for other types of modulation schemes with similar results. Figure 14 shows the constellation diagrams obtained after the demodulation of a 2595 MHz QPSK signal (0.3 roll-off square-root-raised cosine filter), with a symbol rate of 12.5 Msymbol/s. The LO power is $P_{LO} = 0$ dBm, and the RF input power is $P_{in} = -25$ dBm.

5.2. Influence of the Image Frequency in Low-IF

Secondly, the effects of the image frequency on the low-IF receiver will be analyzed. The combination of a 2595 MHz 5 Msymbol/s 64-QAM signal and a 2584.5 MHz tone are introduced in the low-IF receiver. The LO power is $P_{LO} = 0$ dBm, and its frequency is fixed to 2589.75 MHz to achieve a lower IF of 2 MHz. After the acquisition of 1000 symbols (8000 samples, $OSR = 8$), the EVM is calculated for different image attenuation values. Measurements results are collected in Table 1. Signal quality degradation is low for image power levels

Table 1. Influence of the image frequency on the low-IF receiver.

Image Attenuation (dB)	EVM (%)
−10	10.7
0	2.9
10	2.5
20	2.4
30	2.3
40	2.1

below the desired signal power. Degradation starts being significant for equal RF and image power levels. When the image signal power is higher than the desired signal power, the EVM rises to such high values as 10.7% for an image attenuation of −10 dB. I-Q imbalance compensation algorithms must be applied, as I-Q imbalances decrease the image-reject capabilities of the front-end.

5.3. Influence of the LO Power Level

Finally, the influence of the LO power will be studied. Remind that one of the advantages of the six-port architecture is its operation with low LO powers. In order to prove that characteristic, the EVM as a function of PLO will be measured for the three architectures. In this case, a 2595 MHz QPSK modulated signal (0.3 roll-off square-root-raised cosine filter) is used. The symbol rate is 5 Msymbol/s (10 Mbps). The input power level is kept at $P_{in} = -20$ dBm. Figure 15 shows the EVM curves for P_{LO} values of 7, 0, −10, and −20 dBm. EVM is calculated over 1000 demodulated symbols. The six-port receiver performance keeps more stable versus P_{LO} variation, with an EVM increase of 0.6 points in percentage from 7 dBm to −20 dBm. Signal quality degrades 3.7 points in percentage for the low-IF receiver and 4.6 points for the zero-IF receiver. These results demonstrate that six-port receivers can operate with very low LO powers with good performance. This is an important advantage for SDR, as it entails low power consumption and cost reduction. In addition, problems derived from LO leakage and the self-mixing of LO, which are major drawbacks in direct conversion architectures, can be reduced.

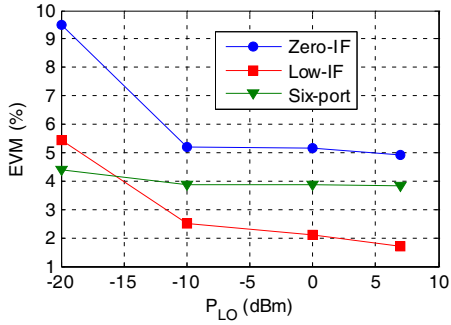

Figure 15. Measured EVM versus P_{LO}: 2595 MHz, 10 Mbps QPSK, $P_{in} = -20$ dBm.

6. SIX-PORT OPERATION AS DUAL ZERO-IF/LOW-IF RECEIVER

Six-port receivers are typically direct frequency conversion architectures. Nevertheless, the operation principle of six-port networks as both homodyne and heterodyne receivers was analytically demonstrated in [11]. In spite of it, almost all previous reported six-port receivers have been homodyne ones.

The first reported six-port network used as a heterodyne receiver was presented in [21]. The six-port architecture is used for down-converting the RF signal to an intermediate frequency of 900 MHz. The second frequency conversion is performed by an analog IF module, composed of two differential amplifiers and a conventional IF demodulator. However, the demodulation capability of the heterodyne six-port receiver is only demonstrated by means of simulation results. Heterodyne six-port receivers have been also used for radar applications [22]. In any case, the problem of heterodyne receivers is that they require a large number of external components, including bulky RF filters for image frequency rejection and IF circuits. Another problem is the difficulty of changing system parameters, since the RF and IF signals are processed by fixed narrowband analog components. Consequently, heterodyne architecture is not the best option when a SDR hardware implementation is addressed.

It has been seen that low-IF combines the advantages of homodyne and heterodyne schemes. Therefore, the most appropriate solution would be to take advantage of both zero-IF and low-IF benefits.

The transformation of the developed SDR six-port receiver into a dual zero-IF/low-IF SDR six-port receiver does not require any change in hardware. In effect, the new block diagram only has changes in

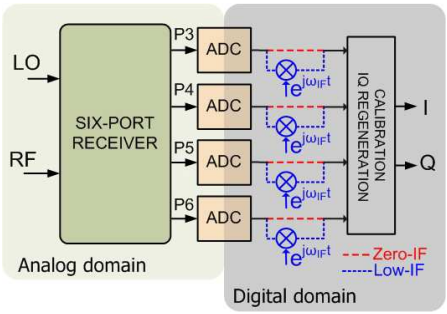

Figure 16. Block diagram of the dual zero-IF/low-IF six-port receiver.

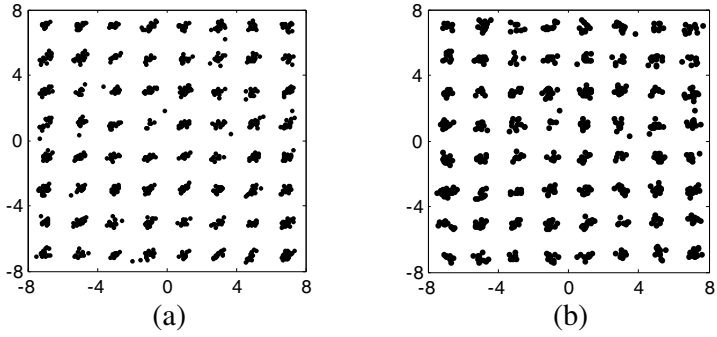

Figure 17. Constellation diagrams obtained from the six-port receiver in (a) low-IF and (b) zero-IF operation modes.

software, as it can be seen in Figure 16. In the low-IF operation mode, the RF signal is down-converted to an IF closed to zero by properly selecting the value of the LO frequency, which could be controlled by software. The final down-conversion to baseband is also performed in the digital domain. In the zero-IF operation mode, the LO and RF frequencies are equal, hence the acquired signals are directly baseband signals and no additional frequency conversions are required. Finally, the six-port calibration algorithm is applied to regenerate the original I-Q components.

First of all, we will validate the six-port receiver in low-IF operation mode. The RF input signal will be a 2.5 GHz signal with a filtered 64-QAM modulation (roll-off $\alpha = 0.3$) and a power level of -20 dBm. The LO frequency will be fixed to achieve that the lowest IF is equal to 2 MHz, and the LO power level will be 0 dBm. In such conditions, the constellation diagram is that presented in Figure 17(a)

Table 2. Six-port receiver performance operating in zero-IF/low-IF modes.

Symb. rate (Msymb/s)	Bit rate (Mbps)	Zero-IF mode		Low-IF mode	
		IF (MHz)	EVM (%)	IF (MHz)	EVM (%)
1.9531	11.71	0–1.2695	6.37	2–4.539	3.05
12.5	75	0–8.125	4.4	2–18.25	3.69

Table 3. Influence of the image frequency on the six-port receiver in low-IF mode.

Image Attenuation (dB)	EVM (%)
−10	36.73
−5	31.45
0	22.77
10	13.15
20	4.04

for a 75 Mbps bit rate. The corresponding constellation for the zero-IF mode is presented in Figure 17(b).

The performance comparison of the six-port receiver operating in zero-IF and low-IF modes is presented in Table 2. It can be seen that the lowest values of EVM are obtained in the low-IF mode, as DC-offset and flicker noise problems do not affect the quality of the signal. That is the reason why the low-IF improvement is more evident for narrow band signals, apart from the additional signal degradation in zero-IF due to the DC-offset cancellation high-pass filter. However, remind that this did not happen in the conventional zero-IF/low-IF receiver prototype, where low-IF was superior only for narrow band signals. It was due to the I-Q imbalances, which are now compensated by the calibration method in the six-port receiver. Nonetheless, it is worth to emphasis that the double baseband bandwidth is required in the low-IF mode, which means more complexity in the diode detector design and in the A/D conversion module.

Furthermore, image frequency remains a major problem in low-IF mode. A RF tone located at the image frequency is introduced in combination with the desired signal. Table 3 shows the effect of the image frequency on the EVM. Note that in this case the degradation of EVM is higher than that observed with the conventional low-IF receiver for the same image attenuation. The reason is that the calibration constants are calculated from a training sequence within the received

data frame. Therefore, in the presence of an image frequency the six-port calibration may produce erroneous calibration constants values, leading to an inadequate IQ regeneration.

To sum up, the six-port architecture is susceptible to operate as both zero-IF and low-IF down-conversion schemes without any hardware modification. The system reconfigurability can be completely controlled via software. Such flexibility is a very important advantage, since the system operation mode can be selected depending on, for example, the application, the environment conditions, etc.. For example, the low-IF operation mode can be selected for narrow band signals, since DC-offset and $1/f$ noise would not degrade the downconverted signal and the A/D conversion requirement would be reachable. However, digital compensation techniques must be applied for image rejection. Moreover, zero-IF mode is more suitable for high-speed signal demodulation, as half video bandwidth is demanded compared with low-IF.

7. TOWARDS THE MINIATURIZATION OF SIX-PORT RECEIVERS

The above contributions prove that the six-port receiver presents promising advantages and benefits. However, one important problem is still pending: the large dimensions of the six-port receiver.

The bandwidth requirements of a RF front-end for SDR force to use multisection designs, which leads to large size circuits. The higher the frequency, the smaller the passive circuit and the easier the integration in a MMIC design [23, 24]. However, for operating frequencies in the lower gigahertz region, a broadband design in conventional technology leads to large dimensions, which could be prohibitive, for example, for mobile communication applications. Therefore, new technologies and solutions must be explored in order to achieve compact size and low-cost productions for configurable radio terminals.

Some solutions of multilayer six-port designs have appeared in the literature [25, 26]. In [27], the authors propose the LTCC technology for implementing a miniaturized broadband six-port receiver. LTCC is a cost-effective multi-layer substrate technology which enables to develop compact microwave and millimeter wave modules. It makes possible to integrate passive and active microwave circuits, antenna structures, low-frequency electronics, and digital components on one multilayer substrate.

In the first place, an LTCC 90-degree hybrid coupler was designed and fabricated, since it is the most critical component of the six-

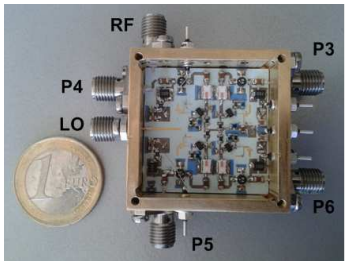

Figure 18. Fabricated 30 × 30 × 1.25 mm 0.3–6 GHz LTCC six-port receiver.

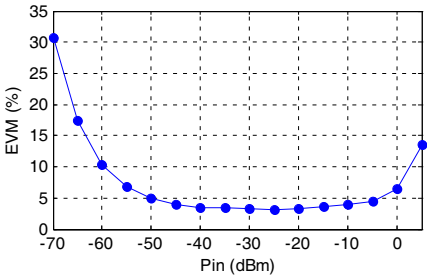

Figure 19. LTCC six-port receiver performance: measured EVM versus Pin at 2.5 GHz, 75 Mbps 6-QAM, $P_{LO} = 0$ dBm.

port network, and a first six-port network design was proposed [27]. Once proved the viability of the technology, a reduced version of the six-port receiver presented in Section 3 has been developed in LTCC technology. Figure 18 shows a photograph of the fabricated LTCC six-port receiver. Its dimensions have been reduced to $30 \times 30 \times 1.25$ mm, with no loss in the receiver performance. In effect, Figure 19 shows the measured EVM obtained with the LTCC six-port receiver in the same conditions of Figure 12. Note that the EVM values are even better to that obtained with the conventional technology six-port receiver. Therefore, the measured dynamic range at $BER = 10^{-3}$ (EVM$\approx$ 7.5% for 64-QAM) is 58 dB. In addition, experimental demodulation results have demonstrated a good performance over the same four-octave bandwidth (0.3–6 GHz) at high data rates (up to 93.6 Mbps).

8. CONCLUSION

An experimental performance comparison between the six-port receiver and a conventional zero-IF/low-IF receiver has been presented in this paper. Interesting conclusions can be extracted from the obtained results.

On the one hand, low-IF architecture can achieve very low values of EVM for narrow band signals, as it is not affected by DC-offset and $1/f$ noise problems. However, direct conversion receivers seem to be the best option when dealing with broadband signals. Low-IF requires the double bandwidth than direct conversion schemes, whereby it is more difficult to maintain proper I-Q balance, which is indispensable to achieve a good image frequency rejection. Image frequency remains a major problem in low-IF receivers, as it can not

be easily solved. On the other hand, the six-port technique shows benefits over conventional zero-IF and low-IF receivers. It can operate with very low values of LO power such as −20 dBm, keeping good quality of the demodulated signal. This is a very important advantage for SDR, as it entails low-cost and low power consumption, as well as a reduction of the LO self-mixing problem [7], troublesome in direct conversion architectures. Furthermore, an important enhancement of the six-port receiver dynamic range has been achieved due to the use of biased detector diodes. This is a very important result, since dynamic range extension is one of the key points in SDR implementation. All previously reported six-port receivers use zero-bias detector diodes, whereby six-port architecture has been traditionally said to have average dynamic range performance compared conventional receivers. However, due to the selection of a high bias current in the diode detector design, the six-port receiver presents larger dynamic range than the conventional zero-IF/low-IF receiver for a LO power around 0 dBm. A dynamic range of 58 dB at $BER = 10^{-3}$ is achieved with the LTCC six-port receiver. There are not many experimental data about dynamic range in six-port receivers. A 37.3 dB dynamic range at $BER = 10^{-3}$ is reported in [20], where a 0.8–2.4 GHz six-port receiver based on zero-biased detector diodes is presented. It is worth to mention that a diode linearization software is used in [20] to extend the square law region, while we do not use any diode linearization technique.

Another key advantage is that six-port receivers can operate over extremely large frequency ranges. The demodulation capability of the developed six-port receiver from 0.3 GHz to 6 GHz has been demonstrated in [14], which is a four-octave bandwidth.

Moreover, we have experimentally demonstrated, for the first time, the capability of the six-port architecture to operate as both zero-IF and low-IF down-conversion schemes. Six-port receivers are traditionally direct conversion architectures. However, we have proposed a dual zero-IF/low-IF SDR six-port receiver, in order to take advantage of both architectures. Such dual operation mode does not require any change in hardware, since all signal processing is digitally performed.

Nevertheless, one of the main problems of broadband six-port receiver is the large size of the passive six-port circuit. Consequently, the potentials of the LTCC technology for the miniaturization of six-port receivers have been shown. A miniaturized ($30 \times 30 \times 1.25$ mm) four-octave (0.3–6 GHz) LTCC six-port receiver has been presented. These promising results may lead to reconsider the six-port architecture as an alternative for the lower gigahertz region, hence for

mobile communication applications.

Considering all the factors mentioned above, it seems logical to consider the six-port architecture as a strong candidate to implement a SDR.

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