Progress In Electromagnetics Research Letters, Vol. 34, 83–90, 2012

K-BAND HARMONIC DIELECTRIC RESONATOR OSCILLATOR USING PARALLEL FEEDBACK STRUCTURE

Y. C. Du*, Z. X. Tang, B. Zhang, and P. Su

School of Electronic Engineering, University of Electronic Science and Technology of China, Chengdu, Sichuan, China

Abstract—A novel K-band harmonic dielectric resonator oscillator (DRO) is presented. Two identical parallel feedback DROs constitute a symmetric structure by sharing the same dielectric resonator (DR). As a result of this special structure, the odd frequency output components offset while the even harmonic frequency components superimposed at the output port. Odd and even mode analysis method is used in theoretical analysis. As the experimental results shown, the fundamental frequency is 9.45 GHz and the output power at the second harmonic frequency of 18.9 GHz is 9.45 dBm. The suppression of fundamental frequency is about 15.5 dBc. A phase noise of −97 dBc/Hz@100 KHz and −78 dBc/Hz@10 KHz is achieved at the output frequency.

1. INTRODUCTION

Oscillator is very important in communication system. As communication frequency improves fast, it is necessary to improve the frequency of oscillator at the same time. However, the fundamental frequency of an oscillator is limited by the operating frequency of active devices. The maximum output frequency can be doubled by using an oscillator's second harmonic output. The push-push oscillator, which cancels out odd harmonic frequency and enhances even harmonic frequency by combining two identical series feedback oscillators together, has been the focus of much attention in recent years [1–7]. Compared with series feedback oscillators, parallel feedback oscillators can output higher power in which there is greater proportion of the second harmonic component, too [8]. If two identical

---

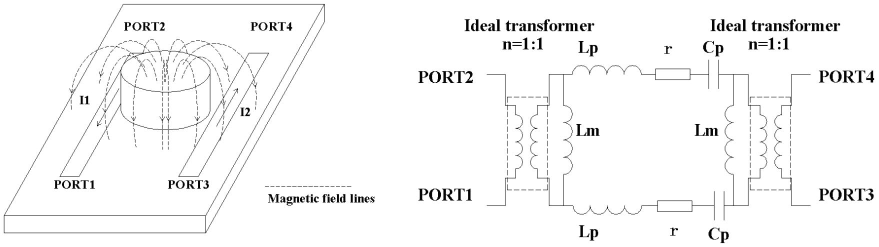
Received 11 June 2012, Accepted 20 August 2012, Scheduled 28 August 2012

* Corresponding author: Yicheng Du (asdfghdu@126.com).

parallel feedback oscillators are combined in a proper way by sharing a single resonant network, the second harmonic output power could be improved while the fundamental component at the output is still suppressed. And a low phase noise can be obtained by using a high-Q dielectric resonator.

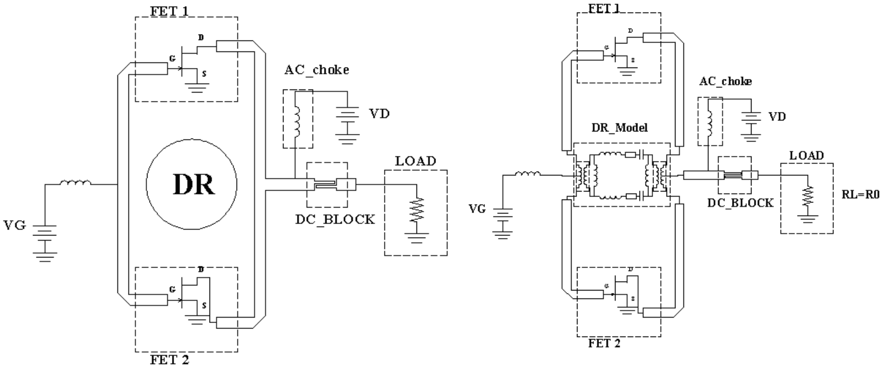
2. THEORETICAL ANALYSIS OF BASIC CIRCUIT STRUCTURE

The coupling structure of DR and two micro-strip lines is shown in Figure 1(a) [9]. The DR, which operates in $TE_{01\delta}$ mode, is coupled with the micro-strip lines through magnetic field. The induced currents



(a) (b)

Figure 1. The coupling structure of DR and two microstrip lines. (a) Coupling circuit, (b) equivalent circuit.



(a) (b)

Figure 2. Simplified structure of this harmonic frequency oscillator. (a) Simplified structure, (b) circuit used lump model.

in two micro-strip lines are the same in value but reverse in phase. And the voltages in Port 1 and Port 2 are also same in value but reverse in phase. In order to simplify analysis and circuit simulation, a lump parameter equivalent circuit is used. The equivalent circuit and corresponding ports are shown in Figure 1(b) [9].

The circuit structure of this harmonic oscillator is shown in Figure 2(a), while in Figure 2(b), the DR has been replaced by its lump parameter equivalent circuit. Two identical parallel feedback oscillators are combined by sharing a same feedback path. In the following sections, the theories about this structure are studied in detail.

It is convenient to use odd and even mode analysis method to analyze this structure as it shows the characteristic of symmetry [9]. The odd mode and even mode equivalent circuits are shown in Figure 3, in which the DC bias circuits are removed, and only the AC equivalent circuits are given. In the odd mode equivalent circuit, the connections are grounded in the middle of the origin circuit, which are broken in the even mode equivalent circuit. The odd mode equivalent circuit is equivalent to a normal parallel feedback oscillator. But in the even mode equivalent circuit, the feedback path is broken. As a result, even mode voltage or current cannot feed back to the input of the amplifier, which means that there is not any even mode voltage or current in the circuit at the fundamental frequency. Therefore, the circuit can and only can oscillate in its odd mode, in which the voltages and currents in the corresponding points of the two oscillators are the same in amplitude but opposite in phase at its operating frequency.

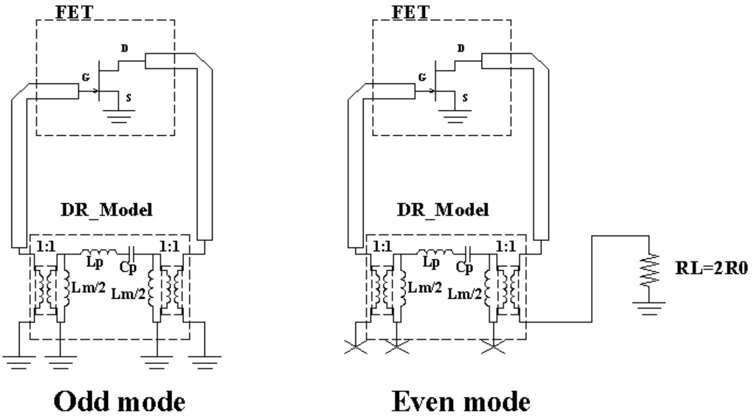


Figure 3. The odd and even mode equivalent circuits.

As the oscillation power increased, the amplifier will enter the nonlinear area, in which high harmonic components are generated. The relationship between the gate voltage of the transistor V_{gs} and its drain current I_D is illustrated in Formula (1) [8].

$$I_D = a_0 V_{gs} + a_1 V_{gs}^2 + a_2 V_{gs}^3 + a_3 V_{gs}^4 + \ldots \tag{1}$$

As analyzed, the voltages are opposite at corresponding points in two oscillators. Therefore, the gate voltages of two transistors in two oscillators, V_{gs1} and V_{gs2}, are opposite to each other. The way by which the output currents of two oscillators are combined is shown in Formula (2).

$$\begin{aligned} I_{D1} + I_{D2} = {} & a_0 V_{gs1} + a_1 V_{gs1}^2 + a_2 V_{gs1}^3 + a_3 V_{gs1}^4 + \ldots a_0 V_{gs2} + a_1 V_{gs2}^2 \\ & + a_2 V_{gs2}^3 + a_3 V_{gs2}^4 + \ldots = a_0 V_{gs1} + a_1 V_{gs1}^2 + a_2 V_{gs1}^3 \\ & + a_3 V_{gs1}^4 + \ldots a_0(-V_{gs1}) + a_1(-V_{gs1})^2 + a_2(-V_{gs1})^3 \\ & + a_3(-V_{gs1})^4 + \ldots = 2 \cdot (a_1 V_{gs1}^2 + a_3 V_{gs1}^4 + \ldots) \end{aligned} \tag{2}$$

The result only contains even power terms which contain only even harmonic components. So the fundamental and odd components of two oscillators are canceled out by each other.

3. DESIGN OF A HARMONIC DRO

As shown in the above analysis, we can design an ordinary parallel feedback DRO at 9.45 GHz at first, and then combine two identical DROs together with DC bias and output DC block parts to finish a design.

Agilent's gallium arsenide field-effect transistor (GaAs FET) ATF26884 is used. Refering to ATF26884's datasheet, the gain of this transistor is fairly low at 19 GHz (1.3 dB), so it can testify the

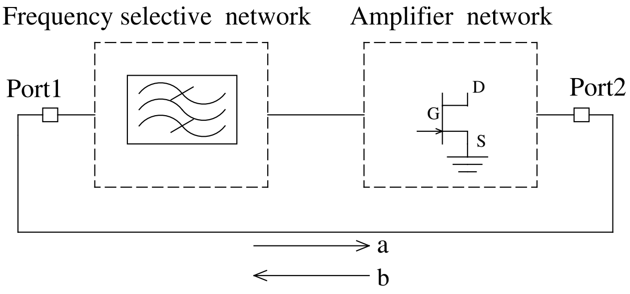


Figure 4. Block diagram of parallel feedback oscillator.

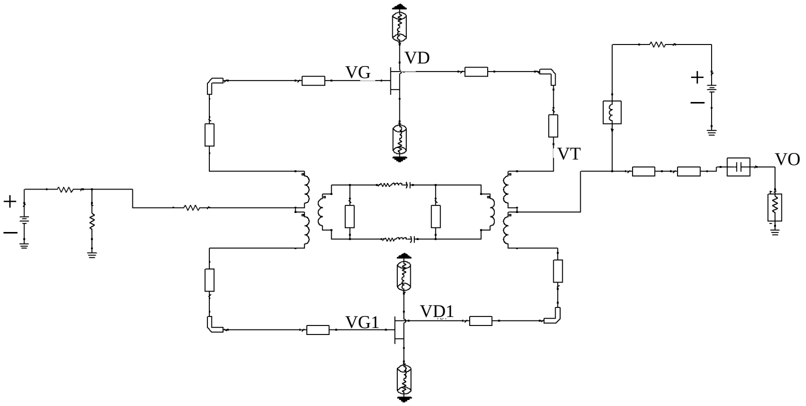


Figure 5. The schematic of harmonic DRO.

practicality of this structure. Rogers 4350 ($\varepsilon_r = 3.66$, $\tan\delta = 0.004$ and thickness of 20 mil), a high frequency and low loss substrate, is used. Agilent's Advanced Design System 2009 (ADS2009) is used in the circuit simulation.

The block diagram of parallel feedback oscillator is shown in Figure 4 [8].

To design a parallel feedback oscillator, the amplifier network with a small S_{11} and large S_{21} should be designed first, and then the phase of S_{21} is adjusted to an integer multiple of 2π. Connecting its output port and input port, the circuit will oscillate [8].

After one oscillator is designed, two identical oscillators are combined together, as shown in Figure 5. As Figure 5 shows, two microstrip lines replace the coupled inductors Lm shown in Figure 1(b) in the lump parameter equivalent circuit. A lump inductor can cause considerable attenuation at the second harmonic frequency as inductive reactance is proportional to frequency, so using a microstrip line to replace can achieve a more accurate result of the second harmonic power. The length of microstrip line d represented by the inch can be calculated from Formula (3) in which l is the inductance represented by nH, Z_0 the characteristic impedance of microstrip line, and ε_r the relative dielectric constant of the substrate [9]. The simulation results are shown in Figure 6.

$$d = \frac{11.81 \cdot l}{Z_0 \cdot \sqrt{\varepsilon_r}} \tag{3}$$

The simulation results show that only even harmonic components exist in output power, which verifies the theoretical analysis above.

4. EXPERIMENTAL RESULTS

Figure 7 shows a photograph of the proposed DRO. The circuit is supplied by a linear power of ±5 V converted from a +9 V power source, and R&S spectrum analyzer FSP40 is used to measure output power as well as the phase noise. The IF bandwidth is 3 kHz, and the video bandwidth is 300 Hz as the phase noise is measured.

Figure 8 shows the test results.

The operating current of each transistor is about 30 mA. The output power is 9.58 dBm, which is a little higher than the simulation results. As parallel feedback DRO has fairly large output power, even though the outputs of two oscillators are simply connected, a considerable second harmonic power can still be achieved. This is a significant advantage compared to traditional push-push circuit. The phase noise can achieve −97 dBc/Hz@100 KHz and

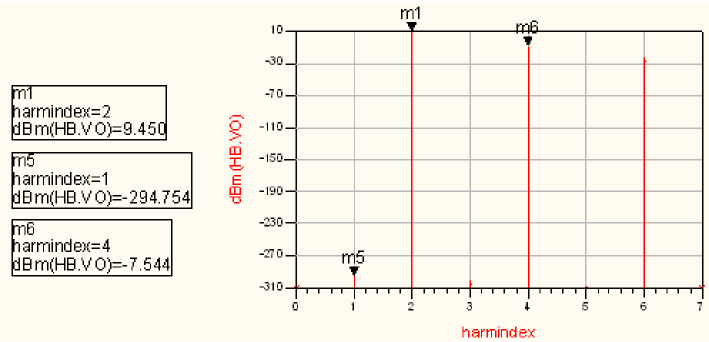


Figure 6. The simulation results.

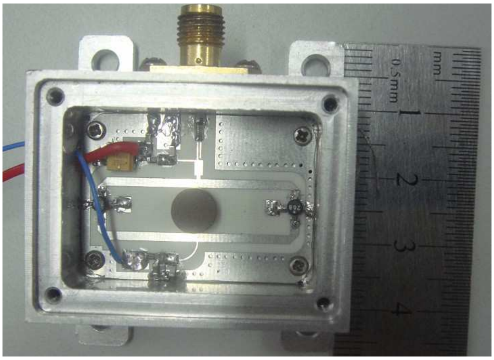
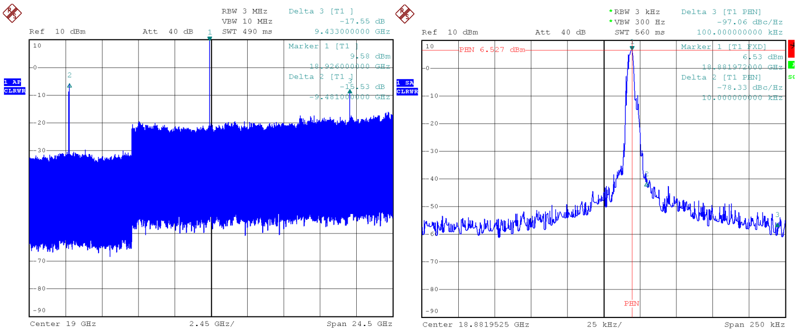


Figure 7. Photograph of proposed DRO.



(a) (b)

Figure 8. Test results. (a) Each harmonic output power, (b) phase noise.

Table 1. Comparison performance.

	Output frequency [GHz]	Output power [dBm]	Fundamental harmonic suppression [dBc]	Phase noise [dBc/Hz @100 kHz]
Ref. [1]	58	−14	17	−100
Ref. [2]	17.4	−14	15	−95
Ref. [3]	34	3	15	−99
Ref. [4]	14	−0.4	28.59	−98
Ref. [6]	18	3.1	17	−103
This work	18.9	9.58	15.5	−97

−78 dBc/Hz@10 KHz. The suppression of fundamental frequency is 15.53 dB.

Table 1 shows the performance comparison with other previous studies. Although the operating frequencies of some other works are higher than the proposed one, it should be taken into account that the performance of the transistor ATF26884 at high frequency is fairly poor. So, it is unnecessary to take the operating frequencies of referenced works. As shown in Table 1, the output power at second harmonic frequency of the proposed oscillator is obviously higher than that of other works. Furthermore, the phase noise and fundamental frequency suppression are also good, compared with other works. According to Table 1, the proposed push-push DRO shows comparable performance, especially the output power.

5. CONCLUSIONS

A new structure of harmonic DRO is proposed, and a K-band oscillator of this structure is designed and fabricated. Taking advantage of the high power characteristic of parallel feedback oscillator, the output power of second harmonic frequency can be improved significantly. Moreover, as shown by the measured results, the output power of the proposed DRO is higher than other referenced oscillators, which justifies the advantage of the proposed structure.

REFERENCES

1. Sinnesbichler, F. X., "Hybrid millimeter-wave push-push oscillators using silicon-germanium HBTs," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 51, No. 2, 422–430, 2006.
2. Xia, Q., Z. X. Tang, and B. Zhang, "A Ku-band push-push dielectric resonator oscillator," *Journal of Electromagnetic Waves and Applications*, Vol. 24, Nos. 14–15, 1859–1866, 2010.
3. Pavio, A. M. and M. A. Smith, "A 20–40 GHz push-push dielectric resonator oscillator," *IEEE Trans. on Microw. Theory and Tech.*, Vol. 33, No. 12, 1346–1349, 1985.
4. Su, P., Z. X. Tang, and B. Zhang, "Push-push dielectric resonator oscillator using substrate integrated waveguide power combiner," *Progress In Electromagnetics Research Letters*, Vol. 30, 105–113, 2012.
5. Sinnesbichler, F. X., H. Geltinger, and G. R. Olbrich, "A 38-GHz push-push oscillator based on 25-GHz f_T BJT's," *IEEE Microwave and Guided Wave Letters*, Vol. 9, No. 4, 151–153, Apr. 1999.
6. Dussopt, L. and G. M. Rebeiz, "A low phase noise 18-GHz push-push VCO," *IEEE Microwave and Wireless Components Letters*, Vol. 13, No. 1, 4–6, Jan. 2003.
7. Lee, O., J.-G. Kim, K. Lim, J. Laskar, and S. Hong, "A 60-GHz push-push InGap HBT VCO with dynamic frequency divider," *IEEE Microwave and Wireless Components Letters*, Vol. 15, No. 10, 679–681, Oct. 2005.
8. Grebennikov, A., *RF and Microwave Transistor Oscillator Design*, 1st edition, Wiley, New York, 2007.
9. Pozar, D. M., *Microwave Engineering*, 3rd edition, Wiley, New York, 2004.