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HIGH PERFORMANCE V-BAND GAAS LOW NOISE AMPLIFIER WITH MODIFIED COPLANAR WAVEGUIDE EBG TRANSMISSION LINES TECHNOLOGY

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Abstract—This paper presents an integrated millimeter-wave (mmW) low noise amplifier (LNA) which is implemented by using 0.15-μm baseline GaAs pHEMT technology. The design utilized modified co-planar waveguide (CPW) to perform a slow wave transmission line (TLine) with electromagnetic band gap (EBG) ground structures for the input/output matching networks. The low noise V-band LNA chip size was hence reduced by adopting the new EBG transmission lines. The developed amplifier exhibited a noise figure of 6.21 dB, and a peak gain of 17.3 dB at 66 GHz. Additionally, the amplifier has linear characteristics and its measured third-order intercept (IIP3) point is greater than −0.5 dBm under a dc power consumption of 75 mW.

1. INTRODUCTION

Recently, high data rate requirements has grown a fast interest in the unlicensed band, the wide available bandwidth of 7 GHz (57–64 GHz in the USA, 59–66 GHz in Japan, 57–66 GHz in Europe) fueled by standards and applications led by WiHD, WiGig and 802.15c. Interest in IEEE 802.15c communications systems for indoor and high speed wireless application has led to significant progress of broadband mmW integrated circuits and wireless personal area networks (WPAN) aim to deliver data rates of 2 to 3Gb/s or even more. GaAs technology provides a low loss substrate, a high linear output power and a low signal distortion compared to traditional RFCMOS process. In this paper, we describe a compact size and a high performance V-band GaAs pHEMT LNA by using EBG ground structure.

Impedance matching networks in the reported circuits were based upon either lumped inductors [1] or electromagnetic bandgap (EBG)

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structures CPW TLines [2, 3]. Lumped inductors offer smaller area and larger quality factors than TLine based matching networks, but are more difficult to be precisely simulated at millimeter-wave band. Modified CPW for EBG-CPW TLines, on the other hand, can be considerably smaller than their conventional counterparts and exhibit high Q values [1, 4, 5].

In this work, a compact size V-band LNA with EBG TLines was demonstrated in standard 0.15-μm GaAs pHEMT process for low noise solution. As an important component for most receivers, the LNA was designed to provide low noise figure and to obtain respectable gain over a broad frequency band especially for high data rate application. The proposed LNA is designed to simultaneously achieve high gain and low noise characteristics.

2. INTERCONNECTION EBG-CPW TLINES

The values of the required inductances in the circuit are smaller than those provided by standard spiral inductors and we have therefore opted for the TLine approach. Conventional coplanar microstrip, and grounded microstrip TLines on GaAs substrate typically exhibited quality factor of 10∼25, which are not sufficient for low noise design. Since it has been shown that EBG TLines can provide much higher Q values [2], we have also taken this approach into this study. The structure of the EBG TLines used in this work is shown in Fig. 1. The slotted bottom metallic shields were patterned as 130 μm metal stripes separated by 10 μm slot widths. The signal line metal width was 37 μm, the distance between signal line metal and the metallic ground was 5 μm. All metal layer resistivity was 0.02 ohm/square, and insulator layers GaAs.

The electromagnetic simulation of EBG TLines is fairly complex, but can be preformed successfully. The numerical analysis of the EBG-CPW LNA studied is performed using the commercial computer software package, Momentum of Agilent Technologies, Advanced Design System (ADS), which is based on the method of moment (MoM) technique for layered media. Momentum solves mixed potential integral equations (MPIE) using full wave Green's functions.

A comparison of the standard (Std.) CPW TLine and EBG-CPW TLines, simulated performance of the TLines is shown in Fig. 2(a). high Q values obtained. For comparison purposes, the results of a classical CPW TLine realized. The centre cut-off frequency which is the resonant frequency depends on the transverse slots number and the square etched hole of the ground plane. The geometrical dimensions and the 60-GHz main electrical properties are summarized in Table 1.

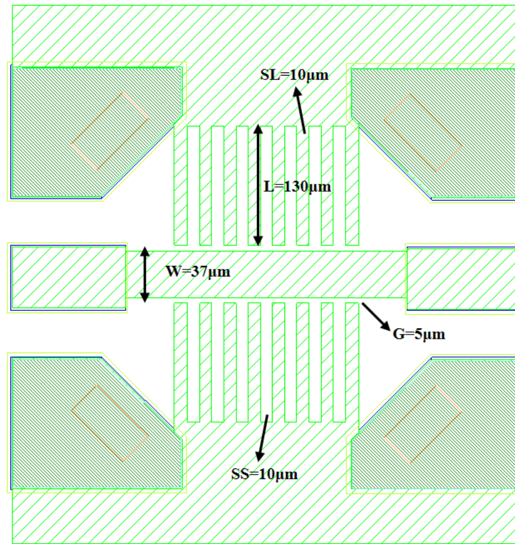

Figure 1. EBG TLine with slotted ground shield.

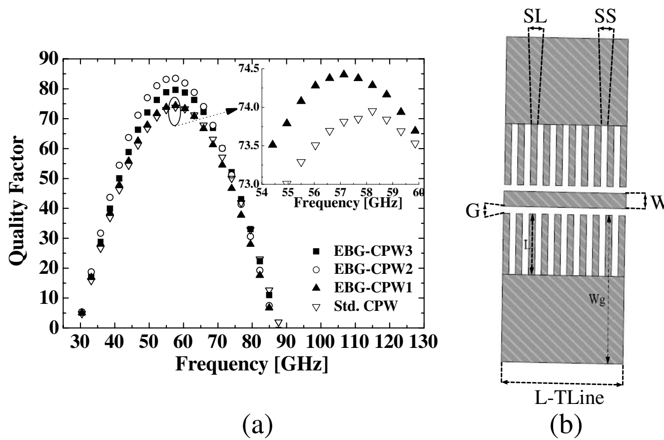

Figure 2. (a) Simulated quality factor. (b) Cross-section of the EBG CPW topology.

In order to avoid the complex EM simulations of EBG CPW TLines, we have developed a simple analytic model, which accurately predicts their properties. The model takes advantage of the well established models of grounded and standard CPWs. The Z element (L, R and C) of EBG TLine model is shown in Fig. 3. It shows that EBG TLine obtained high quality factor (large propagation constant)

Table 1. Physical characteristics and 60-GHz electrical properties for DGS S-CPW.

Parameters	S-CPW parameters								Electrical performance at 60 GHz	
	W (μm)	*G* (μm)	Slot number	*SS* (μm)	*SL* (μm)	*L* (μm)	*Wg* (μm)	TLine length (μm)	*Z* (Ω)	*Q*
Std.CPW TLine	42	7	–	–	–	–	250	450	50.7	73.6
EBG S-CPW1	37	5	9	5	15	130	250	450	49.5	73.8
EBG S-CPW2	37	5	9	10	10	130	250	450	52.4	84.5
EBG S-CPW3	37	5	9	15	5	130	250	450	51.3	79.4

can be achieved by increasing C and L in the TLine.

The resonant frequency of the parallel circuit is defined as

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{1}$$

The equivalent impedance equation of the single resonant model may be expressed as

$$Z = \frac{1}{\frac{1}{R}\frac{1}{j\omega L} + j\omega C} \tag{2}$$

According to the microwave network theory as

$$S_{21} = \frac{2Z_0}{2Z_0 + Z} = \frac{2Z_0}{2Z_0 + \frac{1}{1/R + 1/j\omega L + j\omega C}} \tag{3}$$

The 3-dB cut-off angular frequency ω_c can be determined as

$$S_{21} = \frac{2Z_0}{2Z_0^2 + \left(\frac{\omega_c/C}{\omega_0^2 - \omega_c^2}\right)^2} = \frac{1}{\sqrt{2}}, \quad R \gg Z_0 \tag{4}$$

(1) Into (3), the Capacitance is obtained as

$$C = \frac{\omega_c}{2Z_0\left(\omega_0^2 - \omega_c^2\right)} \tag{5}$$

The inductance can be determined by

$$L = \frac{1}{\omega_0^2 C}\frac{1}{4\pi^2 f_0^2 C} \tag{6}$$

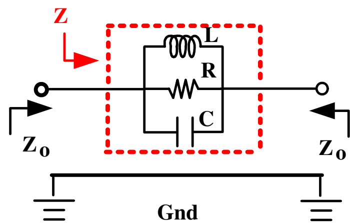

Figure 3. EBG TLine model.

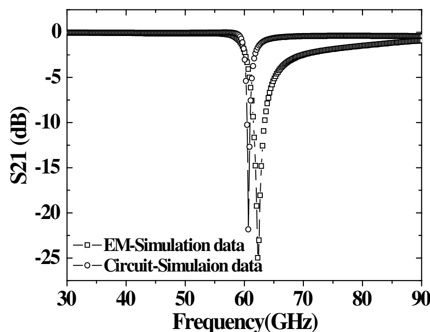

Figure 4. EM simulated data and circuit simulation data.

Table 2. Parameters extracted from equivalent circuit.

Parameters	**Parameters value**
Slot, D (μm)	10
Signal width, W (μm)	37
Metallic ground, G (μm)	5
Resonant frequency, ω_o (GHz)	60
Inductance, L (nH)	0.011
Capacitance, C (pF)	0.64
Resistance, R_1 (kΩ)	1.49

Therefore, the resistance R of the circuit can be obtained form resonant frequency ω respectively

$$S_{21}\left|_{\omega=\omega_0}\right. = \left|\frac{2Z_0}{2Z_0+Z_s}\right| = \frac{2Z_0}{2Z_0+R} \Rightarrow R = 2Z_0\frac{1-S_{21}\left|_{\omega=\omega_0}\right.}{S_{21}\left|_{\omega=\omega_0}\right.} \tag{7}$$

Therefore, this model can predict the EBG TLines with slotted ground shield over the relatively wider frequency range from 50 to 70 GHz, as shown in Fig. 1, in which the circuit simulation results and the EM simulation results show good agreement, as shown in Fig. 4. The resistors, capacitances and inductances are evaluated from the resonant frequencies of the EBG TLines with slotted ground shield and listed in Table 2.

3. V-BAND LNA DESIGN

The proposed LNA was demonstrated on 6 inch semi-insulating GaAs pseudomorphic high electron mobility transistor (pHEMT) technology together with a 0.15 μm gate length T-gate technology which was directly written by electron beam writer. A 12 nm undoped InGaAs channel layer was sandwiched between two Si planar δ-doped layers for high current and high power consideration. A 25 nm-thick n^+ AlGaAs (1×10^{17}cm^{-3}) layer was grown on an intrinsic AlGaAs spacer layer as a Schottky layer, which improves parallel conduction at high voltage. Finally, a 35 nm n^+-GaAs cap layer was grown to improve the resistivities of the ohmic contacts. Ohmic contacts were realized by using Au/Ge/Ni/Au alloy followed by a 430°C, 15 seconds rapid thermal annealing (RTA) alloy. Ion-implant isolation technology was used for mesa isolation to prevent the flow of any side-wall gate leakage current. The 0.15 μm-long T-shaped photoresist profile was formed by bi-layer polymer design and electron beam directly writing technology. After the highly selective succinic acid chemical gate recess process, the Ti/Pt/Au-gates were deposited by lift-off process. Before the deposition of metal-1, a 1000 Å SiN_x was deposited by plasma enhance chemical vapor deposition (PECVD) at 280°C for passivation. The 1 μm Å-thick gold metal (Ti/Au = 500 Å/10000 Å) was then deposited on the SiN_x passivation layer using an electron-beam evaporator. Finally, a 2000 Å SiN_x layer was deposited as a insulator layer between metal-1 layer and metal-2 layer (2 μm-thick gold). The pHEMT of 2 fingers with total gate width of 50 μm has a typical unit current gain cutoff frequency of 78 GHz, power gain cut-off frequency of 134 GHz with 3 V supply.

The three stage common-source LNA schematics are shown in Fig. 5. The first stage transistor had 2 fingers with total gate width of 50 μm. It was biased at a supply voltage of 3 V and drain current of 13 mA. Note that all the matching networks and inductances incorporate EBG-CPW slow wave transmission lines.

The contribution of each noise source to the total output noise is evaluated. The NF is then calculated by evaluating the ratio of the total output noise to the output noise due to parasitic resistance and transistor source resistance.

A die photo is shown in Fig. 6. Note in particular that the EBG TLines are much shorter (by a factor of two) than similar designs using conventional TLines. The chip size of $1.2 \times 0.8\,\mathrm{mm}^2$.

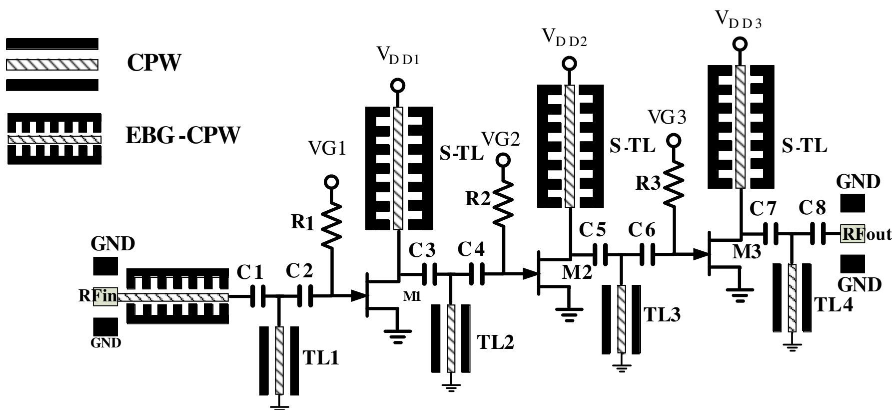

Figure 5. EBG-CPW LNA schematics.

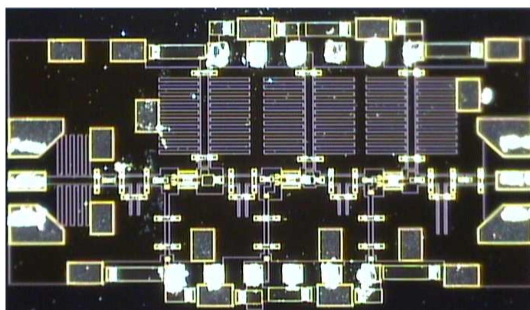

Figure 6. Die photo of EBG TLine LNA.

4. MEASUREMENT RESULTS

The V-band EBG TLines LNA chip measured through on-wafer probing. The related measurement demands are also raised to achieve a complete design flow. As the technology is in progress, a lot of one-box instruments, such as the signal generator (SG) and spectrum analyzer (SA), for high operating frequency were developed for convenience. But some special parameter testing systems, like NF analyzer (NFA) and input third-order intercept point analyzer (IIP3A). For further discussion, the building blocks of the on-wafer NF test system are depicted in details and shown in Fig. 7. A calibrated noise source is usually a diode that is reverse biased to generate noise. The excess noise ration (***ENR)*** is the difference between T_h and T_c, in terms of the equivalent noise temperatures at on/off states. Y-factor is defined

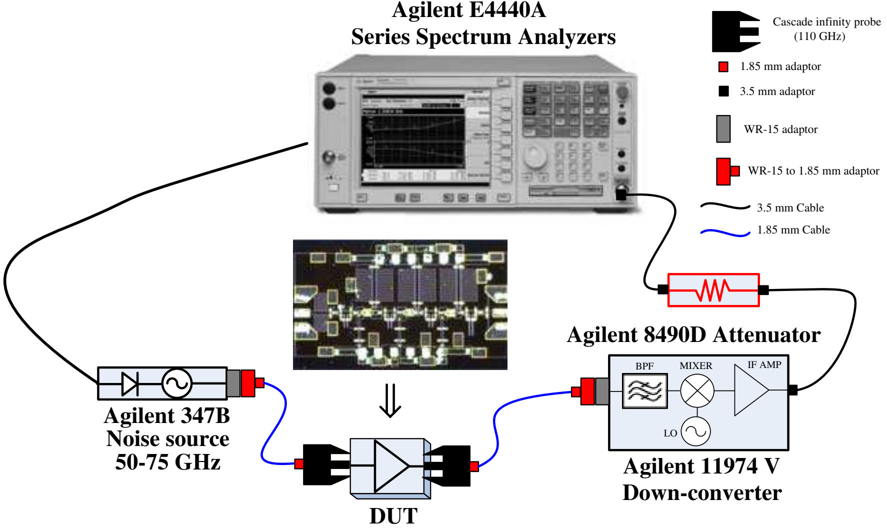

Figure 7. Test setup and procedure of MMW amplifier NF measurement.

as the ratio of N_h to N_c which corresponds to the measured noise powers at on/off states, respectively. A noise source with appropriate ENR is essential, as a rule of thumb, it is recommended to choose a higher ENR for high NF DUT or lower ENR for low NF DUT. If the NF of DUT is much higher than the ENR, it will lead to errors. To calculate the Y-factor substituted by $\boldsymbol{ENR}$ and noise factor, the following equations are used [6].

$$F = \frac{T_c + T_e}{T_c} \tag{8}$$

$$ENR = \frac{T_h + T_c}{T_c} \tag{9}$$

$$Y = \frac{T_h + T_e}{T_c + T_e} \tag{10}$$

where T_e is the equivalent noise temperature of DUT. While Y-factor approaches to one, it makes the measured values of the on/off states too hard to distinguish the DUT's NF from the self-generated noise. Whereas the available gain obtained simultaneously in Y-factor method is derived as below

$$G_a = \frac{\frac{N_{h_\mathrm{DUT}} - N_{c_\mathrm{DUT}}}{T_{h_\mathrm{DUT}} - T_{c_\mathrm{DUT}}}}{\frac{N_{h_\mathrm{NFtest_system}} - N_{c_\mathrm{NFtest_system}}}{T_{h_\mathrm{NFtest_system}} - T_{c_\mathrm{NFtest_system}}}} \tag{11}$$

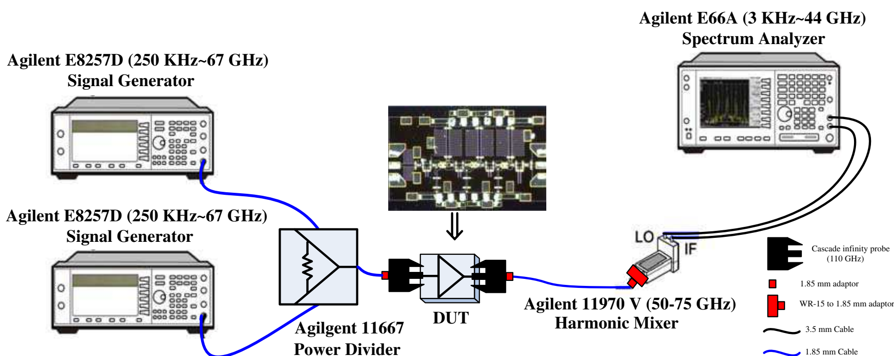

Figure 8. Test setup and procedure of MMW amplifier IIP3 measurement.

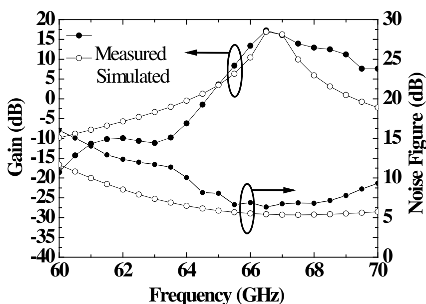

Figure 9. Measured and simulated small signal gain and noise figure versus input frequency.

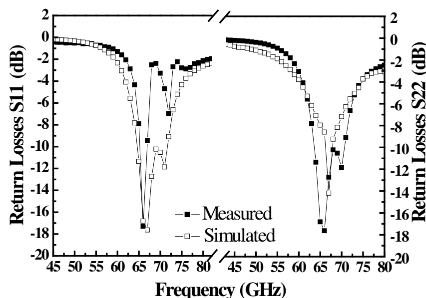

Figure 10. Measured and simulated input/output return losses of EBG-CPW LNA.

From the Y-factor derivation

$$\begin{aligned}\mathrm{NF} &= 10\log\left(\frac{T_h}{T_c}-1\right)-10\log(Y-1)=ENR(RF)-10\log\left(\frac{N_h-N_c}{N_c}\right)\\ &= ENR(RF)-ENR(IF)\end{aligned} \tag{12}$$

For further discussion, the building blocks of the on-wafer IIP3 test system are depicted in details and shown in Fig. 8. A third-order intercept point is a measure for weakly nonlinear systems and devices, for example receivers, linear amplifiers and mixers. It is based on the idea that the device nonlinearity can be modeled using a low-order polynomial, derived by means of Taylor series expansion. The third-order intercept point relates nonlinear products caused by the third-order nonlinear term to the linearly amplified signal, in contrast to the second-order intercept point that uses second order terms.

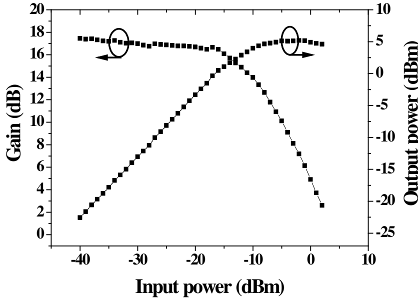

Figure 11. Measured 1 dB power gain compression point.

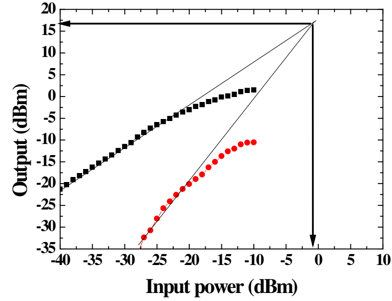

Figure 12. Measured third-order interception point.

Table 3. Comparison table of various V-band LNAs.

Process	Freq. (GHz)	Peak Gain (dB)	NF (dB)	P_{DC} (mW)/V_{DD}	IIP3 (dBm)	Size (mm^2)
[7] CMOS 90 nm	64	15.5	6.5	86	NA	0.52
[8] CMOS 65 nm	60	11.5	5.6	72	NA	0.601
[9] CMOS 90 nm	60	13	7	42	NA	0.315
[10] CMOS130nm	60	12	8.8	54	NA	1.43
[11] GaAs150 nm	60	14	5	NA	NA	0. 9
[12] GaAs HBT	60	25	5.8	NA	NA	1. 6
[13] GaAs 130 nm	60	14	6	NA	NA	0.85
[14] GaAs 150 nm	24.5	20	3.5	106	NA	1
[15] GaAs 200 nm	2.4	15.1	3.8	NA	–3	3
This work	66	17 .3	6.3	75	–0.51	0.96

The V-band EBG TLines LNA chip measured through on-wafer probing. Fig. 9 shows the measured and simulated small signal gain and noise figure versus input frequency from 60 to 70 GHz at 3 V drain bias with total current of 27 mA. The related stability K-factor is greater than 1. Fig. 10 shows the measured and simulated input/output retune losses of EBG-CPW LNA. The measured small signal gain has an amplifier peak gain of 17.3 dB at 66 GHz. The minimum input and output return losses are −16 dB and −18 dB, respectively. The noise figure at the same bias condition exhibits a minimum of 6.21 dB at 66 GHz. The 1-dB power gain compression point and third-order interception point at 66 GHz are measured and plotted in Figs. 11 and 12, respectively. The measured output 1-dB compression point of the amplifier is 0.6 dBm and input IP3 is −0.5 dBm at 60 GHz. The total dc power consumption is 75.2 mW.

The performance of the reported LNA is compared to that of the

similar LNAs in Table 3. Note the lower power consumption and lower noise figure of the reported circuit compared to the V-Band. In spite of the TL matching network used in our chip its size is comparable to circuits using lumped inductor based matching networks.

5. CONCLUSION

A high performance and a compact size V-band LNA was implemented in 0.15-μm baseline GaAs pHEMT process. It exhibited a gain of 17.3 dB and noise figure of 6.21 dB at 66 GHz operation, and the dc power consumption is only 75 mW. The matching networks were based on high Q EBG TLines. The EBG TLines approach enabled us to improve the circuit performance of in standard GaAs foundry service fabrication, and to compete well with similar LNAs fabricated by more advanced technologies.

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REFERENCES

1. Gunnarsson, S. E., et al., "60 GHz single-chip front-end MMICs and systems for multi-Gb/s wireless communication," *IEEE Journal of Solid State Circuit*, Vol. 42, No. 5, 1143–1157, May 2007.
2. Yang, B., X. F. Jin, X. M. Zhang, H. Chi, and S. L. Zheng "Photonic generation of 60 GHz millimeter-wave by frequency quadrupling based on a mode-locking SOA fiber ring laser with a low modulation depth MZM," *Journal of Electromagnetic Waves and Applications*, Vol. 24, No. 13, 1773–1782, Jan. 2010
3. Liu, Y., J. Xu, Y.-Y. Wei, X. Xu, F. Shen, M. Huang, T. Tang, W.-X. Wang, Y.-B. Gong, and J. Feng, "Design of a V-band high-power sheet-beam coupled-cavity traveling-wave tube," *Progress In Electromagnetics Research*, Vol. 123, 31–45, 2012.
4. Chowdhury, D., P. Reynaert, and A. M. Niknejad, "A 60 GHz 1 V +12.3 dBm transformer-coupled wideband PA in 90 nm CMOS," *ISSCC Dig. Tech. Papers*, 560–561, Feb. 2008.

5. Moghadasi, S. M., A. R. Attari, and M. M. Mirsalehi, "Compact and wideband 1-D mushroom-like EBG filters," *Progress In Electromagnetics Research*, Vol. 83, 323–333, 2008.
6. Agilent Technologies, "Noise figure measurement accuracy — The Y-factor method," Application Note 57-2, Mar. 2004.
7. Pellerano, S., et al., "A 64 GHz LNA with 15.5 dB Gain and 6.5 dB in 90 nm CMOS," *IEEE Journal of Solid State Circuit*, Vol. 43, No. 7, 1542–1552, Jul. 2008.
8. Varonen, M., M. Kärkkäinen, and K. A. I. Halonen, "Millimeter-wave amplifiers in 65-nm CMOS," *Eur. Solid-State Circuit Conf.*, 280–283, Sep. 2007.
9. Lin, J.-J., K.-H. To, B. Brown, D. Hammock, M. Majerus, M. Tutt, and W. M. Huang, "Wideband PA and LNA for 60-GHz radio in 90-nm LP CMOS technology," *Compound Semicond. Integr. Circuits Symp.*, 1–4, Oct. 2008.
10. Doan, C. H., S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS design," *IEEE Journal of Solid State Circuit*, Vol. 40, No. 1, 144–155, Jan. 2005.
11. Fujii, K., M. Adamski, P. Bianco, D. Gunyan, J. Hall, R. Kishimura, C. Lesko, M. Schefer, S. Hessel, H. Morkner, and A. Niedzwiecki, "A 60 GHz MMIC chipset for 1-Gbith/s wireless links," *IEEE MTT-S International Microwave Symposium Digest*, Vol. 3, 1725–1728, Jun. 2–7, 2002.
12. Handa, S., E. Suematsu, H. Tanaka, Y. Motouchi, M. Yagura, A. Yamada, and H. Sato, "60 GHz-band low noise amplifier and power amplifier using InGaP/GaAs HBT technology," *25th Annual Technical Digest IEEE Gallium Arsenide Integrated Circuit (GaAs IC) Symposium*, 227–230, 2003.
13. Onodera, K., S. Sugitani, K. Nishimura, and M. Tokumitsu "V-band monolithic low-noise amplifiers using ion-implanted n^+-self-aligned GaAs MESFET's," *IEEE Microw. Guided Wave Lett.*, Vol. 9, No. 4, 148–150, Feb. 1999.
14. Luo, S.-M., R.-Y. Hung, S.-H. Weng, Y.-L. Ye, C.-N. Chuang, C.-H. Lin, and H.-Y. Chang, "24-GHz MMIC development using 0.15-μm GaAs PHEMT process for automotive radar applications," *IEEE Asia Pacific Microwave Conf., APMC*, 2008.
15. Ahsan, N., J. Dabrowski, and A. Ouacha,"A self-tuning technique for optimization of dual band LNA," *Proc. of the 1st European Wireless Technology Conf., EuWiT*, 2008.