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A DISTRIBUTED VARIABLE DELAY LINE FOR WIDEBAND BEAM-FORMERS

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Abstract—A fully integrated CMOS wideband distributed variable delay line for time array beam-formers is presented. The delay line works over a full differential mode, and the delay cell function is based on differential amplifiers with active inductive peaking loads. A delay resolution of 15 ps is obtained with a maximum delay capability of 150 ps. The designed active delay line provides 3 scanning angles with 8.6° of spatial resolution. This delay line is applicable for a 4 channel beam-former with an operational bandwidth of 500 MHz centered at 5 GHz. Our active delay line consumes up to 352 mW of power from a 2.5 V supply. The circuit is simulated in standard 0.25 µm BiCMOS process and occupies 252 µm × 123 µm of silicon area.

1. INTRODUCTION

Antenna arrays have been used for over half a century in various military communications and radar applications. There is a recent surge of interest in using antenna arrays for commercial applications. Broadly speaking, there are two categories of antenna arrays: those used for beam-forming and those used for spatial diversity [6–9]. In the first type, also referred to as phased arrays in narrowband systems or time arrays in wideband systems, a linear summation of complex-weighted signals is formed to create an appropriate beam and enable spatial selectivity [10]. Complex-weighted signals in radio frequency are achieved by changing the gain and phase of each channel that follows an antenna element. The shape of the beam and the direction of the main lobe depend on amplitude and phase settings, and both are electronically controlled. Beam-formers are used to create a line-of-sight connection between a transmitter and a receiver [11, 12].

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Beam-former transmitters limit their emission to specific angles, while beam-former receivers can reject interference signals from unwanted directions, while receiving with high gain at the desired direction.

In a phased array receiver, the received signal arrives at each element of the array at a different moment in time. For narrowband systems with a fractional bandwidth less than 0.1, time difference can be approximated using phase shifters. On the other hand, time difference in wideband systems with a bandwidth greater than 500 MHz need a time delay element to compensate for the delay at each channel [1]. The fractional bandwidth is defined as:

$$Fractional\ (BW) = \frac{2(f_H - f_L)}{(f_H + f_L)} \tag{1}$$

This paper presents a *distributed variable delay line* (DVDL) for wideband beam-formers. Section 2 reviews the fundamentals of time delay architectures. Section 3 presents the design methodology and associated circuitry of the new delay line. Section 4 presents and discusses the simulation results and performance of the variable delay line. The layout of the DVDL line is presented in Section 5, and finally Section 6 provides a conclusion for this paper.

2. BEAMFORMERS AND DELAY LINE CONCEPT

A phased array receiver is a multi-antenna transceiver which coherently combines the signals coming from all channels. For simplicity and convenience, the discussion here will be limited to a linear, one-dimensional, uniform array receiver. A block diagram of a time delay four-antenna receiver is shown in Fig. 1. A received wave with an angle of arrival, θ, reaches each one of the 4 antennas at different moments in time [2].

The delay difference, τ, is a function of the angle of arrival θ, the speed of light c, and the antenna spacing d, and is given by:

$$\tau = \frac{d \sin\theta}{c} \tag{2}$$

If $S_0(t)$ represents the received signal at the first element of the array, then the signal at the nth array element is given by:

$$S_n(t) = S_0(t - n\tau) \tag{3}$$

The summed total signal, $S_{tot}(t)$, is the superposition of the received signals at each antenna, S_n, and is given as:

$$S_{tot}(t) = \sum_{n=0}^{3} S_n(t - \tau_{cn}) \tag{4}$$

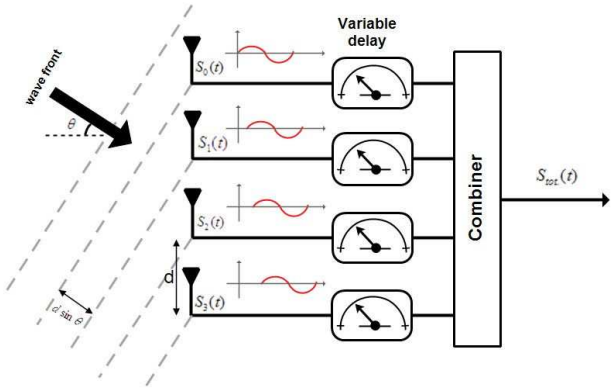

Figure 1. Four channels beam-former with time delay architecture.

where τ_{cn} is the amount of compensated delay in the nth received channel and the required amount of delay between neighboring elements, τ_c [1].

3. DVDL DESIGN

A variable delay element is presented using a differential pair of NMOS transistors with inductive peaking as shown in Fig. 2. The delay is a function of the steering current I_{ss}, output voltage swing ΔV, and load capacitance C_L [4], as given below

$$\tau = \frac{\Delta V}{I_{ss}} C_L \tag{5}$$

For a delay line implementation using this topology, each delay element should drive another one, then the load capacitance presented by C_{gs} of Q_1 and Q_2 can be controlled by the size of these transistors. Usually active loads are preferred instead of passive inductors, since passive inductors occupy a very large area. In Fig. 2, Q_5 and Q_6 are PMOS transistors that work as active resistors connected to Q_3 and Q_4 NMOS transistor load. Gain and bandwidth are controlled with this inductive peaking active load which is adjustable by controlling the size of the PMOS transistors [5]. Fig. 3 presents the equivalent small signal model of the active inductive peaking circuit. The input impedance of the active inductive circuit can be described as

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1 + sR_{eq}C_{gs}}{g_m + sC_{gs}} \tag{6}$$

Table 1. Dimensions of transistors.

	W (in μm)	L (in μm)
Q_1	10	0.25
Q_2	10	0.25
Q_3	10	0.25
Q_4	10	0.25
Q_5	30	0.25
Q_6	30	0.25

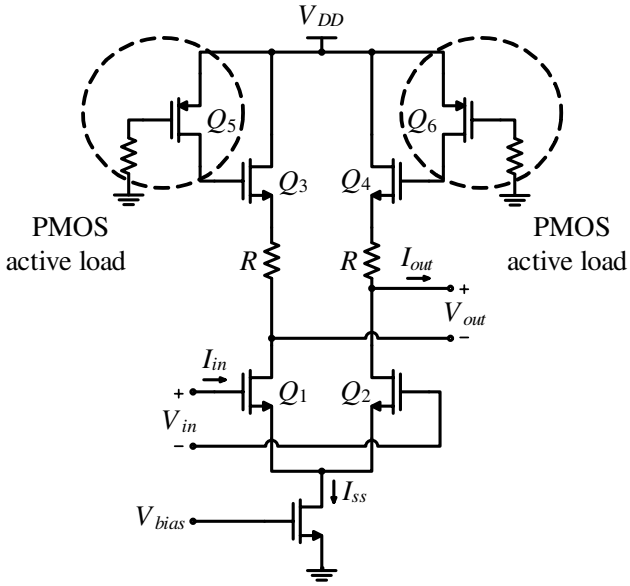

Figure 2. Active delay element.

where R_{eq} denotes the equivalent resistive load Q_5, g_m represents the transconductance of the amplifier, and C_{gs} equals the Q_3 gate-source parasitic capacitance in Fig. 3. The input impedance behaves as a series L-R network, where the input impedance Z_{in} increases with frequency [5].

Table 1 gives the width and length of each transistor used in the designed DVDL element circuit. To ensure stability and high speed response all these transistors must work in the saturation region.

Most of the designs of variable delays used for beam-forming are based on lumped element transmission line implementation with

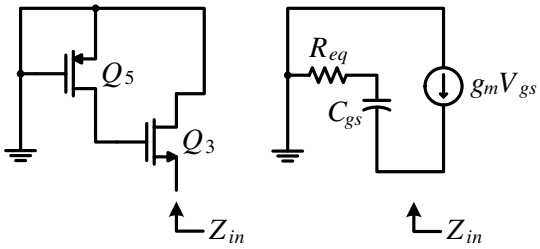

Figure 3. Inductive peaking equivalent circuit.

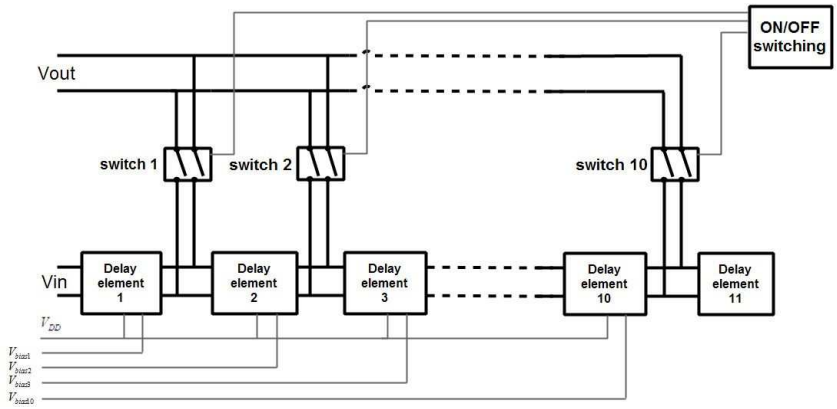

Figure 4. Variable delay line architecture.

variable path controlling the delay [1]. These designs consume large silicon on-chip area and use spiral inductors with low quality factors. The efficiency of these spiral inductors is frequency dependent; in Giga hertz frequencies passive inductors have low efficiency [3]. To the best of our knowledge, this paper introduces the first active delay line operating with 500 MHz bandwidth centered at 5 GHz. Fig. 4 proposes a DVDL line with 10 variable delays. Each delay element circuit is as shown in Fig. 2. The delay resolution of a single element is 15 ps and the maximum delay is ten times that. Delay element 11 in Fig. 4 is added for matching purposes only. Adjustable delay is obtained by controlling the path of the signal between the input and the output using switches. These switches are a couple of NMOS transistors that work as ON/OFF switch. The ON state is when the Gates of the transistors are supplied with 2.5 V, and the OFF state when supplied by 0 V. For example, if we need a delay of 30 ps, switch 2 is turned ON by a 2.5 V supply and delay elements 1 and 2 are turned ON by supplying V_{bias1} and V_{bias2} with 2.5 V. This is a single channel delay line for a wideband beam-former.

4. SIMULATION RESULTS

Accurate MOSFET models at RF will enable better prediction of the simulation. Thus BSIM3v3.2 was used in this work and model parameters were obtained from TSMC. Fig. 5 shows the simulated delay obtained from all paths of the delay line. After simulating the same delay element at different frequencies, the delay is varying correspondingly with frequency. For a band of frequencies between 4.5 GHz and 5.5 GHz delay is varying from 15.3 ps to 15 ps respectively. Fig. 6 shows the curve of delay variation versus frequency change. We have a maximum delay of 17 ps at 1 GHz and a minimum delay of 14 ps at 8 GHz.

The Delay step is defined as the delay difference between two neighboring switches of the DVDL line of Fig. 4. One delay step equals to 15 ps, see Fig. 5. The minimum delay of this line is 15 ps when switch 1 is ON only, and the maximum delay is 150 ps when switch 10 is ON only. In other words:

$$Delay\ step = m_n - m_{n-1} \quad n = 2,\ 3,\ 4,\ \ldots, 11$$
$$Minimum\ delay = m_2 - m_1$$
$$Maximum\ delay = m_{11} - m_1$$

For an array of four elements and an antenna spacing of half wavelength at 5 GHz, the minimum scanning angle occurs at minimum

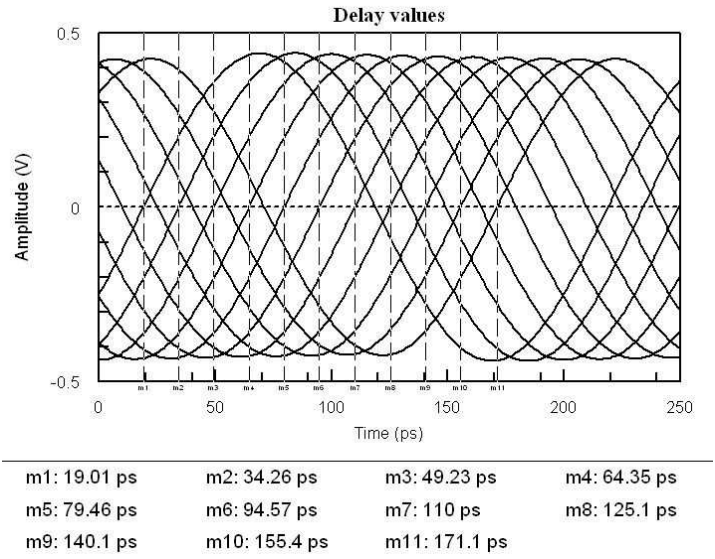

Figure 5. Variable delay obtained from all paths.

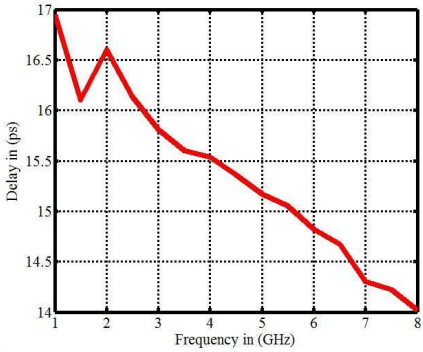

Figure 6. Delay variation versus frequency.

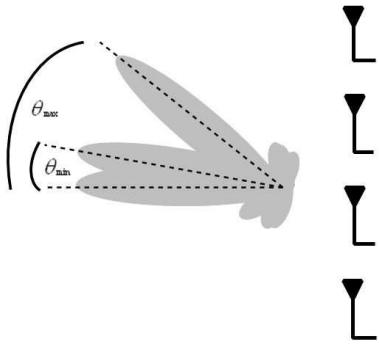

Figure 7. Discrete angle steps for 4-element beam-former.

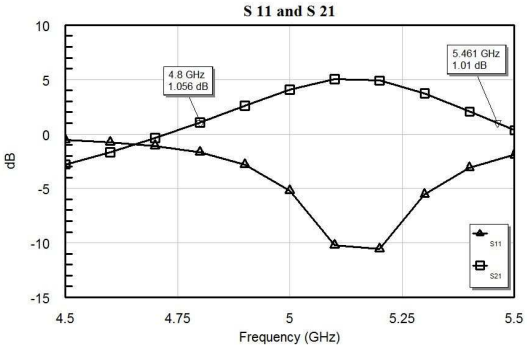

Figure 8. S_{11} and S_{21} in dB.

delay of 15 ps, as:

$$\tau_{\min} = \frac{1}{2f} \sin\theta_{\min} = 15\,\text{ps} \Rightarrow \theta_{\min} = 8.6^{\circ} \tag{7}$$

While the maximum scanning angle is obtained from the maximum delay divided by $(N-1)$, where N is number of antenna elements in the array:

$$\frac{\tau_{\max}}{(N-1)} = \frac{1}{2f} \sin\theta_{\max} = \frac{150\,\text{ps}}{(4-1)} \Rightarrow \theta_{\max} = 30^{\circ} \tag{8}$$

Figure 7 shows the scanning angle resolution of a 4-element array beam-former using the proposed DVDL in this paper. We have 3 different scanning angles (8.6°, 17.5°, 26.7°) which are between the minimum of 8.6° and the maximum of 30°.

All 10 delay elements are connected to each other in a series form. Since all delay elements are identical, each delay element output is matched with the input of the next delay element. In order to match the input of the delay line with 50 Ω an LC matching network can be used.

Figure 8 represents the input return loss S_{11} and the gain S_{21} of the matching network with the DVDL line. We have an operation band between 4.8 GHz and 5.46 GHz with gain varying from 1–5 dB. Fig. 9 represents the reverse isolation, S_{12}, of the matching network with a value that does not exceed −5 dB.

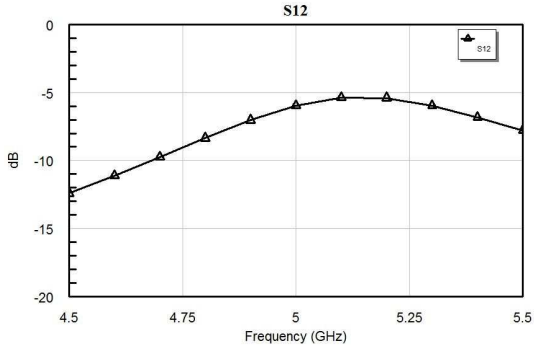

Figure 9. S_{12} in dB.

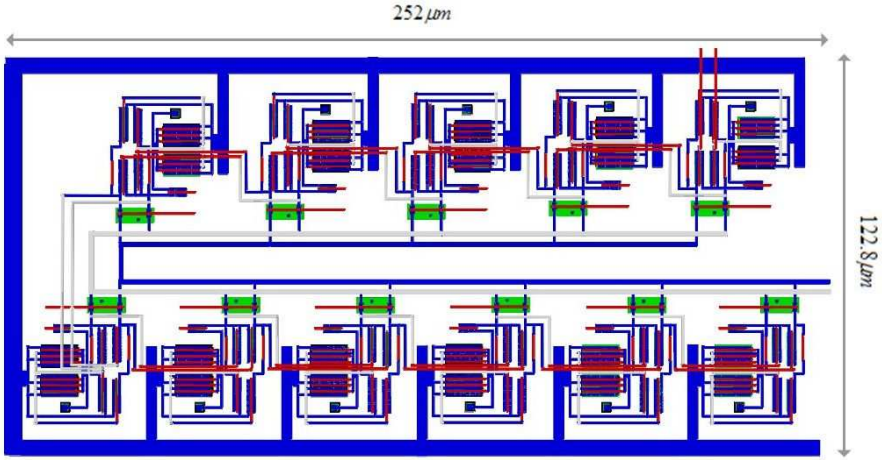

Figure 10. Layout view of designed TTD line.

5. LAYOUT

A proposed integrated circuit layout with 0.25 BiCMOS process was carried out. Fig. 10 shows the design layout of the DVDL which consists of 10 delay elements with 1 delay element at the final stage for matching purposes. The layout consumes a silicon area of (122.8 μm × 252 μm).

6. CONCLUSION

A silicon distributed variable delay line for wideband beam-formers suitable for short range wireless communications has been introduced, and discussed. The DVDL architecture eliminates the bandwidth limited phase shifter implementations in traditional phase shifters. An active DVDL design proposed in this paper replaces the need for a passive delay line that uses passive lumped elements to implement a transmission line. Each delay element consumes around 32 mW from a 2.5 V supply, and occupies a silicon area of (35 μm × 35 μm). The total silicon area occupied by the whole DVDL equals to (122.8 μm × 252 μm).

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