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A 10:1 UNEQUAL GYSEL POWER DIVIDER USING A CAPACITIVE LOADED TRANSMISSION LINE

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Abstract—This paper proposes a 10 : 1 unequal Gysel power divider using a capacitive loaded transmission line (CLTL). For obtaining a high dividing ratio of divider, the CLTL is proposed to realize a low characteristic impedance line below 10 Ω. A design method using a CLTL which consists of a small transmission line with shunt open stub at periodic intervals is newly suggested for power divider with the high power division ratio. For the validation of the CLTL power divider, the high dividing ratio of the fabricated Gysel divider is measured at a center frequency of 1 GHz. The measured performances are in good agreements with simulation results.

1. INTRODUCTION

A power divider and a combiner are the key components in RF and microwave systems. The Wilkinson power divider is used in low power ranges. If it is used at a high power, it requires a high-power isolation resistor. Because the high-power resistor has parasitic inductance and capacitance elements, the isolation resistor must have a matching circuit. Therefore, the high power Wilkinson divider is difficult fabrication. However, the Gysel power divider is used in high power ranges because the isolation resistor is attached to an independent power-dividing port. Therefore, when a phase-array antenna system requires a high-power divider, we will use a Gysel power divider. In this system, the divider needs to have a high dividing ratio of divider. However, if the power ratio increases, the high characteristic impedance lines are not possible to fabricate a microstrip line because of the narrow width of the transmission line. As a solution to the fabrication

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problem, many new structures have recently been reported for the realization of a high characteristic impedance line, such as a coupled line section with two shorts [1] or a defected ground structure [2] or offset double side parallel-strip lines [3] or different impedance lines attached to an open-/short-terminated stub [4]. However, the performance of these methods isn't better than a single transmission-line section.

In this paper, to overcome the conventional problem, a realizable highest characteristic impedance of the transmission-line sections sets arbitrarily. Then, to realize other low impedance lines for a high dividing ratio divider, we investigate the structure of a capacitive loaded transmission line (CLTL). To design an unequal Gysel power divider with a high dividing ratio using CLTL, we changed the input impedances of the output ports. Also, transmission lines with periodic shunt capacitive loading [5–7] were employed to realize the required low characteristic impedance lines. This configuration can transform a low impedance line into a high impedance line with capacitive loading and compact size. As an example, a 10 : 1 unequal Gysel divider at 1 GHz was designed, fabricated, and measured.

2. THEORY AND DESIGN

2.1. Unequal Gysel Power Divider

For a high dividing ratio power divider, we propose a modified unequal Gysel power divider [8, 9]. Fig. 1 shows the Gysel power divider with unequal power division at the output ports 2 and 3. The electrical length at the operating center frequency of transmission line is $\pi/2$

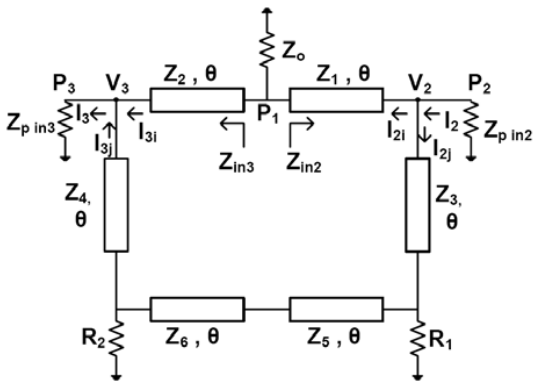

Figure 1. Conventional N : 1 unequal two-way Gysel power divider.

The high power resistors R_1 and R_2 are connected to the ground plane with the dividing ratio value.

In order to fulfill the power divider ratio ($P_3/P_2 = k^2$), the input impedances observed at port 1 followed by the two branches must satisfy the following expressions

$$Z_{pin2} = k^2 Z_{pin3} \tag{1}$$

$$Z_{in2} = k^2 Z_{in3} \tag{2}$$

In addition, in order to obtain a matched port 1 with a characteristic impedance of Z_o, the input impedances must be

$$Z_o = Z_{in2}//Z_{in3} = \frac{k^2}{1+k^2} Z_{in3} \tag{3}$$

Combining Eqs. (2) and (3), these two input impedances can be written as

$$Z_{in2} = \left(1+k^2\right) Z_o \tag{4}$$

$$Z_{in3} = \frac{1+k^2}{k^2} Z_o \tag{5}$$

The impedances at ports 2 and 3 are defined as

$$Z_{pin2} = \frac{Z_o}{k} \text{ and } Z_{pin3} = \frac{Z_o}{k^3} \tag{6}$$

To satisfy the lossless power division and transmission, in Fig. 1, when the input port 1 is excited, the circuit structure can be considered to the equivalent circuit shown in Fig. 2.

Because the electrical lengths of transmission line in Fig. 2 are equal to $\pi/2$, this circuit operates the quarter-wavelength transformers, and their characteristic impedances can be written as

$$Z_1 = \sqrt{\frac{1+k^2}{k}} Z_o \tag{7}$$

$$Z_2 = \sqrt{\frac{1+k^2}{k^5}} Z_o \tag{8}$$

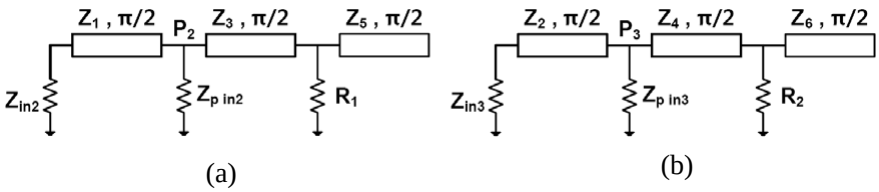

Figure 2. Equivalent circuit of unequal Gysel power divider when port 1 is excited.

By applying the transmission matrix concept into Fig. 1, the relationship between voltages and currents can be derived

$$\begin{pmatrix} V_2 \\ I_{2i} \end{pmatrix} = \begin{pmatrix} A_{i1} & B_{i1} \\ C_{i1} & D_{i1} \end{pmatrix} \begin{pmatrix} V_3 \\ I_{3i} \end{pmatrix} \tag{9a}$$

$$\begin{pmatrix} V_2 \\ I_{2j} \end{pmatrix} = \begin{pmatrix} A_{j1} & B_{j1} \\ C_{j1} & D_{j1} \end{pmatrix} \begin{pmatrix} V_3 \\ I_{3j} \end{pmatrix} \tag{9b}$$

$$I_2 = I_{2i} + I_{2j}, - \quad I_3 = I_{3i} + I_{3j} \tag{9c}$$

The ABCD parameters of above equations may be expressed by (10) as

$$\begin{pmatrix} A_{i1} & B_{i1} \\ C_{i1} & D_{i1} \end{pmatrix} = \begin{pmatrix} -Z_1Y_2 & -Z_1Z_2Y_o \\ 0 & -Z_2Y_1 \end{pmatrix} \tag{10a}$$

$$\begin{pmatrix} A_{j1} & B_{j1} \\ C_{j1} & D_{j1} \end{pmatrix} = \begin{pmatrix} \frac{1}{k^2}Z_3Y_4 & Z_3Z_4\left(k^2\frac{1}{R_1} + \frac{1}{k^2}\frac{1}{R_2}\right) \\ 0 & k^2Y_3Z_4 \end{pmatrix} \tag{10b}$$

If the signal is excited at port 2, the perfect isolation and matching condition of divider is $I_3 = 0$ and $V_3 = 0$. Then, combining (9) with this condition result in

$$B_{i1} + B_{j1} = 0 \tag{11a}$$

$$Z_{pin2} = \frac{V_2}{I_2} = \frac{B_{i1}}{D_{i1} - D_{j1}} \tag{11b}$$

After some algebraic manipulations, the (6)–(10) can lead to the final mathematical design expressions as follows:

$$Z_3 = \frac{Z_o}{k}, \quad Z_4 = \frac{Z_o}{k^3}, \text{ and } R_1 = \frac{Z_o}{k} \tag{12a}$$

$$Z_5 = \frac{Z_o}{k}, \quad Z_6 = \frac{Z_o}{k^3}, \text{ and } R_3 = \frac{Z_o}{k^3} \tag{12b}$$

Note that when a signal is excited from port 3, port 2 should be isolated effectively. In this case, the condition becomes $I_2 = 0$ and $V_2 = 0$. Due to the reciprocity property for passive circuit, the derived equations are the same as (10). Therefore, the design (11) makes the Gysel power divider to produce perfect output port matching and isolation.

If the power ratio $k^2 = 10$, then according to theory, the characteristic impedances of the transmission lines and resistors of the unequal Gysel divider are $Z_1 = 93.25\,\Omega$, $Z_2 = 9.33\,\Omega$, $Z_3 = 15.8\,\Omega$, $Z_4 = 1.58\,\Omega$, $Z_5 = 15.8\,\Omega$, $Z_6 = 1.58\,\Omega$, $R_1 = 15.8\,\Omega$ and $R_2 = 1.58\,\Omega$. If we make impedances of below $10\,\Omega$, the microstrip fabrication technique cannot be used because of the large width of the transmission line. Hence, the CLTL is used to achieve a low impedance line.

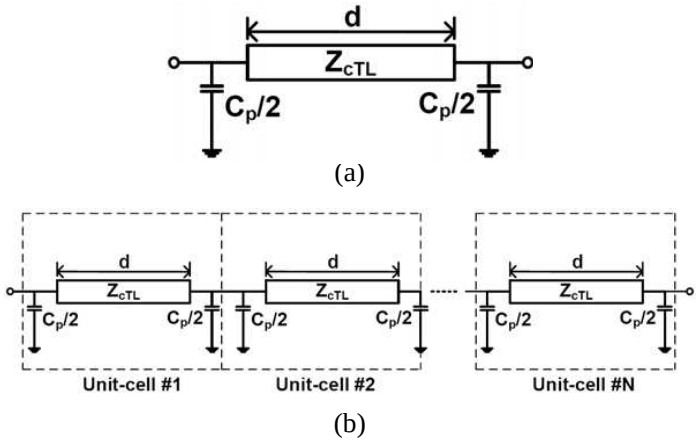

Figure 3. (a) Equivalent circuit of unit cell of CLTL. (b) Cascade connection of CLTL unit cells.

2.2. Capacitive Loaded Transmission Line (CLTL)

A CLTL consists of N unit-cells, and the transmission line has a spacing d that is shorter than the guided wavelength and the shunt capacitance, as shown in Fig. 3.

Because of the slow wave characteristics, the CLTL can be used to reduce the physical length of the transmission line and to realize low impedance lines using small transmission line and shunt open stub at periodic intervals The CLTL behaves as a transmission line with an effective characteristic impedance Z_{oCLTL} and phase velocity v_{oCLTL} given by

$$Z_{oCLTL} = \sqrt{\frac{L}{(C + C_P/d)}} \tag{13}$$

And

$$v_{oCLTL} = \frac{1}{\sqrt{L(C + C_P/d)}} \tag{14}$$

where L and C are the distributed inductance and capacitance of the transmission line, respectively.

The characteristic impedance (Z_{cTL}) and phase velocity (v_{cTL}) of the transmission line are given, respectively, by

$$Z_{cTL} = \sqrt{\frac{L}{C}} \tag{15}$$

And

$$v_{cTL} = \frac{1}{\sqrt{LC}} \tag{16}$$

Comparing the characteristics of the CLTL and a conventional transmission line, it is found that the CLTL has a low effective characteristic impedance and phase velocity. Hence, the CLTL can convert a low impedance line to a high impedance line. Moreover, the low phase velocity of the CLTL leads to a reduction in physical size. The CLTL has N unit cells, and its electrical length is

$$\theta_{CLTL} = 2\pi f_o N d \sqrt{L\left(C + \frac{C_P}{d}\right)} \tag{17}$$

where f_o is the frequency of interest.

In order to design a CLTL, we can calculate the transmission line length d and capacitance C_p for a given transmission line (Z_{cTL} and v_{cTL}) and given values (Z_{oCLTL} and v_{oCLTL}) of the CLTL as follows:

$$d = \frac{Z_{oCLTL} \cdot \theta_{CLTL} \cdot v_{cTL}}{2\pi \cdot f_o \cdot N \cdot Z_{cTL}} \tag{18}$$

$$C_p = \frac{\theta_{CLTL} \cdot (Z_{cTL}^2 - Z_{oCLTL}^2)}{2\pi \cdot f_o \cdot N \cdot Z_{cTL}^2 \cdot Z_{oCLTL}} \tag{19}$$

The loading capacitance can be realized by shunt open stubs;

$$2\pi \cdot f_o \cdot C_p = \frac{1}{Z_{OS}} \cdot \tan\left(\frac{2\pi f_o}{v_{OS}} \cdot l\right) \tag{20}$$

where Z_{OS} and v_{OS} are the characteristic impedance and phase velocity, respectively, of the open stub transmission lines, and l is the open stub length.

According to the CLTL design method, the low characteristic impedances of $9.33\,\Omega$, $8.89\,\Omega$, $15.8\,\Omega$ and $21.6\,\Omega$ can be changed to high impedance lines above $24\,\Omega$.

3. SIMULATION AND EXPERIMENTAL RESULTS

3.1. Design and Simulation

In order to validate the high dividing ratio power divider, we simulated the power ratio $k^2 = 10$. Because the microstrip fabrication technique cannot be used below $10\,\Omega$, we had to use a CLTL. Table 1 lists the CLTL elements that made up the transmission line using a Teflon substrate with $\varepsilon_r = 2.2$ and a height (h) of 0.787 mm; the

Table 1. CLTL Microstrip line — element dimensions for low characteristic impedances.

	Z_{oCLTL} $= 21.6\,\Omega$	Z_{oCLTL} $= 15.8\,\Omega$	Z_{oCLTL} $= 9.3\,\Omega$	Z_{oCLTL} $= 1.58\,\Omega$
W_{cTL} (mm)	4.0	4.0	5.2	6.5
d (mm)	4.6	4.6	4.6	1.0
W_{cOS} (mm)	1.0	1.0	1.0	0.5
L_{OS} (mm)	30	30	38	50
N	5	5	5	5

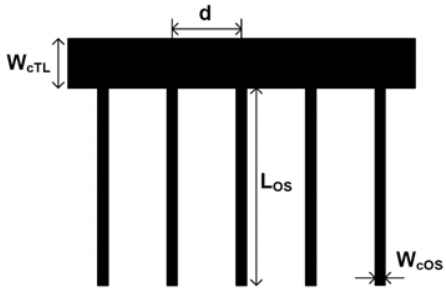

Figure 4. Configuration of a CLTL.

design frequency was $f_o = 1.0\,\text{GHz}$ and the open stub characteristic impedances for the line width and length corresponding to Fig. 4.

Table 1 lists the element dimensions for low characteristic impedances of $9.33\,\Omega$, $8.89\,\Omega$, $15.8\,\Omega$ and $21.6\,\Omega$ which is $\lambda/4$ transformer impedance between impedance Z_2 and port P_3 impedance $50\,\Omega$. These values are the calculation results with $N = 5$.

The simulation results are presented in Fig. 5; the simulation was carried out using the ADS software developed by Agilent, with the center frequency set to 1.0 GHz. For a return loss of 10 dB, the relative bandwidth was about 7%. From Fig. 5, the S-parameters at 1 GHz are $|S_{11}| = -35\,\text{dB}$, $|S_{21}| = -9.7\,\text{dB}$, $|S_{31}| = -0.77\,\text{dB}$, and $|S_{32}| = -22.8\,\text{dB}$. In addition, the phase difference of the output ports has a tolerance of about $\pm 1.0°$.

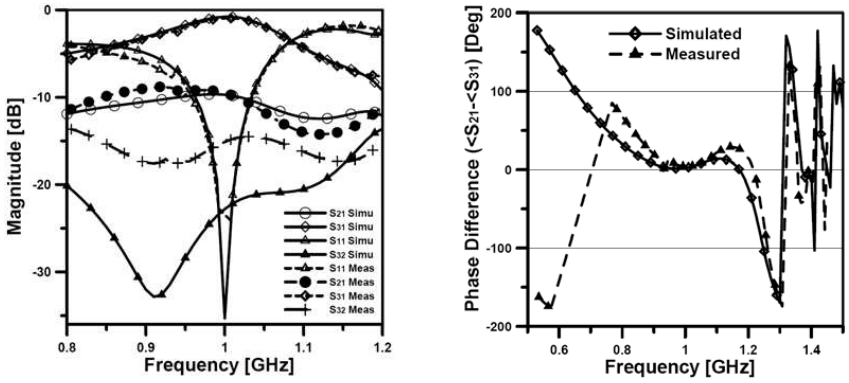

Figure 5. Characteristics of simulated and measured results. (a) S-parameters. (b) Phase difference of S_{21} and S_{31}.

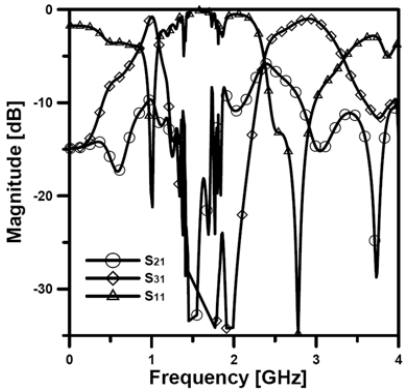

Figure 6. Simulation results of harmonic characteristics of the unequal divider.

In Fig. 6, because of the non-periodic structure of the CLTL with open stub capacitive loading and the distributed capacitance of the transmission line, the harmonic characteristics of the unequal Gysel divider using the CLTL do not appear.

3.2. Fabrication and Measurement Results

A photograph of the implemented unequal Gysel divider is shown in Fig. 7. The unequal Gysel divider was implemented using microstrip

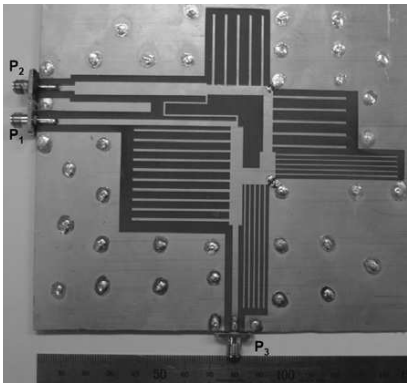

Figure 7. Photograph of the implemented unequal Gysel divider.

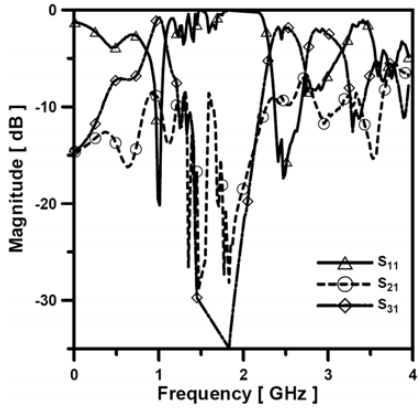

Figure 8. Measured results of harmonic characteristics of the unequal divider.

technology on a Teflon substrate with $\varepsilon_{\mathrm{r}} = 2.2$ and a height (h) of 0.787 mm; the design frequency was $f_{\mathrm{o}} = 1.0$ GHz.

The measurement data of the high dividing unequal Gysel power divider are shown in Fig. 5. It is seen that the simulated and measured data almost coincide.

From Fig. 5, $|S_{21}|$ are -9.6 dB and $|S_{31}|$ are -0.9 dB. This small disagreement is due to the ignored substrate loss and the approximated components. The isolation parameters of $|S_{23}|$ are -15.2 dB. The return losses of $|S_{ii}|$, where $i = 1, 2, 3$ are below 15 dB. Also, the output port has a phase difference of 2° at 1 GHz.

In Fig. 8, the harmonic frequencies of the unequal Gysel divider do not appear because of the non-periodic structure of the CLTL.

4. CONCLUSION

In this paper, we have presented the theoretical design and practical implementation of a high dividing ratio unequal Gysel power divider with a CLTL. The CLTL enabled us to achieve low characteristic impedances of below 10 Ω. The fabricated 10 : 1 divider had excellent matching and isolation, exact dividing ratios of -9.6 dB and -0.9 dB, and a phase difference of about 2° at output ports 2 and 3 at a center frequency of 1.0 GHz.

This design method can be used to implement low characteristic impedance line for RF and microwave components.

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