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AN INVESTIGATION OF TRADEOFF OPTIONS FOR THE IMPROVEMENT OF SPURIOUS-FREE DYNAMIC RANGE IN HBT TRANSIMPEDANCE DISTRIBUTED AMPLIFIERS

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Abstract—This work introduces and investigates various methods of improving spurious-free dynamic rage (SFDR) in HBT transimpedance distributed amplifiers by trading off transimpedance gain. The methods are theoretically analyzed in detail with design examples, compared against each other in terms of performance and the best tradeoff is determined. SFDR improvements of up to 9 dB are reported in our design examples.

1. INTRODUCTION

The design of transimpedance amplifiers for photoreceivers has made remarkable strides in recent times, especially Optoelectronic Integrated Circuit (OEIC) implementations on InP, where the photodetector and transimpedance amplifier are integrated together on the one chip [1–3]. Receivers capable of up to 100 V/W optoelectronic gain at a 46.5 GHz optoelectronic bandwidth were realized using InP HBTs [3], which are more attractive compared to InP HEMTs for optoelectronic applications as the device structures are highly compatible with high-performance PIN diode photodetectors.

Until now, most works focusing on OEIC receivers concentrated on the gain, bandwidth and noise performance, due to their importance in digital applications. Works focusing on linearity, particularly on the Spurious-free Dynamic Range (SFDR) of OEIC receivers on the other hand have been few and far between. The prospect of such photonic systems being implemented in electronic warfare platforms has resulted

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in the dynamic range of such systems becoming a research priority in recent times. However, defense applications such as these require the system to feature high bandwidth, low noise, high linearity and high dynamic range.

The dynamic range in analog photonic links is currently limited primarily by the linearity of the optical modulator at the transmitter, and secondly by the OEIC receiver. Recently an optical modulator SFDR of 68 dB was reported [4]. Assuming that the dynamic range of modulators improves further, the optical receivers will become significant in determining the overall dynamic range of wide-band analog photonic links. It is therefore important to work on improving the dynamic range of the receivers as well. There have been a number of papers in recent years focusing on improving the linearity of amplifiers by improving their OIP3 performance [5, 6, 13, 14, 19], however they are mostly power amplifiers intended for wireless and radio applications rather than low noise transimpedance amplifiers suitable for analog optoelectronic applications. On the other hand, recent works that focused on amplifier linearity in analog applications suitable for defense electronic systems such as radar and electronic warfare platforms, were based on HEMT technology [15, 16] which is not as compatible with OEIC devices such as PIN photodetectors as HBT technology in terms of fabrication simplicity. We have also seen some recent works which used various techniques to improve the linearity of HBT LNAs [17, 18]. However, they are not suitable for electronic warfare platforms due to their limited bandwidth performance. We have established in a previous work that distributed amplifier topology is significantly superior compared to other design topologies for HBT transimpedance amplifiers in terms of gain bandwidth product while retaining a comparable SFDR performance [7]. Hence we concluded that the DA topology will be the best option for HBT transimpedance amplifiers for OEIC analogue applications, if its SFDR can be further improved.

This work focuses on tradeoff options for the achievement of high SFDR in HBT transimpedance distributed amplifiers. We will introduce and analyze three different techniques to improve the SFDR of HBT transimpedance amplifiers at the expense of their transimpedance gain performance. These techniques are meant to provide designers with the flexibility to predict and improve SFDR by sacrificing the transimpedance gain, in applications where SDFR is the highest priority. Each of the techniques will be theoretically analyzed and then illustrated by a design example and the analytically predicted response will be compared with the results obtained by computer-aided circuit analysis.

2. REFERENCE DESIGN

As a starting point for each of our design examples, we will use an HBT transimpedance distributed amplifier designed using a methodology described and used by Cohen et al. [2], which is based on and improves a methodology proposed by Kobayashi et al. [8]. This methodology has been used by Kraus et al. [3] to design an HBT transimpedance amplifier with excellent performance as recently as 2007. Therefore this methodology for HBT transimpedance amplifier design can be regarded as the state of the art. The topology that Cohen uses for each gain stage or gain cell comprises an emitter follower at the input followed by a cascode, as shown in Figure 1. For the design, we chose to use InP/InGaAs HBTs in our transimpedance distributed amplifier, because of the ease of integration of HBT transimpedance amplifiers with PIN photodetectors [1]. The parameters of the HBT transistor model that we used in the amplifier were taken from [9], which reports experimentally verified large signal model parameters of an actual InP/InGaAs HBT. This amplifier design will be regarded as the reference design for the rest of the work. This reference design will be used as a starting point for the design examples of each of the techniques, and the performance of each of the techniques will be measured against the performance of this reference design. Following this reference design methodology, the optimal number of gain stages for the amplifier was calculated to be 4, and the amplifier

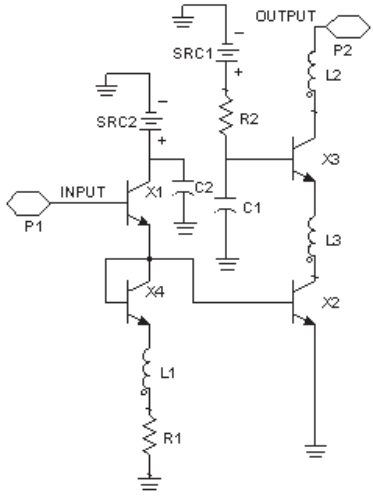

Figure 1. Schematic of a single gain stage of Cohen's design [2].

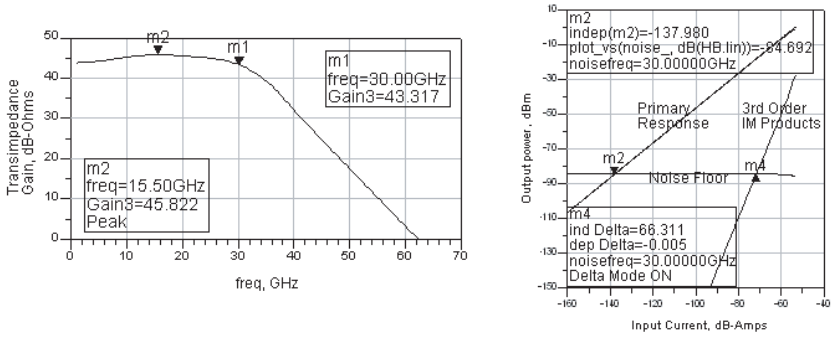

Figure 2. Transimpedance gain vs frequency characteristics and the large signal SFDR produced by the reference design (Cohen) at 30 GHz.

was then simulated to have a relatively flat transimpedance gain of about 43.3 dBΩ at up to 30 GHz and a large signal SFDR of about 66.3 dB, as shown in Figure 2. A noise bandwidth of 10 MHz has been used for this and all other SFDR simulations in this work.

3. TECHNIQUES WITH DESIGN EXAMPLES

3.1. Technique 1: Replacement of Emitter Follower Section

The emitter follower section preceding the cascode section in the gain stage shown in Figure 1 was originally proposed by Kobayashi et al. [8] and was intended to transform the capacitive impedance at the input of the cascode section to generate negative resistance at the input of the gain stage in order to achieve attenuation compensation on the input line. The objective was to improve the gain bandwidth product of the DA. However, as the emitter follower also performs current amplification, it has a detrimental effect on the linearity of the DA. In order to verify this, we performed a two-tone spectral analysis on each of the four gain stages of the standard amplifier. From this analysis, we learned that the emitter follower section attenuates the primary response, but it increases the third order products, thereby degrading the SFDR performance. As linearity and dynamic range are the priority in this work, we decided to remove the emitter follower section and introduce a parallel RC section in its place, as shown in Figure 3. The purpose of the capacitor in the parallel RC section is to reduce the input capacitance of the gain stage, while the resistor is used for biasing. It was verified through spectral analysis simulations that in this case, the input capacitor attenuates the primary response, but

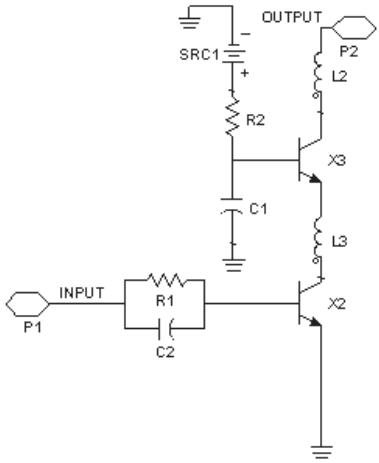

Figure 3. Schematic of a single gain stage of the altered design with the emitter follower section replaced by a parallel RC section.

does not generate additional third order products. Thus, the linearity and SFDR is improved with this replacement over that obtained with the emitter follower at the input of the gain stage, at the cost of a reduction in gain.

In order to make a fair comparison of performance with the reference design, the resistor in the parallel RC section was adjusted to retain the DC biasing in the cascode section, while the capacitor was adjusted to attain a flat input capacitance characteristic for the gain stage. We found that this resulted in the SFDR improving from 66.3 dB to 71.8 dB at 30 GHz which is a 5.5 dB improvement. The gain dropped from 43.3 dBΩ to 34.5 dBΩ, which is an 8.8 dB gain tradeoff, as shown in Table 1.

A comparison of the noise floor level of the amplifier with the emitter follower section (the reference design) and the amplifier with the parallel RC section was also made. It was found that the noise floor was about 5 dB lower with the parallel RC section. This drop is less than the 8.8 dB reduction in gain, so the introduction of the parallel RC section has degraded the amplifier noise figure. Nonetheless, an overall improvement in SFDR is still obtained.

Notably, although variations of this technique have been used by designers in past work in order to attain linearity [10], their details and performance have not been adequately researched to the best of the authors' knowledge. This work discusses it in detail and compares its performance with other techniques that are introduced in this work.

Table 1. SFDR and transimpedance gain comparison between the reference design and designs altered using the three techniques.

Simulation frequency	10 GHz		20 GHz		30 GHz	
	SFDR	Gain	SFDR	Gain	SFDR	Gain
Reference Design	68.0 dB	45.3 dBΩ	68.0 dB	45.6 dBΩ	66.3 dB	43.3 dBΩ
Technique 1 Design Example	68.8 dB	34.3 dBΩ	72.9 dB	34.3 dBΩ	71.8 dB	34.5 dBΩ
Technique 2 Design Example	68.8 dB	34.3 dBΩ	69.2 dB	35.2 dBΩ	70.3 dB	34.5 dBΩ
Technique 3 Design Example	69.1 dB	38.8 dBΩ	71.1 dB	36.9 dBΩ	71.8 dB	34.5 dBΩ

3.2. Technique 2: Adjustment of Amplifier Load

Most of the load power generated by a distributed amplifier is contributed by last few stages nearest the load, and almost half the total output power is generated by the stage nearest the load [11]. According to Equation (15) of [11], the output voltage across the kth gain stage of an n stage distributed amplifier is given by

$$V_{ds,k} = \frac{Z_\pi}{2} g_m V_{gs,1} e^{-j(k-1)\theta} \left\{ k + \frac{e^{-j2\theta} - e^{-j2(n-k+1)\theta}}{1 - e^{-j2\theta}} \right\} \quad (1)$$

where g_m is the transconductance of each gain stage, $V_{gs,1}$ is the input voltage of the first gain stage, i.e., the gain stage that is furthest from the load, Z_π is the image impedance of the Pi sections of the input and output transmission lines and θ is the electrical length between two adjacent gain stages, i.e., the propagation constant of each of the Pi sections of the input and output transmission lines. These terms are defined and explained in more detail in [11].

According to Equations (13) of [11], the current injected by the kth stage of the amplifier into the output line is given by

$$I_k = g_m V_{gs,1} e^{-j(k-1)\theta} \quad (2)$$

If we let $\omega \ll \omega_c$, then $Z_\pi \cong Z_0$ where Z_0 is the characteristic impedance of the output line and the load impedance of the amplifier. Therefore the load seen by the kth gain stage can be calculated as follows using the previous two equations.

$$Z_{L,k} = \frac{V_{ds,k}}{I_k} = \frac{Z_0}{2} \left\{ k + \frac{e^{-j2\theta} - e^{-j2(n-k+1)\theta}}{1 - e^{-j2\theta}} \right\} \quad (3)$$

Therefore the load seen by the last stage (i.e., with $k = n$),

$$Z_{L,n} = \frac{Z_0 n}{2} \tag{4}$$

Taking the effect of the output line capacitance, C_{ds} on $Z_{L,k}$ into account, we get,

$$Z_{L,n} = \frac{Z_0 n}{2 - j2\pi f C_{ds} Z_0 n} \tag{5}$$

Equation (5) shows that the load seen by the final stage is a function of the load of the amplifier, and therefore the load seen by the final stage can be adjusted to a certain degree by adjusting the load of the amplifier.

Running a load-pull analysis simulation on the last gain stage of the amplifier generates 3rd order IMD (intermodulation distortion) contours on the Smith chart, which allows us to predict the 3rd order IMD and therefore the linearity performance of the gain stage for any given $Z_{L,n}$ value. As almost half the output power is generated by the last stage over most of the frequency range [11], it can be assumed most of the nonlinearity is also generated by the last stage. Therefore the nonlinearity of the amplifier can be adjusted by varying $Z_{L,n}$, which can be done by tuning the load of the amplifier, Z_0 as (5) suggests. Thus the value of Z_0 can be adjusted or tuned to improve the dynamic range of the amplifier. However, changing Z_0 will also have an effect on the gain of the amplifier, and in most cases, changing Z_0 to improve the SFDR will have a negative effect on the transimpedance gain, which is the tradeoff.

Third order IMD contours generated by Agilent ADS software from load-pull simulation of a single gain stage of the reference design at 30 GHz and at an input power level of -25 dBm (which is an arbitrary input power level for which the 3rd order intermodulation is higher than the noise floor but lower than the 1 dB compression point) are shown in Figure 4. From (5), we can calculate that for a $50\,\Omega$ amplifier load (Z_0), the load seen by the final stage of the amplifier, i.e., the fourth stage of the amplifier, $Z_{L,4} = 30.70 + j46.12\Omega$. Changing the amplifier load from $50\,\Omega$ to $23.19\,\Omega$ and accordingly adjusting all elements of the distributed amplifier circuit (such as the output line inductance L_d, input line inductance L_g, the input line termination, Z_{0g}, etc.) results in the value of $Z_{L,4}$ to change from $30.70 + j46.12\,\Omega$ to $31.22 + j21.75\,\Omega$ according to (5). As we can see from Figure 4, this causes $Z_{L,4}$ to move to a location on the Smith chart where the 3rd order IMD of the final gain block is lower and therefore the linearity is better. Finally, the output of the amplifier is matched to a $50\,\Omega$ load using an impedance matching network. Thus we can use (5) and load

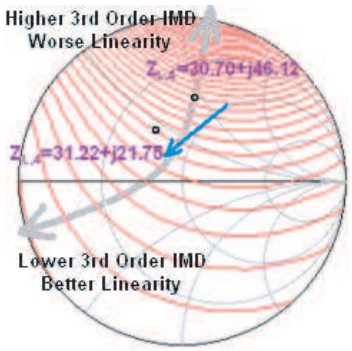

Figure 4. Third order IMD contours generated from load-pull simulation of a single gain stage of the reference design, at 30 GHz and at an input power level of −25 dBm. $Z_{L,4}$ values for $Z_0 = 50\,\Omega$ and $Z_0 = 23.19\,\Omega$ are shown. The contour step size is 1 dB.

pull analysis of the gain block to analytically predict that decreasing Z_0 will result in better linearity. Understandably, this procedure of using a lower Z_0 value will result in a lower transimpedance gain. Thus lower 3rd order IMD, i.e., better linearity and better SFDR, can be achieved by trading off transimpedance gain. The exact amount by which to reduce Z_0 will depend on the gain and SFDR requirements of the specific case and the discretion of the designer. However, reducing it too much will not only drastically reduce gain, but also make it difficult to match the output to $50\,\Omega$.

For our example, reducing Z_0 from $50\,\Omega$ to $23.19\,\Omega$ and then making necessary adjustments to the appropriate circuit elements as per the reference design methodology and using an impedance matching network to match the $23.19\,\Omega$ output to a $50\,\Omega$ load resulted in the SFDR to move up from 66.3 dB to 70.3 dB at 30 GHz, which is a 4 dB improvement. However, the gain dropped from 43.3 dBΩ to 34.5 dBΩ, which is an 8.8 dB gain tradeoff. Further details are provided in Table 1.

3.3. Technique 3: Adjustment of Cascode Base Capacitor

In an attempt to improve output power performance of HBT Distributed Amplifiers, Fraysse et al. in 2000 [12] added a capacitance C_a between the base of the common base HBT and ground, which allows the control of voltage across the input of the common base HBT by voltage division between C_a and C_{be} of the common base HBT. Therefore it also allows the control of the load that the common

emitter HBT sees to a certain degree. Running a load-pull simulation on the common emitter HBT allows us to see how the linearity of the HBT varies with varying the load that it sees, which can then be optimized as necessary via optimization of the capacitance that is the equivalent of C_a in our design, which is denoted as C1 in Figure 1.

Load-pull analysis simulation is performed on the common emitter HBT in our gain stage (denoted as X2 in Figure 1) at 30 GHz in order to generate 3rd order IMD contours as shown in Figure 5. These contours indicate the load preferences for X2 for low 3rd order intermodulation distortion and better linearity. In order to study how the load impedance of X2 varies as the capacitor C1 is varied, we swept the C1 value. We found that decreasing C1 causes the load impedance to move towards lower 3rd order IMD positions, as indicated by the contours. This indicates that in this case, using a lower capacitor value for C1 will result in lower 3rd order IMD, i.e., better linearity and higher SFDR. However, a lower C1 value will have a negative effect on the gain of the amplifier, because it will cause a higher reactance at the base of the common base HBT. Therefore the exact amount by which to reduce C1 will be a tradeoff between gain and SFDR.

For this example, reducing C1 from 10 pF to 0.25 pF in steps of -0.05 pF caused the load impedance of X2 to change from $15.96 + j33.45\,\Omega$ to $80.92 + j27.47\,\Omega$. Figure 5 shows the load impedances of X2 at various C1 values, and the arrow indicates the direction that the load moves as C1 is reduced. As can be observed from Figure 5, this caused the load impedance of X2 to move to a lower 3rd order

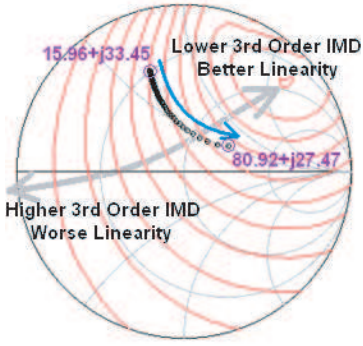

Figure 5. Third order IMD contours generated from load-pull simulation of the common emitter HBT transistor X2 (in Figure 1). Load impedances of X2 for C1 values ranging from 10 pF to 0.25 pF in steps of -0.05 pF are shown. The contour step size is 1 dB.

IMD position, which resulted in a 5.5 dB SFDR improvement (from 66.3 dB to 71.8 dB). However, the gain dropped from 43.3 dBΩ to 34.5 dBΩ. Further details including improvements at other frequencies are provided in Table 1.

4. RESULTS AND OBSERVATIONS

Table 1 shows comparisons between the reference design and design examples of each of the techniques in terms of their gain and SFDR performances. In our design examples for each of the three techniques, an equal amount of gain was traded off (from 43.3 dBΩ to 34.5 dBΩ) at 30 GHz from the reference design on purpose, so that a fair comparison can be made between the three techniques in terms of SFDR improvement.

As can be observed from Table 1, Technique 2 produced the least SFDR improvement among the three. Techniques 1 and 3 on the other hand have performed similarly in terms of SFDR improvement. However each of these two techniques has its drawback. As Technique 1 is basically the replacement of the emitter follower section with a parallel R-C network followed by appropriate adjustments, this technique is not at all tunable in terms of tradeoff, and therefore significantly lacks flexibility. On the other hand, Technique 3, although fully tunable via the capacitor, compromises the flat response of the output capacitance of the gain block. As a result, if the capacitance is tuned too much, maintaining a flat gain response becomes difficult for the designer. Therefore the usage of Technique 3 is only advisable when a relatively smaller gain tradeoff is desired. When a relatively larger SFDR improvement is desired and a larger gain sacrifice is afforded, Technique 1 can be combined with either Technique 2 or Technique 3. For demonstration of this, we applied Techniques 2 and 3 individually on our design example for Technique 1 in order to further improve the SFDR, while trading off more gain. Once again, for fair performance comparison between the two combinations, the gain was traded off equally (from 34.5 dBΩ to 30.0 dBΩ) in both cases. As can be observed from Table 2, the combination of Techniques 1 and 3 performs significantly better than the combination of Techniques 1 and 2 in terms of SFDR improvement. Hence we conclude that usage of a combination of Techniques 1 and 3 is advisable when a relatively larger SFDR is desired. In our design example, this combination resulted in a nett SFDR improvement of 9 dB with a nett 13.34 dBΩ gain tradeoff. Notably although Technique 2 has the worst SFDR performance, it does not have the drawbacks of the other techniques, as it is both tunable and retains a flat gain response for the amplifier.

Table 2. SFDR transimpedance gain comparison between different combinations of techniques.

Simulation frequency	10 GHz		20 GHz		30 GHz	
	SFDR	Gain	SFDR	Gain	SFDR	Gain
Technique 1 Design Example	68.8 dB	34.3 dBΩ	72.9 dB	34.3 dBΩ	71.8 dB	34.5 dBΩ
Techniques 1 and 2 combined	72.4 dB	30.3 dBΩ	73.2 dB	29.6 dBΩ	73.1 dB	30.0 dBΩ
Techniques 1 and 3 combined	73.9 dB	32.2 dBΩ	75.4 dB	30.7 dBΩ	75.3 dB	30.0 dBΩ

Notably, these techniques have not been experimentally validated. This was due to technical limitations of facilities available to the authors. However, we are confident of the validity of these methods as they have been theoretically predicted and reasoned, and then backed up through simulations which fully agree with conclusions reached through theoretical analysis. Moreover, we have used the experimentally validated large signal model of a real transistor [9] rather than an ideal transistor for all our simulations which adds further validity to our predictions and simulations. It should also be noted that we have compared the techniques using the same transistor model in all simulations in order to ensure that the comparisons were fair.

5. CONCLUSION

Three different methods of trading off transimpedance gain in order to improve the SFDR of HBT transimpedance distributed amplifiers were introduced, discussed and demonstrated. Their performances were compared and the pros and cons of each method were presented. Performances of combinations of these methods were also compared and discussed. It was found that the Cascode Base Capacitor Adjustment Technique (Technique 3) offers the best tradeoff option in terms of SFDR performance when a relatively small gain tradeoff is desired, while a combination of the Emitter Follower Replacement Technique (Technique 1) and the Cascode Base Capacitor Adjustment Technique (Technique 3) is the best option when a relatively large SFDR improvement is desired. It was also found that the Amplifier Load Adjustment Technique (Technique 2) or a combination of Techniques 1 and 2 is the suitable tradeoff option when a flat gain response is desired.

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