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A FLEXIBLE INTEGRATED PHOTONIC TRUE TIME DELAY PHASER FOR PHASED ARRAY ANTENNAS

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Abstract—An integrated photonic True Time Delay phaser for phased array, based on an innovative technology, is here presented. The module versatility is showed by presenting more driving strategies matching different antenna features. The phaser insertion loss, the fluctuations of the excitation coefficients corresponding to the various driving configurations and the statistical modeling of the realization defects are also discussed.

1. INTRODUCTION

Photonics represents a key technology for present and future developments of high performance antennas for civil and military applications, giving a possible solution to the limitations showed by conventional steering control systems when applied to modern phased-arrays [1–4]. Indeed, the optical technology allows a reduction of both weight and size of the Beam-Forming Network (BFN) and guarantees high interference immunity. Moreover, optical BFNs permit variable and electronically controlled delay lines and the efficient implementation of the True Time Delay (TTD) concept. Accordingly, wide-band beam-squint-free phased arrays can be realized, as Optical Time-Steered Antennas (OTSA) [2–4]. Some of the most recent examples of OTSAs are presented in [5–12].

To implement an optical time shifter, and get the TTD control, two main approaches can be pursued: the first uses Switched Delay Lines (SDL), while the second employs Variable Propagation Velocity Lines (VPVL).

A SDL network exploits optical or electrical switches to select the delay-line realizing the desired time delay [2, 7, 13, 14]. A classical SDL

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is the Binary Fiber Optic Delay Line (BiFODeL), exploiting optical switches and fiber segments with lengths progressively increasing by a power of 2 [4]. Such a structure requires, for large arrays, a large number of optical components. To save optical hardware, free space delay lines can be employed, as that proposed in [15] and based on an acousto-optic deflector.

In VPVL systems time delays are controlled by varying the propagation velocity of the optical signal [16]. This approach allows realizing a continuous beam-steering. It can be implemented by using tunable lasers together with high dispersion fibers [5, 8, 17], or chirped fiber Bragg gratings [6, 10, 18]. These architectures are able to feed the entire antenna guarantying, if compared to SDL solutions, a drastic reduction of the hardware complexity. However, they suffer from some drawbacks. For large arrays, high dispersion fiber beam-formers require very long fibers to cover large scanning sectors, and a temperature control system to avoid instabilities. Furthermore, when Bragg grating delay units are involved, the trade-off between grating reflectivity and bandwidth has to be properly managed.

Obviously, the time steering control system can be employed to feed each element of the array, thus ensuring an ultra-wide-band control. However, as long as saving hardware is required, also time-steering techniques based on sub-array partitions can be considered, applying the time control only at the sub-arrays stage, while using the more standard phase-steering at the radiating element level. Obviously, this second possibility represents a compromise between wide-band and costs specifications [19].

The aim of this paper is to present a new photonic integrated TTD Phaser (TPH) [20], whose core is a TTD Unit (TTDU) exploiting an innovative technology based on the cross-connect switch described in [21]. We discuss how the TTDU can be programmed to achieve two different TPH configurations. Both the array and sub-array architectures above are considered.

In particular, in the Section 2, the features of the TTDU, are described: a 32×32 switches TTDU has been considered, able to drive up to 4 elements/sub-arrays. Section 3 is devoted to issues related to the TPH design. In Section 4, the TTDU driving strategies, related to two different TPH configurations of practical interest, are discussed. The TPH has been designed to realize four 4 bits time shifters, allowing to drive a 4 element OTSA prototype, or four 5 bits time shifters driving a four sub-arrays antenna. Then, in Section 5, we discuss the system beam capabilities and the main design issues as the Insertion Loss (IL), the Amplitude Uniformity of the excitation coefficients (AU) and, by accounting for the statistical modeling of the TPH components,

the effects due to realization defects. Finally, in Section 6, a comparison with photonic TTD systems available in the open literature is provided. Conclusions are drawn in Section 7.

As final remark, it is worth noting that, thanks to the modularity of the TTDU, TPHs bigger than those described in this paper can be straightforwardly obtained by integrating several chips, thus allowing larger antennas and/or more accurate beam pointing capabilities.

2. TTDU FEATURES DESCRIPTION

The TTDU essentially realizes a SDL matrix. Its layout is represented in Fig. 1. The chip we consider here is composed of $N \times M$ integrated optical waveguides intersecting each other at cross points denoted by black dots in Fig. 1 [21]. We will indicate with the index r and s the generic input and output ports of the unit, respectively (see Fig. 1). The optical signal, entering the r input waveguide can be switched towards the output waveguide s by means of a driving circuit activating the proper cross point (Fig. 1). Obviously, according to the selected cross point (r, s), the length of the light signal path, and the related delay, can be changed. On the other hand, if no cross points are activated, the light entering the r-th input waveguide passes through the TTDU and arrives on the r-th "drop" port (see Fig. 1). Thanks to the presence of the "drop" and "add" ports, modular structures can be realized by arranging more basic units, so that bigger matrixes can be obtained. Moreover, also a bidirectional use of the TTDU becomes possible [20].

As long as the TTDU is treated as a black box, it can be described by means of input-output relationships expressing both delays and insertion losses.

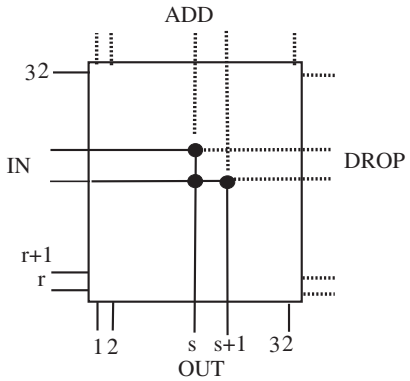

Figure 1. The TTDU layout.

Concerning delays, the time delay associated to the input-output pair (r, s), say $\tau(r, s)$, is given by:

$$\tau(r,s) = \tau_{ref} + (r-1)\tau_\Delta + (s-1)\tau_\Delta \tag{1}$$

where τ_{ref} (irrelevant, and then assumed equal to zero later on) is a reference delay accounting for the connecting fibers delays and the chip input and output path delay, and τ_Δ is the elementary delay associated to path between two adjacent cross points.

Concerning insertion losses, the TTDU loss associated to the input-output pair (r, s), say $L(r, s)$, is given by:

$$L(r,s) = 2C + R + (r-1)T + (s-1)T \tag{2}$$

where $2C$ is the loss term associated to the path between the input and output connecting fibers and the first chip cross point, T is the loss term due to the propagation between two consecutive cross points, and R is the loss term related to the deflection mechanism at a cross point. In the following, we will always refer to a 32×32 switches TTDU.

3. THE OTSA PROTOTYPE DESIGN

As discussed in the Introduction, an OTSA can implement an ultra wide-band beam-squint-free antenna. In such antennas, the TPH has to provide a linear phase slope of the array excitation coefficients proportional to the microwave working frequency.

In particular, given a linear array of N radiating elements/sub-array, with uniform spacing d, and the beam pointing angle θ as the angle between the beam pointing direction and the normal to the array, to attain the beam pointing in a direction θ, the n-th element $(n = 1, \ldots, N)$ has to be fed with a signal subjected to a delay τ_n given by:

$$|\tau_n| = \frac{(n-1)d}{c} \sin|\theta| \tag{3}$$

where c is the speed of light in the vacuum.

To get a given maximum beam-pointing angle $\theta_{\max}$, the TPH has to provide a maximum time delay $\tau_{\max}$ proportional to the array length $L = (N-1)d$ and to $\sin(\theta_{\max})$. Accordingly, the maximum time delay $\tau_{\max}$ becomes a key design parameter. On the other hand, given TPH with a maximum delay $\tau_{\max}$, it allows an efficient beam-steering of an array antenna once L and $\theta_{\max}$ are properly assigned.

The OTSA design involves three different main aspects:

-Discrete Beam-Steering

In most of applications discrete beam-steering is considered, i.e., the delay distributions of interest are assumed to belong to a discrete

set, and achievable by means of digital Time Shifters (TS) allowing a finite number, say M, of bits. In other words, each TS realizes a set of $2^M - 1$ delays, multiples of an elementary one (MBIT mode). Obviously, digital TSs are affected by quantization errors that degrade the pattern performance, with possible detrimental effects on the Side Lobe Level (SLL), the beam pointing accuracy and the beam-width. It is worth noting that also the value of $\tau_{\max}$ affects the pattern degradation. In fact, for an M bits TS, the nominal delays distribution is approximated by means of 2^M states, with a time step equal to $\tau_{\text{step}} = \tau_{\max}/(2^M - 1)$. Accordingly, the maximum phase error φ_{err} can be assumed uniformly distributed across τ_{step}, and is given by [22]:

$$|\varphi_{err}| = \left|\frac{\omega\tau_{\text{step}}}{\sqrt{32}}\right| = \left|\frac{\pi f \tau_{\max}}{\sqrt{3}\,(2^M - 1)}\right| \tag{4}$$

where f is the Microwave (Mw) operating frequency. Unlike digital phase shifters, where the phase quantization error depends only on the number of bits, the phase error φ_{err} grows with the array size, and with $\tau_{\max}$ [19]. In particular, longer $\tau_{\max}$ values are desirable since they allow larger arrays, for a given $\theta_{\max}$, or larger $\theta_{\max}$, for a given array size. However, as long as $\tau_{\max}$ grows, the quantization error raises and M must be increased to keep the performance at the desired level.

According to the above remarks, a flexible and programmable TPH becomes really useful to face different requirements needed in different applications/working configurations.

-Sub-array Structure

As mentioned before, to save hardware, the time-steering control can be applied at the sub-arrays level. However, when dealing with wideband sub-array structures other pattern deterioration sources have to be taken explicitly into account. In particular, the sub-array pattern has to be designed to compensate for Grating Lobes (GL) possible in the array pattern. Obviously, when varying the operative frequency, due to the sub-array pattern squint, the compensation could become inadequate to correctly cancel the undesired GL [19]. To overcome this problem overlapped distribution network, or multi-beam wideband feed networks have been proposed [19].

-Practical Issues

Matthews identifies the principal practical issues of an OTSA in [23]: random amplitude and phase errors due to BFN asymmetries and drifts, periodic amplitude and phase errors due to the quantized amplitude and phase control and/or to the sub-array architecture, the beam-forming/steering speed, the BFN size, weight, robustness,

costs and reliability, the efficient use of the optical power and the environmental issues.

Here we want to show how the TTDU flexibility allows realizing different OTSA configurations, by taking into account for the mentioned issues. In particular, first we will consider two TTDU different driving strategies allowing to control the maximum delay $\tau_{\max}$ and the time quantization level, and to drive antennas with different size and beam pointing resolutions. Then, the TPH insertion loss and AU for the different configurations will be discussed.

Once the TPH delay properties have been given, the design of the radiating system is considered and the system capabilities derived, by discussing the issues related to the GL and the Electromagnetic Coupling (EmC). Finally, the effects of random amplitude and phase errors, due to realization defects of each component in the TPH, is addressed.

4. THE TPH DESIGN

Before discussing the TTDU driving strategies, reported in Sections 4.2 and 4.3, the TPH architecture, attempting to save optical power, to reduce size and costs, has to be defined (Section 4.1). To this end let us note that the TPH has to drive a whole array antenna, eventually subdivided into sub-arrays.

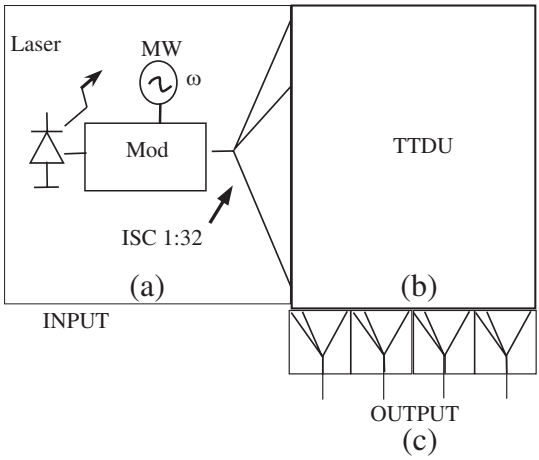

Figure 2. The TPH layout.

4.1. TPH Architecture

The TPH is, generally, made of three sections (Fig. 2):

- Section a), namely the generation and modulation stage,
- Section b), namely the optical BFN,
- Section c), namely the conversion stage.

Stage a) is made of one or more optical sources and modulating systems, fed by the modulating Mw signal. Stage b) provides the proper delay distribution to the modulated light signals generated at stage a). Once experienced the desired time delay, the different light signals are down-converted in the Stage c), and so can be exploited to feed the array radiating elements.

The BFN (stage b)), the TTDU in our case, is the TPH core. It can realize more than just one TS. According to Eq. (1) each TS must be associated to a proper set of input-output pairs, and each TS can be programmed to provide the delays related to the desired beam-pointing directions. However, we have also to take into account for the TTDU insertion loss in Eq. (2). In other words, the driving strategy must be devised by accounting also for the AU control. On the other hand, since, for a given driving configuration, only some input and output TTDU ports are used, the choice of the driving strategy will affect the characteristics of both stages a) and c).

Regarding stage a), we will adopt the most compact and cheap set-up: the optical signals needed to correctly feed all the "active" TTDU input ports (according to the considered strategy) are obtained by using a single laser, a single high speed modulator, and an Integrated Star Coupler (ISC). In Fig. 2, as an example, a $1 : 32$ ISC is depicted, feeding all the 32 TTDU inputs.

Regarding stage c), the TTDU outputs corresponding to each TS are combined together, through a power combiner, and connected to a single photodetector (in Fig. 2 four combiners are depicted, corresponding to four detectors). This choice reduces both complexity and costs of the conversion stage, even if the power loss increases due to the combiner insertion losses. As discussed in [20], the outputs assigned to each TS can be contiguous or non contiguous. In the first case, ISCs can be used allowing a fully integrated TPH structure, compact and reliable. On the contrary, the non-contiguous outputs configuration, while requiring nonintegrated couplers, allows better time delay performance, since the input-output pairs locations to be combined are not subjected to constraints [20]. Accordingly, our attention is focused on this latter output configuration.

Finally, let us observe that, when the TTDU is used to feed an entire array antenna, as in all the cases here reported, the TTDU,

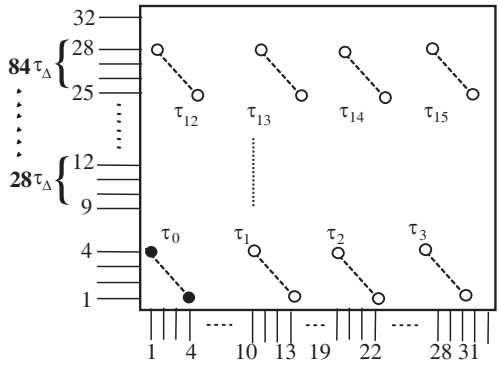

Figure 3. Working scheme in the 4 bits mode.

together with the star couplers, behaves essentially as a "multiplexer", combining all the TTDU inputs associated to a single radiating element into the corresponding output port.

The TTDU parameters exploited later on are those typical and equal to $\tau_\Delta = 1.5\,\text{ps}$, $C = 0.25\,\text{dB}$, $T = 0.07\,\text{dB}$, $R = 2.1\,\text{dB}$ [21, 24, 25].

4.2. Case A: 4 Bits Mode

The TPH has to realize four 4 bits TSs. Each TS has to realize 16 delays $\tau_n = n\Delta t$, with $\Delta t = \tau_{\max}/15$ and $n = 0, \ldots, 15$. In particular, by adopting a proper TTDU driving strategy, Δt and $\tau_{\max}$ can be varied while realizing the same number of delays for each TS. In this way the TTDU can be used to drive different aperture antennas. In particular, the driving strategy allows to vary Δt from $4\tau_\Delta = 6\,\text{ps}$ to $9\tau_\Delta = 13.5\,\text{ps}$ with a step of $1.5\,\text{ps}$ so that $\tau_{\max}$ can be varied from $90\,\text{ps}$ to $202.5\,\text{ps}$, with a step of $22.5\,\text{ps}$.

The TTDU provides each delay τ_n by activating the cross point related to the input-output pairs (r, s) and specified according to Eq. (1). In particular, since the TTDU implements four TSs, for each delay τ_n four input-output pairs realizing the same delay should be individuated. According to Eq. (1) these pairs should respect the relation:

$$r + s = c_n \tag{5}$$

where c_n is a constant value, properly chosen according to the delay to be realized.

Let us denote with $\lfloor x \rfloor$ the function that rounds x to the nearest integer towards zero and consider separately the two limit cases, i.e., $\tau_{\max} = 202.5\,\text{ps}$ and $\tau_{\max} = 90\,\text{ps}$. To attain the $\tau_{\max} = 202.5\,\text{ps}$, the

input-output pairs needed to realize the n-th delay for the α-th TS, are (see Fig. 3):

$$\begin{cases} r_{\alpha,n} = 4 - (\alpha - 1) + 8\lfloor n/4 \rfloor \\ s_{\alpha,n} = 1 + 9(n - 4\lfloor n/4 \rfloor) + (\alpha - 1) \end{cases} \tag{6}$$

The correct total delay is obtained by using three external delays equal to $28\tau_\Delta$, $56\tau_\Delta$ and $84\tau_\Delta$ connected at the inputs from 9 to 12, 17 to 20 and 25 to 28, respectively. Accordingly, Eq. (5) can be easily verified: f.i. for the delay τ_0 we have $r_{\alpha,0} + s_{\alpha,0} = c_0 = 5$, thus selecting the input-output pairs (4, 1), (3, 2), (2, 3), (1, 4) for the 1st,2nd, the 3rd and the 4th TS, respectively (the full dots in Fig. 3).

Once the driving strategy (for $\tau_{\max} = 202.5\,\text{ps}$) has been defined, we can focus our attention on the following parameters: the TPH insertion loss, namely IL_T, the AU and the phase quantization error φ_{err}.

Regarding the IL_T, some observations are in order. Firstly, let us observe that this configuration requires a 1 : 16 ISC in the stage a), and four 4 : 1 coupler to combine the outputs corresponding to each TS. And so the cumulative IL is given by the input and output couplers contribute (about equal to 18 dB), and by the TTDU loss, that varies with the working configuration, thus generating the mentioned unwanted asymmetries. According to Eq. (2) the minimum TTDU loss, in this configuration, is about 3 dB. In this way, apart from the conversion losses and star coupler excess losses, the whole loss is, at least, equal to 21 dB. However, it is worth noting that this value takes into account also for the power division losses needed to feed the 4 radiating elements. As consequence, the IL_T is about 6 dB lower than the previous value, i.e., $\text{IL}_T = 15\,\text{dB}$.

Regarding the AU, since the stage a) and c) are symmetric for each TS, it will depend only on the losses due to the light propagation within the chip associated to the considered input-output pairs. In particular it is given by $L\,(32,\,25)$-$L\,(4,\,1)$. According to Eq. (2) the AU is about 3.5 dB. Finally, according to Eq. (4), the phase quantization error due to time quantization is, at 15 GHz, about $|\varphi_{err}| = 0.37\,\text{rad}$.

A similar discussion is possible for the case $\Delta t = 4\tau_\Delta = 6\,\text{ps}$ and $\tau_{\max} = 90\,\text{ps}$, corresponding to the minimum value for max attainable with this strategy. In this case the input-output pair needed to realize the n-th delay for the α-th TS, is $r_{\alpha\cdot n} = 4 - (\alpha - 1) + 24\lfloor n/8 \rfloor$, $s_{\alpha\cdot n} = 1 + 4(n - 8\lfloor n/8 \rfloor) + (\alpha - 1)$, and the inputs from 25 to 28 require an external delay equal to τ_Δ.

The design parameters related to the 4-bits mode, namely the number B of bits, the $\tau_{\max}$, IL_T, AU and $|\varphi_{err}|$, are reported in Table 1, by only considering the maximum and minimum delay ranges.

4.3. Case B: 5 Bits Mode

The TPH has to realize four 5 bits TSs. Each TS realizes 32 delays $\tau_n = n\Delta t$, with $\Delta t = \tau_{\max}/31$ and $n = 0, \ldots, 31$. Also in this case external delays are employed. The 32 input-output pairs related to each TS are obtained by using 8 input gates and 4 output gates. As for the previous case $\tau_{\max}$ can be varied. In particular, $\tau_{\max}$ can be changed from 186 ps up to 418.5 ps with a step equal to 46.5 ps. Here we refer to the case $\tau_{\max} = 418.5$ ps. The α-th TS can realize the n-th delay by using the input-output pair defined by (see Fig. 4):

$$\begin{cases} r_{\alpha,n} = 4 - (\alpha - 1) + 4\lfloor n/4 \rfloor \\ s_{\alpha,n} = 1 + 9(n - 4\lfloor n/4 \rfloor) + (\alpha - 1) \end{cases} \tag{7}$$

Moreover, to ensure the correct delay, each exploited input gate r has to be fed by means of an external delay τ_{ext} according to $\tau_{ext} = 32\lfloor (r-1)/4 \rfloor \tau_\Delta$ (Fig. 4). In this way only seven external delay are used, each feeding a 4 input gates group: the input from 5 to 8 are fed by means of a $32\tau_\Delta$ external delay, the input from 9 to 12 are fed by a $64\tau_\Delta$ external delay, and so on, while no one delay should be used for the first four inputs.

Concerning the use of the external delay lines, an observation is in order. Generally speaking, the TTDU could be used as a simple

Table 1. Design parameters related to the 4 bits mode.

	B	$\boldsymbol{\tau_{\max}}$	$\mathbf{IL}_{\boldsymbol{T}}$	**AU**	$\lvert\phi_{\mathbf{err}}\rvert$ **(15 GHz)**
max range	4	202.5 ps	15 dB	3.5 dB	0.37 rad
min range	4	90 ps	15 dB	3.5 dB	0.16 rad

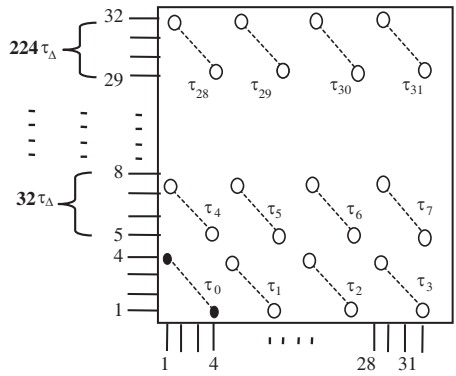

Figure 4. Working scheme in the 5 bits mode.

Table 2. Design parameters related to the 5 bits mode

	B	$\tau_{\max}$	IL_T	AU	$\lvert\phi_{err}\rvert$ (15 GHz)
max range	5	418.5 ps	18 dB	3.5 dB	0.37 rad
min range	5	186 ps	18 dB	3.5 dB	0.16 rad

switch to select a set of external delay lines as in BiFODeL systems. On the contrary, our aim is to realize the delay lines within the TTDU, and employ the minimum possible number of external delay lines so that the insertion loss and the delay distribution performances are improved.

This configuration requires a $1:32$ ISC in the stage a), and four $4:1$ output combiners. The corresponding IL_T is about 18 dB. The AU is about 3.5 dB, while $|\varphi_{err}| = 0.37$ rad at 15 GHz. The design parameters related to the maximum and minimum $\tau_{\max}$ configurations are reported in Table 2.

5. SYSTEM BEAM CAPABILITIES AND DESIGN CRITERIA

Once the TPH configurations and delay distributions have been defined, the system performances can be estimated.

In particular, we are interested in the maximum beam pointing angle $\theta_{\max}$, for a given array dimension. To easily solve the problem, we introduce a planning chart suited for both array and sub-array architectures (see Fig. 5). The planning chart represents graphically Eq. (3), parameterized as function of the Mw frequency and the element spacing d. Once the design frequency and element distance have been set, the chart allows to determinate $\theta_{\max}$, given $\tau_{\max}$. In the case depicted in Fig. 5, we refer to the 4 bits configuration, with $\tau_{\max} = 90$ ps, driving four elements. The value achievable for $\tau_{\max}$ with the TTDU in the 4 bits configuration is reported as continuous line. The planning chart shows that, for $d = 0.5\lambda$, the 4 bits mode allows a $\theta_{\max}$ equal to 37°, 64° and 90° for 10 GHz, 15 GHz and 20 GHz respectively. Obviously, the chart can be straightforwardly scaled as long as key parameters related to other configurations become of interest. In particular, regarding the 4 bits configuration realizing a $\tau_{\max}$ equal to 202.5 ps, a wide scanning range $\theta_{\max}$ equal to about 60° [19], for $d = 0.5\lambda$, can be achieved by using a design frequency equal to 7 GHz. On the contrary, the 5 bits mode can be exploited to provide the time control at sub-array level, since, in this configuration,

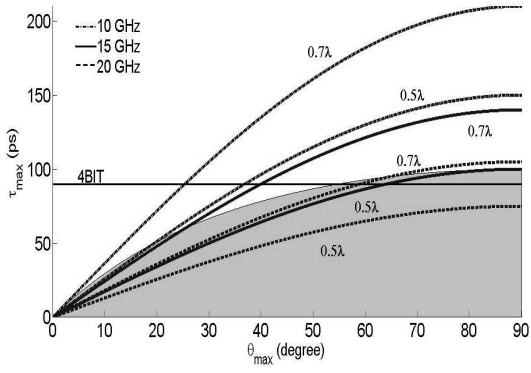

Figure 5. Planning chart.

the TTDU can drive a 28 elements antenna made of 4 sub-arrays of 7 elements spaced by a half a wavelength, for $f_D = 22\,\text{GHz}$, and ensure a $\theta_{\max}$ equal to 60°.

To complete the performance evaluation, the choice of d has to be discussed. It depends on the trade-off between the GL phenomenon and the EmC.

Regarding GLs, the compensation issue related to the sub-array structures has been already discussed. Here, let us consider the array structures. In this case it is possible to consider the values of d avoiding GLs. By identifying this set on the planning chart, we can obtain the GL free design zone. With reference to the 4 bits configuration ($\tau_{\max} = 90\,\text{ps}$), we can use the upper limit $d_0(\theta_{\max}) = 1/(\sin(\theta_{\max})+1)$ in Eq. (3), thus obtaining the curve $\tau_{\max}(\theta_{\max})$ delimiting, in the planning chart, the GL free zone. This zone, for a frequency equal to 15 GHz, is represented as a shadowed region (see Fig. 5). This additional feature in the planning chart allows an easy evaluation of both the values of $\theta_{\max}$ and d realizing a GLs-free pattern, once $\tau_{\max}$ is known.

As far as EmC is concerned, depending on the value of d, it can seriously deteriorate the electrical behavior of the radiating elements leading to a significant mismatch and thus, to bad working conditions for photodetectors and TSs. Moreover, mismatch varies with the beam pointing angle. To solve this problem and reduce mismatching effects, isolators must be introduced between photodetectors and radiating elements.

Finally, some practical issues should be taken into account in the design process. Indeed, systematic and/or random errors can affect the

nominal array excitation distribution. The systematic errors are due, in our case, to the TTDU non uniformities, and will concern the control of the amplitude distribution, while the random errors are related to the realization defects of each device exploited in the TPH structure. In both cases, a proper set of trimming stages should be introduced, within the TPH structure, to compensate for the errors effects. To this end, it is useful to have at disposal an effective and realistic model of the OTSA prototype, wherein both systematic and random errors are considered, thus making possible the evaluation of the errors effects, and the optimization of the trimming network configuration.

Regarding the systematic errors, since these involve the control of the amplitude distribution, a preliminary observation is in order. Generally speaking, apart from the systematic errors, the control of the amplitude of the excitations of the radiating elements, although requiring additional hardware, can guarantee a significant improvement to the radiated pattern. In particular, the control of the amplitude distribution by means of an advanced array synthesis technique [26] allows to take into account the coupling effects and to get low SLLs. However, in the case of our interest, the additional hardware should be employed not only to realize the required nominal amplitude distribution, but also to compensate for the undesired TTDU asymmetries. Since the TTDU insertion loss variations change with both the beam pointing angle and the stages configuration of the TPH structure, the values for the compensations must be carefully chosen [20].

Regarding the random errors, these are due to the realization defects of each TPH device: indeed, any component can suffer from undesired attenuations or spurious time delays that change amplitudes and phase/time delays of antenna excitations. Accordingly, the realization defects of each TPH component must be adequately modeled. In particular, let us refer to the effects of the realization defects on the amplitude of the excitation coefficients. A similar approach can be adopted for the phase. According to the procedure exploited for the fiber-optic links, two different analysis can be used: the worst case analysis and the statistical one [27, 28]. In the worst case procedure, the maximum variation in excitation coefficients, due to the TPH components realization defects, is obtained starting from the knowledge of the maximum and the minimum insertion loss variations reported for each components. The statistical analysis, on the other side, is obviously based on the statistical models of the insertion loss of each exploited device. A Gaussian distribution efficiently describes the insertion loss for star coupler and power combiner [27, 28], while a truncated Gaussian [27] or a Log-Normal [29] distribution can be used

for the connectors.

Based on these considerations, and exploiting a CAD tool, the model of the TPH has been implemented, by using a Gaussian distribution for the insertion loss of the star couplers, power combiner and for the TTDU losses, and a truncated Gaussian distribution for the connectors. As expected, the resulting insertion loss associated to the α-th radiating element can be described by means of a Gaussian distribution with mean $\mu_\alpha = \sum \mu_i$, μ_i being the mean loss of the i-th device associated to the α-th radiating element, and with standard deviation $\sigma_\alpha = (\sum \sigma_i^2)^{0.5}$, where σ_i represents the standard deviation of the i-th component. Accordingly, the insertion loss variation of the α-th element, due to the realization defects, is contained in the interval $[\mu_\alpha - 3\sigma_\alpha, \mu_\alpha + 3\sigma_\alpha]$, with a confidence level $> 99\%$. This information can be fruitfully exploited to identify the maximum allowable excitation coefficient errors, i.e., the ones corresponding to the maximum tolerable pattern errors. To get this goal, a statistical analysis [30, 31] can be used as a guide line to carry out a numerical analysis for our 4 elements antenna [32]. F.i., by considering a Tchebitchev distribution, with a 15 dB SLL, to guarantee an error pattern with a SLL lower than 10 dB and a beam pointing angle error less than few degree, the maximum acceptable error bounds for amplitude and phase must be respectively lower than 12% and 7°.

Accordingly, the design of the trimming stages has to be carried out in order to reduce the errors on the excitation coefficient distribution under the acceptable bound. Regarding the systematic errors it is possible to design the trimming network in order to reduce the errors effects on the antenna pattern, since a priori information are available. On the contrary, regarding the random errors due to the realization defects, these cannot be taken into account during the design step. The errors have to be evaluated once the prototype has been realized. Then, the trimming procedure can be performed.

6. COMPARISON WITH OTHER SOLUTIONS

Let us spend some words to highlight the peculiar aspects of the solution herein proposed when compared to those in the open literature.

It is worth noting that the TTDU herein presented behaves as a particular SDL architecture, called Parallel Delay Line (PaDeL) [2, 14, 20]. Accordingly we will compare our TTDU to PaDeL architectures, since the differences among the main SDL schemes have been already widely discussed [33].

To carry out an exhaustive comparison the following issues should

be taken into account:

1) hardware complexity;
2) costs and compactness;
3) time delay performance;
4) insertion loss, and amplitude uniformity.

-Hardware Complexity

As a first remark, we would like to stress that our TTDU exploits just one laser, unlike solutions in [2, 14] where 2^B lasers are employed, B being the number of bits considered.

To further quantify the hardware complexity a figure of merit must be considered, even if, when dealing with integrated SDL, a correct evaluation of the hardware complexity is, in our opinion, a hard task, since it should take into account also for technological aspects related of the peculiar implementation.

Leaving this out of consideration, we use the figure of merit proposed in [33] for the main SDL architectures: it is based on the number of lasers, fibers and switches employed for each TS. Accordingly, for a B bits TS, the figure of merit related to the PaDeL scheme [2, 14] is $C_{PaDeL} = 2^{B+1}$, since 2^B lasers and 2^B fibers are employed [33]. The hardware complexity figure of merit for the proposed scheme, C_{TPH}, can be evaluated similarly to the PaDeL case as the sum of the four following terms: the number of lasers, equal to 1, the number of external delay lines, the number of realized switches, equal to 2^B, and the number of exploited waveguides, equal to $0.5\,(N_{\mathrm{IN}}+N_{\mathrm{OUT}})$, N_{IN} and N_{OUT} being the number of TTDU inputs and outputs exploited, respectively.

When dealing with a 4 bits unit we have $C_{\mathrm{PaDeL}} = 32$, while $C_{\mathrm{TPH}} = 24$, since three external delay line are used and only 4 inputs and 4 outputs are employed (we are referring to the case with the longest $\tau_{\max}$). For a 5 bits TS we have $C_{\mathrm{PaDeL}} = 64$, $C_{\mathrm{TPH}} = 46$. Accordingly, the proposed structure requires a hardware complexity lower than the one of a canonical PaDeL structure.

-Costs and Compactness

The costs of the TPH depend on the costs to realize each unit and on the hardware complexity of the whole BFN. To this end the TTDU driving strategy has been studied to get more TSs within a single chip, thus reducing the hardware figure of merit and, consequently, the overall BFN costs.

Concerning the compactness, the driving strategies have been designed to realize the desired delays within the integrated TTDU, with the minimum number of external fibers. Moreover, thanks to the

TTDU modularity, more elementary chips can be joined together to get bigger TTDUs to drive larger antennas, with good compactness.

-*Time Delay Performance*

It is worth noting that, in some driving configurations, the TTDU allows to reconfigure the time delays within a certain interval, at difference of standard PaDeLs. This feature improves the pattern control flexibility, since it can become useful when the chip must be reprogrammed in the case of faults or different pattern requirements.

-*Insertion Loss, and Amplitude Uniformity*

Regarding the AU, it represents an issue common also to other implementations [2, 14], and it has been widely discussed above. Concerning the IL, the TTDU behaves exactly as a PaDeL. Indeed, apart from the constant losses related to the signal propagation and reflection, the IL is given by $10\log_{10}(2^B)$, B being the number of bits.

7. CONCLUSION

The performance of an integrated TPH for phased array antennas has been presented. Three different TTDU driving strategies have been considered. The presented TTDU allows realizing a phaser made by four 4 bits TSs to feed a four element OTSA, or by four 5 bits TSs to feed a phased array antenna in a sub-array configuration. The OTSA design criteria, the TPH insertion loss, AU and the statistical modelling of the TPH components realization defects have been discussed. Also a comparison with other similar architectures has been reported.

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