METHODS AND DESIGNS FOR IMPROVING THE SIGNAL INTEGRITY OF VERTICAL INTERCONNECTS IN HIGH PERFORMANCE PACKAGING

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Abstract—Design of high performance package interconnects using full-wave electromagnetic solvers is necessary due to increased operation speed, miniaturization and vertical 3D integration. Thus the segmented study and optimization is becoming inevitable for designers to improve the signal integrity of IC packaging. This paper addresses alternative methods and optimal designs on several components and structures for package electrical interconnects, including voiding technique, padless via implementation, spiral micro-via stacking and signal/ground layout pin patterns. The simulation results have been presented to demonstrate the improvements of optimized schemes. These methodologies could be treated as handy references and general guidelines applicable to different package designs and could result in significant improvements of overall package signal integrity performance.

1. INTRODUCTION

The actual trend in the silicon industry toward higher levels of integration and multi-core architecture generates chips with densities of hundreds of billions of transistors. As a consequence, the signal switching frequency across a broad range of electronic packaging technologies including system-on-chip (SoC) and system-on-package (SoP) is far beyond the gigahertz range. When the bandwidth requirement increases, the electrical properties of the interconnect affect and limit the integrity of the traveling digital signals [1–5]. These phenomena also have an impact on the electromagnetic compatibility (EMC) performance of the system since the corrupted signals can easily increase the unwanted electromagnetic interference (EMI).

Integrated circuit (IC) packaging is a critical link in the chip-package-board design flow. It serves as a spatial transformer between the chip and the board that includes horizontally routed traces and vertical interconnects comprising vias with their associated pads and anti-pads (also called voids). Higher frequencies of operation together with non-negligible coupling arising from high density interconnects mean that full-wave analysis is now compulsory and important for package analysis [6–10]. The vertical interconnect inside a package core layer substrate are plated through-holes (PTHs). Such a 3D structure contributes heavily to the degradation of the channel performance, increasing reflections and reducing the bandwidth. Therefore it is imperative that schemes have been developed to optimize the dimensions of the various features of these vertical interconnects.

With high speed transmissions, a PTH produces excessive capacitive loading, mainly due to the large pads at the PTH ends, which lead to impedance mismatch and signal discontinuity. On the other hand, a set of micro-via structures usually lies on top and/or bottom of the PTH. Although shown as rising vertically, stacked micro-vias in extra layers may rise at an angle around vertical axis, potentially to contribute to the inductive effect. The number of rise layers may depend on the number of dielectric layers needed for certain package functionality and power consideration.

This paper provides and analyses various design strategies for signal integrity (SI) optimization of 3D vertical interconnects in high performance IC package. Firstly, we propose to cut the voids and adjust the size of the voids above and beneath the via-pads in order to reduce the capacitive loading. Second, we study the pad size and various micro-via stacking schemes for routings in the build-up layers. Last we provide some guidelines of signal/ground layout pin pattern and differential via-pair orientation.

2. VOIDING FOR OPTIMAL PERFORMANCE

Figure 1 shows a cross-section of an IC package, which includes several key components along the electrical path such as C4bump on the top, main routing (microstrip or stripline with dual referencing), micro-vias, PTH, and ball grid array (BGA) solder balls on the bottom. As shown, there are large parasitic capacitances between the PTH/BGA pads and the adjacent metal layers, which can result in large impedance mismatches.

Therefore, in order to diminish the impedance discontinuity, we propose a method to cut the voids on those adjacent planes, shown as dashed circles in Figure 1. Figure 2 gives the 3D demonstration after
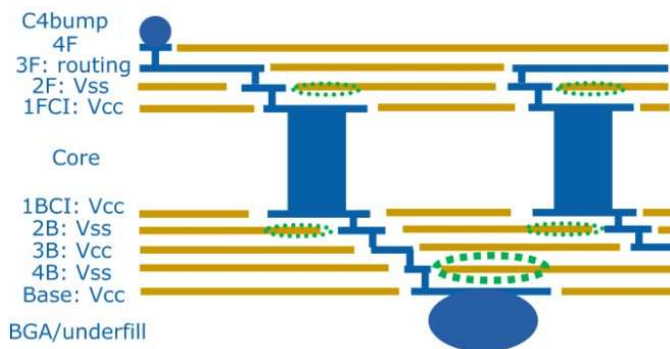
Figure 1. An illustration of the cross-section of an IC package.
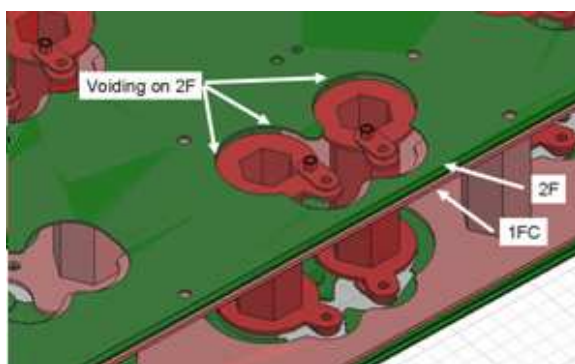

Figure 2. Voids cut above and beneath the PTH pads.

cutting the extra voids above and beneath the PTH pads.

We use the Ansoft Q3D to assess the parasitic capacitances against different void sizes. Figure 3 shows that beyond the ratio of 1.2 (void diameter/pad diameter) the enlargement of void becomes quite non-effective. The critical ratio of 1.2 is determined based on the nominal values of stackup thickness in various IC packages. Investigation also shows the cutting voids through all the layers on top/bottom of the PTH would reduce the parasitic capacitance to the best scenario.

We choose this ratio to optimize the signal integrity performance of high speed interface. However, on the other hand, the cheesed ground/power plane with many voids would cause potential risks of power delivery (PD) or metal balance war-page issues. If the power plane is not completely large, it may lead to voltage non-uniformity and IR drop issue. If the ground plane is cheesed, the cross-layer coupling may happen under the condition of poor referencing and shielding, or
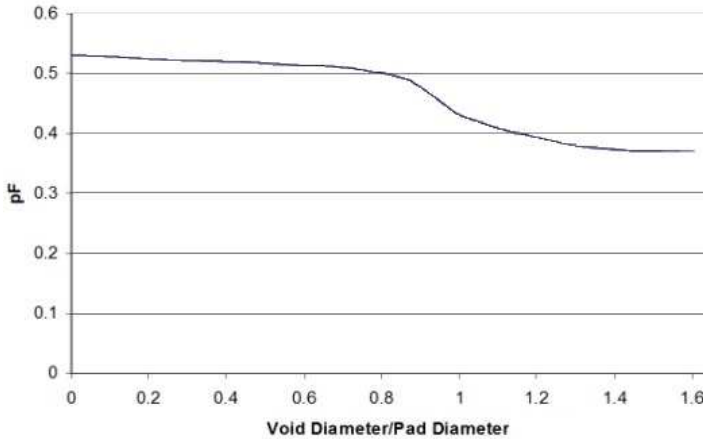
Figure 3. Parasitic capacitance of PTH-pad to adjacent plate with voiding.
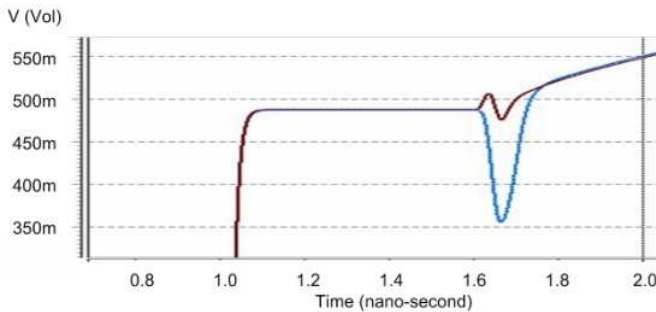

Figure 4. TDR plots of a step pulse into a package with and without using void technique.

even increase the length of return path loop. Therefore in the actual design, we should be careful of implementing the voiding techniques in order to balance the SI/PD co-design requirement.

We use Ansoft HFSS full-wave solver to model the structures with modifications, and then convert the model to the Spice-ready format for the transient analysis. Figure 4 shows the time domain refractometry (TDR) results of properly using voiding techniques. The blue curve of negative notch represents the original capacitive loading at PTH-pads, while red curve one gives the optimal voltage reflection after cutting the voids. It is observed that the signal discontinuity is greatly reduced by using large voids, while some small minor ripples

may still exist as the inevitable and combined effect of trace-feeding, micro-via stacking and PTH routing.

3. PADLESS PTH VIA

We propose and design the padless PTH via to further reduce the capacitive load from the conventional pads at the via-ends. It also may help shrink the spacing between vertical vias, which could facilitate a larger number of vertical interconnects and dense routing in the package. The through-hole could be plated without traditionally-large circular pad cover. The plated cap of the via-end is then not extended
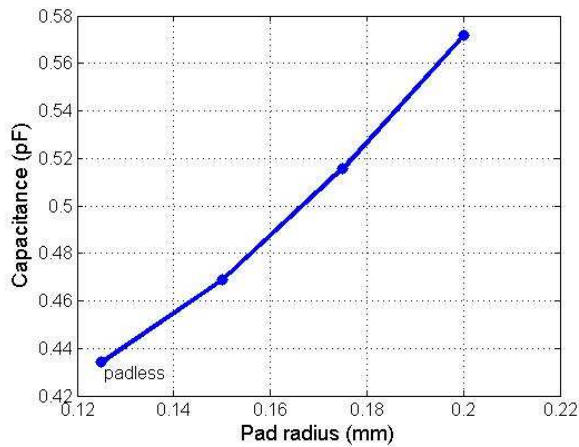

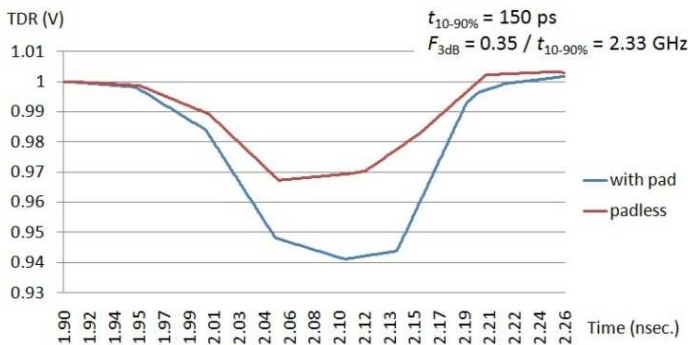**Figure 5.** Capacitances for various sizes of PTH-pads.

Figure 6. Comparison of TDR for a step impulse into a PTH.

beyond any edge of the through-holes. Thus, the PTH will rely on the incoming signals trace or shape to be anchored to the PTH with sufficient width to provide a plating tail and anchor point. By studying the reducing sizes of the via-pad, we found the smaller the size could definitely lead to the smaller capacitive load. Figure 5 shows that the padless case can provide the smallest value of capacitive load.

In Figure 6, we find the negative notch of the red plot is much smaller for a padless PTH design. The voltage reflection of a padless PTH design is 50% smaller than that of a design with large pads.

4. MICRO-VIA STACKING SCHEME

The typical patterns of the micro-via stacking are two kinds: straight-out and staggered as shown in Figure 7. From the intuitive perception, the straight-out micro-via stacking or its kind may provide better performance with less signal discontinuity against the staggered one, as the electromagnetic field is perceived as more smoothened from horizontal routing to vertical one in 3D view. But the actual electromagnetic simulation shows the staggered pattern gives the best performance, just because the voiding size is relatively large and all aligned vertically on top of the PTH pad.

Paper [1] has provided the actual simulation results of the structures with given dimensions in Figure 7. It means, whenever the stacking routing scheme change, the dominant factor is the voiding style that varies due to the different structural specifications.

Here, we introduce a new micro-via stacking technique by increasing the inductive effect along the micro-via to compensate the intrinsic capacitive load of the PTH pad [11]. As shown in Figure 8, the micro-via stacking pads in rising layers could form a path around an

(a)   (b)

Figure 7. Micro-via stacking: (a) the straight-out type, and (b) the staggered.

imaginary axis. The complete spiral structure may provide inductance which may at least partially offset the capacitance induced by the PTH, thereby helping to manage impedance along the transmission line. The shape of micro-pads can be circular, squared, or triangular. The enclosed loop around the axis can be in one turn or more to enhance the inductive effect. Usually the substrate with higher layer count would provide more loops.

For the differential via-pair, the micro-vias can be mirrored images of each other with corresponding turns and rises to match the signal path as closely as possible. Usually creating the LC-type component in the signal path would cause some band-pass filter-like effect at high frequency range [12, 13]. But for this new design, we have observed very minor issues on that. Figure 9 shows the red curve, labeling the squared
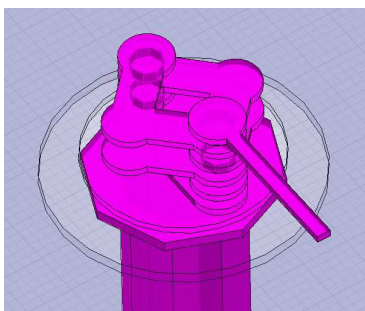

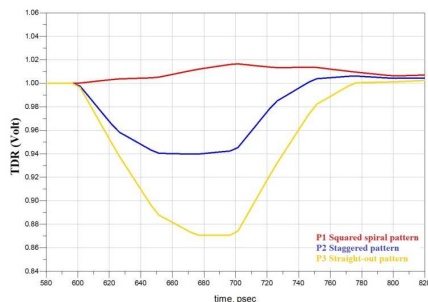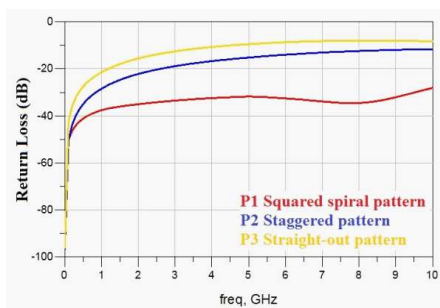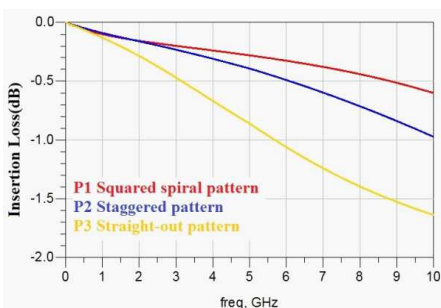**Figure 8.** Spiral micro-via stacking with squared pattern.

Figure 9. TDR of a step impulse into different micro-via stacking schemes.

(a)

(b)

Figure 10. (a) Insertion losses and (b) return losses of different micro-via stacking schemes.

spiral micro-via stacking, give the minimal TDR voltage reflection. In Figure 10, the spiral scheme shows the smaller insertion loss and return loss against other conventional designs. This verified the proposed spiral micro-via stacking scheme is helpful for improving the signal integrity along the vertical electrical path. We have also concluded and tabulated the LC parasitic of different micro-via stacking schemes in Table 1, in order to quantify the strong enhancement of self-inductance on the spiral structure. These values are assessed and simulated using Ansoft Q3D on the nominal design of micro-via stacking.
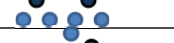
5. PTH SIGNAL/GROUND LAYOUT PATTERN

For differential signals going through the PTHs, the signal-to-ground (S/G) layout pin pattern is critical for the optimal return path loop and ground shielding. Usually the ground via is placed exactly on the central line of the differential via-pair. But when many pairs are crowded together in the actual design, we have to struggle and consider a few alternative ways of placing them around. Table 2 gives some

Table 1. LC parasitics of different micro-via stacking schemes.

Micro-via stacking pattern	Self-inductance (nH)	Capacitance (pF)
Squared spiral	2.053	0.4756
Staggered	0.995	0.4293
Straight-out	1.082	0.9372

Table 2. A guideline of differential PTH pin patterns and their performance.

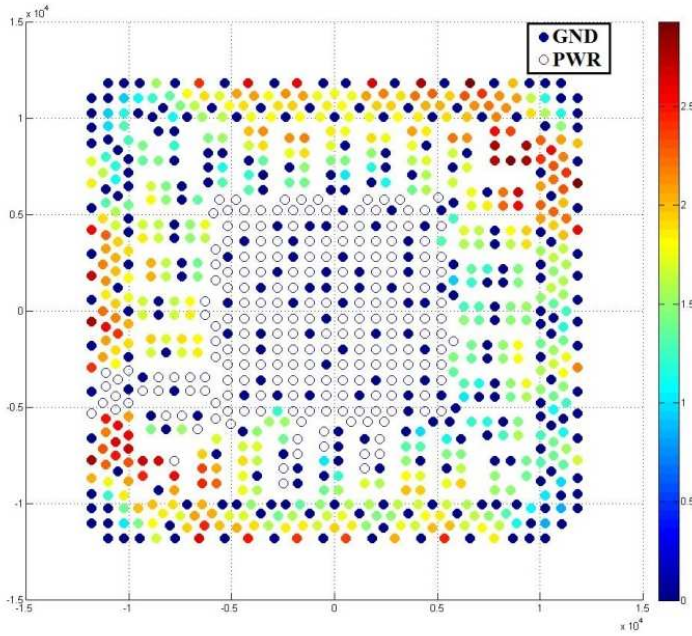| Diff PTH Pattern	NEXT @ 10 GHz	FEXT @ 10 GHz	IO density (mm² /pair)
	-54 dB	-54 dB	0.878
	-49.5 dB	-52.5 dB	1.025
	-36 dB	-37.5 dB	0.720
	-35.5 dB	-37.5 dB	0.855
	-41.5 dB	-41 dB	0.698
	-37 dB	-38.5 dB	0.675

Figure 11. SG ratio assessment on ball grid array layout.

typical patterns of S/G pin pattern and their corresponding crosstalk performance with IO density estimation. The black dots represent the ground vias, and the blue dots represent the signal ones. Then it becomes a real trade-off decision for designers to balance the physical constrains and electrical performances in the actual design.

In Figure 11, we present the BGA SG ratio assessment of a testing sample board. The blue solid dots represent the GND pins; while the unfilled dots label the PWR pins. Similarly, the power-to-ground (PG) ratio assessment can also be processed using modified numerical code in MATLAB. These SG and PG hot-maps could provide important signal integrity information and design automation to facilitate the hardware board designer to have a global view of the package electrical performance. The ground rule is to decrease the SG and PG ratio as small as possible. Usually 2:1 is ideal for differential pairs and 4:1 for single-ended one, which also leads to the compromise and alignment between board design and package design.

6. CONCLUSION

This paper addresses alternative methods and optimal designs on several components for package electrical interconnect. The simulation results have been presented to demonstrate the improvements of optimal schemes. These methodologies could be treated as handy references and general guidelines applicable to different package designs. The proposed methods could result in significant improvements of overall package signal integrity performance.

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