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A LOW POWER PUSH-PUSH DIFFERENTIAL VCO USING CURRENT-REUSE CIRCUIT DESIGN TECHNIQUE

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Abstract—This paper presents a complementary metal-oxide-semiconductor (CMOS) differential voltage-controlled oscillator (VCO) implemented with the push-push principle. The push-push VCO uses two frequency doublers stacked in series with an LC quadrature voltage-controlled oscillator (QVCO) to share the dc current with the QVCO for low power consumption. The proposed CMOS VCO has been implemented with the TSMC 0.18 μm CMOS technology, and the die area is $0.822 \times 1.564\,\mathrm{mm}^2$. At the supply voltage of 0.9 V, the total power consumption is 3.15 mW. The free-running frequency of VCO is tunable from 10 GHz to 11.15 GHz as the tuning voltage is varied from 0.0 V to 1.2 V. The measured phase noise at 1 MHz frequency offset is −114.93 dBc/Hz at the oscillation frequency of 9.99 GHz, and the figure of merit (FOM) of the proposed VCO is −190.0 dBc/Hz.

1. INTRODUCTION

A differential frequency source is a critical component in fully-integrated radio-frequency transceivers. The design of high-frequency source entails trade-offs among several parameters including the phase noise, power consumption, frequency tuningrange, power consumption and chip area. These parameters are lumped into an equation to indicate the figure of merit of the voltage-controlled oscillator (VCO) for performance comparison. The frequency signal source can be formed with (i) a fundamental oscillator, (ii) a low frequency source in conjunction with frequency multipliers, and (iii) a high-frequency source with frequency dividers. The second approach is

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gaining popular because the oscillation frequency can be beyond the cutoff frequency limitation of the active transistors. It enables the fundamental VCO to work at lower frequency, and the VCO can be designed with better spectral purity by exploiting the higher device gain and higher varactor Quality-factor (Q-factor) available at lower frequencies. It is not easy to design wide-band high-frequency VCO, because wide-band tuning requires large varactor tuning, which limits the operation frequency. A high oscillation frequency VCO can be designed via the parasitic cancellation [1] and a wide-band VCO can be designed using a tunable negative-inductance cell [2]. The second approach allows wide-band high-frequency generation.

A single-ended push-push frequency doubling signal can be tapped from a virtual node of a differential VCO [3, 4]. However, the strength of the push-push signal is small. A buffer amplifier is often used to enhance the signal strength of the 2nd harmonic [5]. The single ended second harmonic terminal is typically sensitive to on chip interference and noise. A balun and a differential amplifier are used to integrate the push-push VCO to provide a differential 2nd harmonic signal [6]. Alternatively, a differential push-push signal can be tapped from two balanced virtual grounds for fundamental in a quadrature voltage-controlled oscillator (QVCO) [7, 8]. The extracted signal strength is small and can be amplified by a 2nd harmonic regenerator [9]. The approach in [6] or [9] requires high power because it uses two dc current paths: one for VCO and the other for amplifiers.

A single-ended push-push signal can also be obtained by using a VCO and a frequency doubler [10], and the differential signal of the VCO is applied to the inputs of the doubler to generate the second harmonic. One dc current path for the doubler and the other current path for the VCO are used. This paper proposes a new differential push-push VCO composed of two single-ended output/differential input frequency doublers stacked in series with a quadrature VCO (QVCO) to reuse the dc current for low power consumption. The QVCO consists of two differential VCOs coupled by a ring transistor and provides the input signals to the frequency doublers, which are designed to enhance the strength of the output signals. The proposed push-push VCO circuit was implemented in the TSMC 0.18 μm complementary metal-oxide-semiconductor (CMOS) technology and operated in the 10 GHz band. The figure of merit (FOM) of the proposed VCO is −190.0 dBc/Hz comparable to those of fundamental VCOs. The proposed VCO circuit is a useful design when the operation frequency of VCO is seriously limited by the technology or by the low Q-factor at higher operation frequency close to millimeter wave.

2. CIRCUIT DESIGN

Figure 1 shows a CMOS frequency doubler, a pair of differential signals (S_1, S_2) is applied to the gates of (M_1, M_2) serving as amplifiers with a shared inductive load L_3. The frequency of input signal is the radian frequency ω_o, while the output frequency of the doubler is $2\omega_o$. The transistors (M_1, M_2) are biased to generate the second-order harmonics, at the inductive load that the fundamental signal and odd harmonics cancel, while the second harmonic and other even harmonics

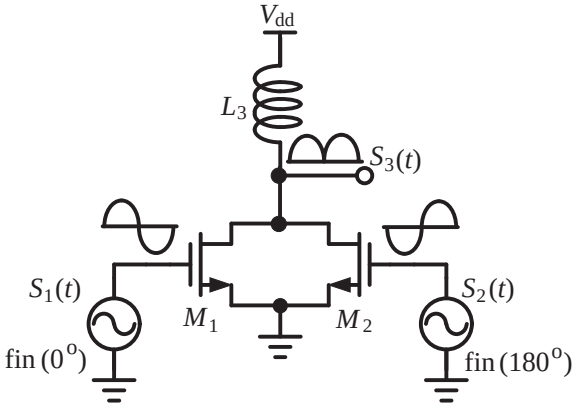


Figure 1. Schematic of a frequency doubler.

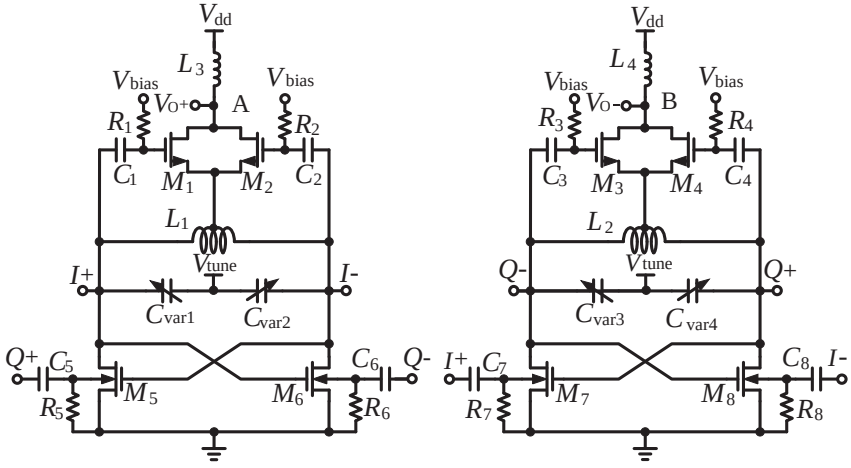


Figure 2. Proposed quadrature VCO using the body injection locked technique.

add constructively. The doubler generates single-ended clock frequency at $2\omega_o$ by using a differential clock signal at ω_o. The circuit can be combined with a differential VCO to provide a push-push single-ended output. The doubler can be placed parallel to a VCO or stacked in series with a VCO. The latter is a low power approach while the former is a low voltage approach. However, the combined circuit cannot provide a differential push-push signal.

Figure 2 shows the proposed differential push-push VCO composed of two frequency doublers stacked in series with respectively two differential VCOs coupled by 4 parallel back-gate lateral npn bipolar junction transistors (BJTs) to form a QVCO [11]. The resistors ($R_5 \sim R_8$) are the bias resistors and the capacitors ($C_5 \sim C_8$) are used for dc blocking. The parasitic npn BJTs are normally off because the bases are dc grounded. The n-metal-oxide-semiconductor field-effect transistors (nMOSFETs) (M_5, M_6), inductor L_1 and varactors (C_{var1}, C_{var2}) form one differential cross-coupled VCO. The nMOSFETs (M_7, M_8), inductor L_2 and varactors (C_{var3}, C_{var4}) form the other VCO. During the measurement, the common source of switching transistors is wired to a bonding wire and the V_{dd} is also tied to a bonding wire. The common node of bonding wire and transistors is a virtual ground for the fundamental and provides the push-push signal at $4\omega_o$ [12]. A virtual ground is also found at the common nodes of bonding wire and inductors (L_3, L_4), and L_1 and (M_1, M_2). The voltage V_{tune} is used for frequency control. The switching transistors provide negative differential resistance to compensate for the loss of the LC tanks. The first frequency doubler consists of (M_1, M_2), and L_3 is stacked in series with the first differential VCO with a common node shared by (M_1, M_2) and L_1. The second frequency doubler consists of (M_3, M_4), and L_4 is stacked in series with the second differential VCO with a common node shared by (M_3, M_4) and L_2. The capacitors ($C_1 \sim C_4$) are used for dc blocking, and ($R_1 \sim R_4$) are the bias resistors. The gate bias V_{bias} is larger than V_{dd}, also used to control the power consumption of the QVCO and as the bias voltage for the frequency doubler circuit. The common node of (M_1, M_2) and inductor L_1 is a virtual ground for the fundamental signal. Two common-source amplifiers for (0° ($2\omega_o$), 180° ($2\omega_o$)) output signals and 4 amplifiers for (0°(ω_o), 90°(ω_o), 180°(ω_o), 270°(ω_o)) quadrature signals are designed for measurement purpose.

Figure 3 shows the simulated voltage waveforms of the VCO and QVCO. Figure 3(a) shows the voltage waveforms of the transistors M_5 and M_6. The lower bound of QVCO output voltage is limited by the ground level when the transistors $M_5 \sim M_8$ are turned-on. The upper bound is above the V_{dd} level. Figure 3(b) shows the voltage waveforms

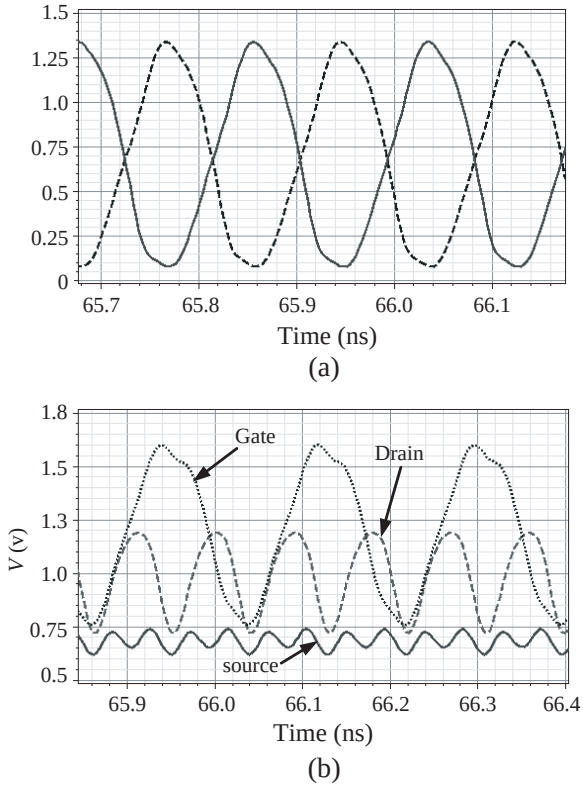


Figure 3. (a) Simulated output voltage of M_5 and M_6. (b) Simulated drain, source and gate voltages of M_1. $V_{dd} = 1\,\mathrm{V}$, $V_{bias} = 1.2\,\mathrm{V}$.

of M_1. The transistors M_1 and M_2 are switched on and off cyclically, which leads to the second-harmonic at the common drain of M_1 and M_2. The drain current i_{di} of M_i (i =1, 2) is modeled as

$$i_{di} = i_{oi} + a_{1i}x + a_{2i}x^2 + \tag{1}$$

where $x = A_i \cos(\omega_o t + \varphi_{i+})$ is the input gate voltage signal, i_{oi} the dc current component, a_{ij} ($j = 1, 2$ and $i = 1, 2$) the expansion coefficient, and φ_{i+} the phase. The net current of M_1 and M_2 is

$$\begin{aligned} i_{d1}+i_{d2} = &\left[\left(i_{o1} + i_{o2} + 0.5a_{21}A_1^2 + 0.5a_{22}A_2^2\right)\right] \\ &+[a_{11}A_1\cos(\omega_o t + \phi_{1+}) - a_{12}A_2\cos(\omega_o t + \phi_{2+})] \\ &+ \left[0.5a_{21}A_1^2\cos(2\omega_o t + 2\phi_{1+}) + 0.5a_{22}A_2^2\cos(2\omega_o t + 2\phi_{2+})\right] \end{aligned} \tag{2a}$$

The last term on the right hand side is the ac output signal which operates at twice the fundamental frequency. The second is the leakage

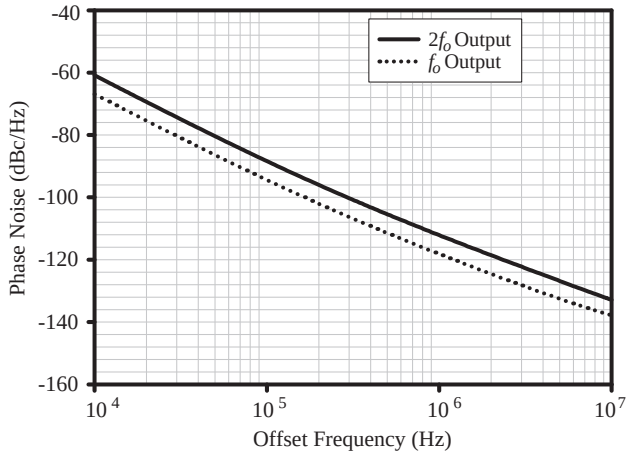


Figure 4. Simulated phase noises at the output voltages of M_5 and M_1. $V_{dd} = 1\,\mathrm{V}$, $V_{bias} = 1.2\,\mathrm{V}$, $V_{tune} = 0\,\mathrm{V}$.

of the fundamental signal to the output. The phase and amplitude errors, due to device and bias mismatch, and layout asymmetry are inevitable in practical circuit implementation, which can lead to the leakage of the fundamental at the doubler output. In addition, the amplitude and phase imbalance of input signals to the push-push circuit may also be the cause of the leakage. Ideally, the input signals are balanced, and no device mismatch occur. Equation (2a) becomes

$$i_{d1} + i_{d2} = [(2i_{o1} + a_{21}A_1^2)] + \left[a_{21}A_1^2\cos(2\omega_o t + 2\phi_{1+})\right] \qquad (2b)$$

Equation (2b) shows that ideally the phase noise of the push-push VCO is 6 dB higher than that of the QVCO output. This has been shown in Figure 4, where the simulated phase noises at the outputs of the transistors M_5 and M_1 are plotted.

In Figure 2, the outputs of QVCO have four phases, denoted by φ_{1+}, φ_{1-}, φ_{Q+} and φ_{Q-}. Ideally, the phase difference between $\varphi_{1+}/\varphi_{1-}$ and $\varphi_{Q+}/\varphi_{Q-}$ is 90 degrees. The outputs of the push-push VCO oscillate at second harmonic frequency. Ideally, the phase difference between the two VCO's outputs can be expressed as $2\varphi_{1+} - 2\varphi_{Q+}$. Mismatch of transistors and passive components affects QVCO phase error and VCO phase accuracy. This is the drawback of the differential push-push VCO. Therefore, the accurate generation of differential outputs depends upon accurate quadrature signal generation by the core QVCO. The two differential VCOs shown in Figure 2 can be seen as two first-harmonic injection locked oscillators (ILOs) with a locking range. The outputs of the first VCO are applied

to the injection npn transistors of the second VCO, and the oscillation frequency of the second VCO tracks with the oscillation frequency of the first VCO if the injection frequency falls in the locking range of the second ILO and vice versa. When there is a device mismatch between devices, the oscillation frequencies of the two ILOs differ. However, because the two sub-VCOs inter-lock to each other, the injection-locking mechanism reduces the phase error of the core QVCO and can improve the phase accuracy of the push-push differential VCO outputs. If the QVCO uses the quadruple-push [12] coupling alone, the oscillation frequency is the same as the resonance frequency. The coupling strength depends upon the oscillation frequency and the resonant frequency of the coupling tail LC tank, and the phase accuracy degrades as the oscillation frequency shifts away from tail resonance. The QVCO also uses the first-harmonic injection locking mechanisms to couple two differential VCOs and this is a wide-band approach. However, the oscillation frequency shifts away from resonance, and an increasing coupling strength degrades the phase noise. Both coupling techniques in the QVCO core are used to trade off the phase noise and phase accuracy.

The phase noise of QVCO is an important factor to determine the phase noise performance of the push-push VCO. The phase noise of the push-push VCO comes from three sources: The first one is the added noise generated by the devices (M_1, M_2), and this is mainly the thermal noise and the multiplied noise generated by the nonlinear harmonic mixing in the transistors (M_1, M_2). The last major source comes from the injection source due to the core-QVCO. Therefore, it is important to optimize the phase noise of the QVCO. It has been shown [13] that the near-carrier phase noise is reduced to 1/2 that of a single oscillator for two oscillators coupled by a reciprocal coupling network. An improvement of the phase noise of both the Rucker and quadruple-push oscillators, using four sub-oscillators coupling by a star and a ring coupler respectively with respect to a single oscillator, obtained by replacing the coupling network with a short-circuit termination, has been observed [14]. The differential cross-coupled VCO has a medium phase noise performance. The QVCO in the proposed circuit uses both the quadruple-push coupling technique and BJT coupling methods to minimize the phase noise of QVCO and improve the phase accuracy. The quadruple-push coupling technique is a passive low phase noise coupling technique similar to the method in [14], and the BJT coupling is also a low-phase noise approach similar to the method in [13]. Because the BJT is a bulk device, the parasitic BJT coupling technique is better than the parallel nMOSFET coupling and has lower flicker noise than the surface-channel nMOSFET.

3. MEASUREMENT RESULTS

The differential push-push VCO was designed and fabricated in the TSMC 0.18 μm 1P6M CMOS technology. Figure 5 shows the micrograph of the proposed push-push VCO with a chip area of $0.822 \times 1.564\,\text{mm}^2$ including the pads. Accumulation-mode MOS varactors are used for frequency tuning. Two 3-turn octagonal inductors for L_3 and L_4 are shown on the left-hand and right-hand sides. The rest two 3-turn octagonal inductors are for L_1 and L_2. The output spectra were measured using the Agilent E4407B spectrum analyzer. The oscillating frequency of push-push VCO can be tuned from 10.0 GHz to 11.15 GHz as shown in Figure 6. As the control voltage is increased, the varactor's

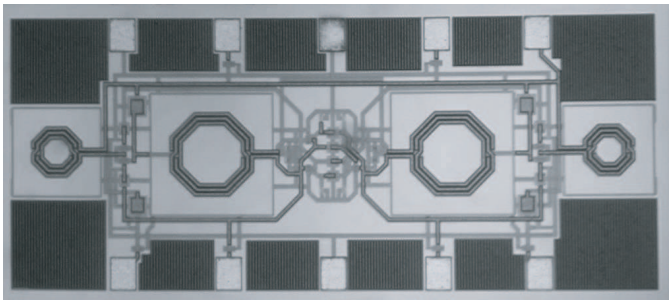


Figure 5. Chip photograph of the proposed push-push differential VCO.

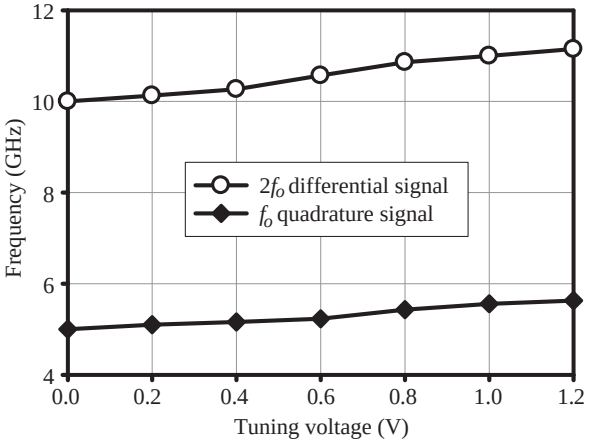
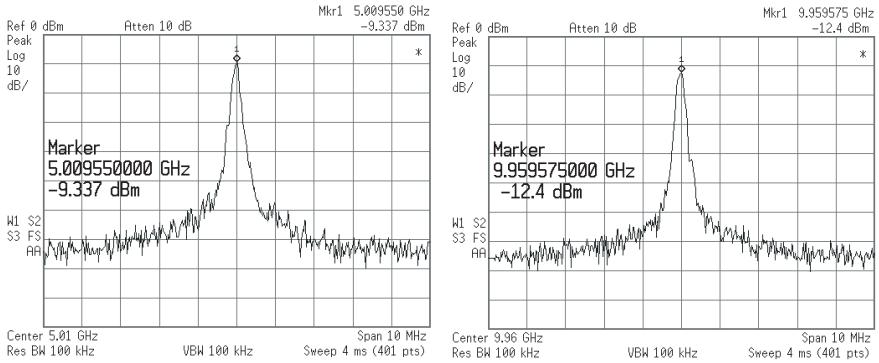


Figure 6. Measured tuning range of the VCO and QVCO. $V_{dd} = 0.9\,\text{V}$. $V_{bias} = 1.03\,\text{V}$.

capacitance decreases, therefore the output frequency increases. The power consumption of VCO core is 3.15 mW at the supply voltage of 0.9 V. Figure 7 shows the measured frequency spectra of the proposed VCO and the QVCO. The output power is $-9.337/-12.4$ dBm at 5 GHz / 9.96 GHz. Measured data in Figure 8 show that at the push-push VCO output, the first harmonic is smaller than the second harmonic by 26.98 dB. The small fundamental signal leakage to the outputs of the push-push VCO indicates the device mismatch, and phase and amplitude imbalance of the inputs are small. Figure 7 shows the measured phase noise at the oscillation frequency of 9.99 GHz. The phase noise is -114.83 dBc/Hz at 1 MHz offset frequency. Figure 9



(a) (b)

Figure 7. Measured spectra of the (a) differential VCO at 9.99 GHz, and (b) quadrature VCO. $V_{dd} = 0.9$ V, and $V_{tune} = 0.0$ V.

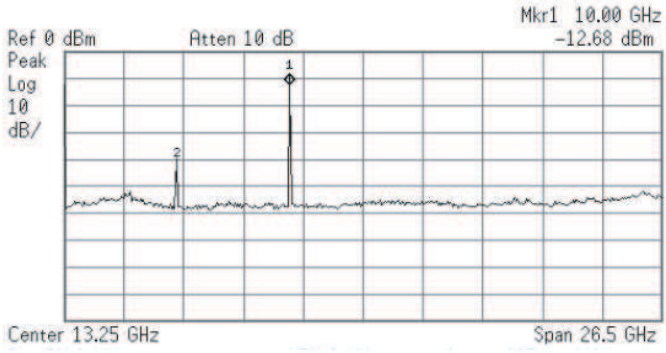


Figure 8. Measured full-span spectrum of the differential VCO. $V_{dd} = 0.9$ V, and $V_{tune} = 0.0$ V.

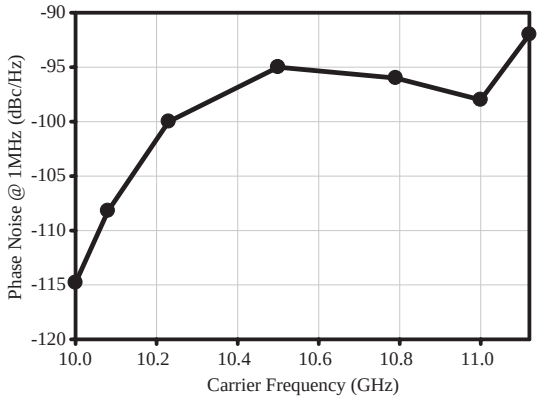


Figure 9. Measured phase noise of the differential VCO at 1 MHz offset frequency. $V_{dd} = 0.9\,\text{V}$, and $V_{tune} = 0.0 \sim 1.2\,\text{V}$.

Table 1. Comparison of VCO performance.

	This	[15]	[16]	[17]	[18]
Tech. (μm)	0.18	0.18	0.09	0.18	0.18
Freq. (GHz)	10	9.4	10.13	11.22	10.52
V_{dd} (V)	0.9	1.5	0.4	1.8	1.5
PN@1 MHz (dBc/Hz)	−114.83	−114.2	−108.78	−109.4	−122.4
P_{DC} (mW)	3.15	6.2	1.32	6.84	20.4
FOM (dBc/Hz)	−190	−185.5	−187.68	−181.8	−189.7
Tuning Range (GHz)	1.15	0.8	3.62	0.3	0.83
Tuning percentage	10.9%	8.6%	33%	3%	8.21%
Tuning Voltage (V)	$0 \sim 1.2$	$-1 \sim 2.5$	$0 \sim 1$	$1.6 \sim 2$	$0 \sim 2$

shows the measured phase noise at 1 MHz offset frequency. The measured phase noise of the push-push VCO output is higher than the phase noise of the QVCO output. The figure of merit (FOM) of this proposed push-push VCO is about −190.0 dBc/Hz, and it is defined as

$$\text{FOM} = L\{\Delta\omega\} + 10 \cdot \log\left(\frac{P_{DC}}{1\,\text{mW}}\right) - 20 \cdot \log\left(\frac{\omega_o}{\Delta\omega}\right) \tag{3}$$

where ω_o is the oscillating frequency, $\Delta\omega$ the offset frequency, $L(\Delta\omega)$ the phase noise at $\Delta\omega$, and P_{DC} the DC power consumption of the measured VCO. Table 1 lists the performance comparison of

VCOs with similar frequency band. The differential VCOs [16, 17] use a standard cross-coupled oscillator topology, and they cannot be used to generate frequency sources with higher frequency than the cutoff-frequency of active transistors. The QVCO [18] uses two differential VCOs to form a quadrature VCO and can be used as a differential VCO. Its upper operation frequency is also limited by the cut-off frequency of transistors. The proposed VCO has potential for generating higher frequency source than the reference VCOs.

4. CONCLUSION

A new push-push VCO circuit has been proposed and successfully implemented in the 0.18 µm CMOS technology. The circuit uses the fundamental quadrature signal outputs applied to the inputs of frequency doublers to generate differential 2nd harmonic. The prototype circuit is a low power circuit because it reuses the dc current for the sub-circuit blocks. And it can be used as a dual band VCO. The high band frequency range is from 10.0 GHz to 11.15 GHz and the low-band in the 5 GHz ISM band. The figure of merit for the proposed push-push VCO is −190.0 dBc/Hz while the VCO dissipates 3.15 mW for the whole VCO core from the supply voltage of 0.9 V. The prototype circuit is ready to extend to higher operation frequency range.

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REFERENCES

1. Chen, Y., K. Mouthaan, and F. Lin, "Design of X-band and Ka-band Colpitts oscillators using a parasitic cancellation technique," *IEEE Trans. Circuits and Systems I*, Vol. 57, No. 8, 1817–1828, Aug. 2010.
2. Chen, Y. and K. Mouthaan, "Wideband varactorless LC VCO using a tunable negative-inductance cell," *IEEE Trans. Circuits and Systems I*, Vol. 57, No. 10, 2609–2617, Oct. 2010.
3. Trotta, S., H. Li, V. P. Trivedi, and J. John, "A tunable flipflop-based frequency divider up to 113 GHz and a fully differential 77 GHz push-push VCO in SiGe BiCMOS technology," *Radio Frequency Integrated Circuits Symp.*, 47–50, 2009.

4. Cao, C., E. Seok, and K. K. O, "192 GHz push-push VCO in 0.13 lm CMOS," *Electronics Letters*, Vol. 42, No. 4, 9–10, Feb. 2006.
5. Molavi, R., S. Mirabbasi, and H. Djahanshahi, "A 27-GHz low-power push-push LC VCO with wide tuning range in 65 nm CMOS," *IEEE Int. Symp. Circuits and Systems*, 1141–1144, 2011.
6. Degani, O. and S. Ravid, "Differential output, transformer coupled push-push VCO and divider for 60 GHz applications in 90 nm CMOS," *IEEE Int. Conf. Microwaves, Communications, Antennas and Electronics Systems*, 1–4, 2009.
7. Yazdi, A. and M. M. Green, "A 40 GHz differential push-push VCO in 0.18 µm CMOS for serial communication," *IEEE Microw. Wireless Compon. Lett.*, Vol. 19, 725–727. 2009.
8. Wong, J. M. C. and H. C. Luong, "A 1.5-V 4-GHz dynamic-loading regenerative frequency doubler in a 0.35-µm CMOS process," *IEEE Trans. Circuits and Systems I*, Vol. 50, No. 8, 450–455, Aug. 2003.
9. Yang, C.-Y., C.-H. Chang, J.-H. Weng, and H.-M. Wu, "A 0.5/0.8-V 9-GHz frequency synthesizer with doubling generation in 0.13-µm CMOS," *IEEE Trans. on Circuits and Systems-II: Express Briefs*, Vol. 58, No. 2, 65–69, Feb. 2011.
10. Lee, O., J.-G. Kim, K. Lim, J. Laskar, and S. Hong, "A 60 GHz push-push InGaP HBT VCO with dynamic frequency divider," *IEEE Microw. Wireless Compon. Lett.*, Vol. 15, No. 10, 679–681, 2005.
11. Kim, H.-R., C.-Y. Cha, S.-M. Oh, M.-S. Yang, and S.-G. Lee, "A very low-power quadrature VCO with back-gate coupling," *IEEE J. Solid-State Circuits*, Vol. 39, No. 6, 952–955, Jun. 2004.
12. Jang, S.-L., C.-C. Shih, C.-C. Liu, and M.-H. Juang, "A 0.18 µm CMOS quadrature VCO using the quadruple push-push technique," *IEEE Microw. Wireless Compon. Lett.*, Vol. 20, 343–345, Jun. 2010.
13. Chang, H.-C., X. Cao, U. K. Mishra, and R. A. York, "Phase noise in coupled oscillators: Theory and experiment," *IEEE Trans. Microw. Theory Techn.*, Vol. 45, No. 5, May 1997.
14. Ramírez, F., M. Pontón, S. Sancho, and A. Suárez, "Stability analysis of oscillation modes in quadruple-push and Rucker's oscillators," *IEEE Trans. Microw. Theory Techn.*, Vol. 56, No. 11, Part 2, 2648–2661, Nov. 2008.
15. Liao, Y.-S. and C. F. Jou, "X-band low phase noise quadrature CMOS VCO with transformer feedback," *PIERS Proceedings*,

Hangzhou, China, Mar. 24–28, 2008

16. Jang, S.-L., Y.-S. Chen, C.-C. Liu, and M.-H. Juang, "A 33% tuning range voltage-controlled oscillator robust to environmental variation," *Micro. and Opti. Tech. Lett.*, 517–519, Mar. 2011.
17. Oh, N.-J. and S.-G. Lee, "11-GHz CMOS differential VCO with back-gate transformer feedback," *IEEE Microw. Wireless Compon. Lett.*, Vol. 15, No. 11, 733–735, Nov. 2005.
18. Jang, S.-L., S.-S. Lin, C.-W. Chang, and S.-H. Hsu, "Quadrature VCO formed with two Colpitts VCO coupled via an LC-ring resonator," *Progress In Electromagnetics Research C*, Vol. 24, 185–196, 2011.