Progress In Electromagnetics Research, Vol. 119, 59–84, 2011

A CONTRIBUTION TO LINEARITY IMPROVEMENT OF A HIGHLY EFFICIENT PA FOR WIMAX APPLICATIONS

L. El Maazouzi[1,*], A. Mediavilla[1], and P. Colantonio[2]

[1]Department of Communication Engineering, University of Cantabria, Santander, Spain

[2]Department of Electronic Engineering, University of Roma "Tor vergata", Italy

Abstract—This paper describes the design of a highly efficient and linear GaN HEMT power amplifier which may be used in WiMAX application. To improve linearity of highly efficient power amplifiers, a technique using diodes in the gate DC path was applied to TL and 2HT amplifier. This solution using diodes offers a good manner to improve linearity near saturation zone compared to the approach using only a DC gate resistor for TL (tuned load) case as well as for 2HT (second harmonic tuning approach). A 2.5 GHz 2HT power amplifier circuit was built, and measured data confirm the linearity improvement, particularly near saturation zone, as predicted by simulation, maintaining higher power performances. An output power of 36.8 dBm has been measured with an associated power added efficiency of 46.5% and carrier to third order intermodulation ($C/I3$) of 53.4 dBc. A 2HT PA also exhibits good performances across the full (2.3–2.7) GHz band. An output power ranging from (35–36.9) dBm with an associated gain of 12.9 ± 0.9 and a power added efficiency ranging from (40–46)% are measured across the full (2.3–2.7) GHz band.

1. INTRODUCTION

The deployment of modern digital telecommunication systems, with continuously increasing capacity, has demanded a steady improvement of the RF front-end's performance. The PA designer is therefore in front of a difficult trade-off among the contrasting goals of

Received 16 May 2011, Accepted 24 June 2011, Scheduled 21 July 2011

* Corresponding author: Latifa El Maazouzi (Latifa_maaz@yahoo.com).

high transmitted power, low power consumption and, for many telecommunication systems, highly linear operation. Given the widespread diffusion of many telecom applications, all of the above specifications have to be fulfilled keeping unit cost to a minimum. Such goals and the resulting compromise may vary depending on the type of radio link to be established and overall system requirements. For mobile handset, the power amplifier (PA) is the circuit where power gain (G_T), output power (P_{out}), power added efficiency (PAE), and intermodulation distortion (IMD) requirements are still difficult to be simultaneously fulfilled.

Power amplifier designed by following second harmonic tuning (2HT) approach (i.e., 2nd harmonic is optimised, while the 3rd and higher harmonics are short-circuit) using GaN HEMT technology has shown high power performance in term of efficiency, gain and output power [1–4], stressing also the relevance of input harmonic terminations. Regarding the linearity performances of harmonic-controlled PAs, high-efficiency tuning does not necessarily imply detrimental linearity effects [5]. On the contrary, an analytical and experimental work reported in [6–8], has demonstrated an improvement of linearity of PAs designed using HT approaches over Tuned Load (TL, i.e., short circuiting harmonic terminations) class AB amplifier. Moreover, harmonic injection techniques have been proposed to optimise linearity performances [14]. In any case, however, linearization techniques, such as feedback, feed forward [22], or predistortion [9–15], could be used to further improve the linearity. Feedback is good for audio power amplifiers, but for RF power amplifiers the stability and efficiency can be compromised. System-level feed forward or predistortion can be useful for RF frequencies, but the overall efficiency will be decreased because extra components have to be added.

For successful design of linear power amplifiers, suitable techniques must be developed to maintain high levels of both efficiency and linearity. For example, to achieve high efficiency, devices must be biased in the class AB to class B range, which reduces linearity compared to class A operation. There are some particular PA features that provide a way to escape from this apparent dead end. One of such PA characteristics resides in the so-called large-signal IMD sweet-spots, i.e., a deep in the IMD vs. P_{in} plot [16, 17]. IMD sweet-spots can be understood as the result of interactions between the PA mild and strong nonlinearities [18]. The former are determined by the PA quiescent operating point, and govern the circuit's small-signal nonlinear distortion. The latter are determined by the device current turn-on and current saturation (found when signal excursion reaches

the triode region of FETs or the saturation region of bipolar devices), and govern large-signal distortion effects.

Given this large-signal sweet-spot origin, it becomes clear that the parameters controlling the on-set of saturation (namely the biasing voltages and the load terminations) can be effectively used to produce a sweet-spot at the desired operating power level [17]. Lowering the gate-to-source DC voltage in a FET amplifier would move the point of optimum linearity to higher input power levels.

In this contribution, an approach based on the gate bias adjustment, in accordance with the input signal to optimize linearity and maintain high efficiency, by using diodes in gate DC path is presented. In order to demonstrate the proposed approach for a 2nd HT power amplifier design, an hybrid amplifier for 2.5 GHz application was realized and its experimental results are discussed. The active device used for the PA design is a Nitronex NPTB00004 GaN HEMT, whose quiescent bias point was settled at $V_{DD} = 28\,\text{V}$ and $V_{GG} = -1.5\,\text{V}$. For the gate bias shaping a Schottky diode was adopted.

The architecture was simulated by using AWR CAD tool and the designed amplifiers in this work are built on Rogers RT/DUROID 6010 board with a dielectric constant of 10.2.

The paper is organised as following: in Section 2, the proposed approach is described, while in Section 3 its application to a tuned load (TL) power amplifier (drain voltage second and third harmonic short-circuited) is discussed, with the aim to enhance the linearity near the saturation zone, where power performances are optimal. In Section 4, the effectiveness of this technique was evaluated for a highly efficient power amplifier, designed by means of 2HT approach [1–4]. In order to demonstrate the proposed approach for a 2nd HT power amplifier design, an hybrid amplifier for 2.5 GHz application was realized and its experimental results are discussed in Section 5.

2. A DYNAMIC GATE BIAS TECHNIQUE

Intermodulation behaviour of power amplifier in small input signal can be expected with only fifth-degree Taylor series:

$$I_{ds}(t) = G_0 + G_1 \cdot V_{in} + G_2 \cdot V_{in}^2 + G_3 \cdot V_{in}^3 + G_4 \cdot V_{in}^4 + G_5 \cdot V_{in}^5 \quad (1)$$

If two-tone signal is applied, the gate voltage is set as:

$$v_{in} = V_{GS} + A\cos(\omega_1) + A\cos(\omega_2) \quad (2)$$

where V_{GS} is the DC gate voltage and A is the magnitude of the applied input voltage.

G_n is the nth order derivative of the current I_{ds} given by:

$$G_n = \frac{1}{n!}\frac{\partial^n Ids(t)}{\partial v_{in}}\bigg|_{v_{in}=V_{GS}} \tag{3}$$

The IMD at $2\omega_2 - \omega_1$, including components up to fifth order, will be [21]:

$$SS_{Iout}(2\omega_2 - \omega_1) = \frac{3A^3}{8} \cdot G_3 + \frac{50A^5}{32} G_5 \tag{4}$$

$$SS_{Iout}(2\omega_2 - \omega_1) = \frac{3}{8}\left(G_3 + 4G_4 V_{GS} + 10G_5 V_{GS}^2\right) A^3 + \frac{25}{16}(G_5)A^5 \tag{5}$$

In a large input signal, a higher Taylor series degree must be used. Carvalho and Pedro have mathematically formulated the overall IMD behaviour by integrating the small and large signal contributions in closed form analytical expression [21].

$$\begin{aligned} I_{out}(2\omega_2 - \omega_1) &= \frac{2j}{AT_1T_2} \int_{-T_1/2}^{T_1/2} \int_{-T_2/2}^{T_2/2} f_{NL}[v_{in}] \cdot e^{j\omega_1 t_1} \cdot e^{-j\omega_2 t_2} dt_1 dt_2 \\ &= LS(A,\, 2\omega_2 - \omega_1) + SS_{Iout}(2\omega_2 - \omega_1) \end{aligned} \tag{6}$$

where, V_{in} is given in Equation (2) and $LS(A,\, 2\omega_2 - \omega_1)$ is Large-signal IMD contribution [21].

If $I_{out}(2\omega_2 - \omega_1)$ have a phase of 0° in small signal region and then tends to 180° for its large signal regime, it must have a zero, which results from the interaction between large and small signal contribution. Since $SS_{Iout}(2\omega_2 - \omega_1)$ depend on device bias, its phase can be optimised to assure the appropriate phase with respect to large signal one to minimize the third order intermodulation distortion by the optimization of device bias behaviour. In this regard, a linearization technique based on the insertion of diode in gate DC path is proposed with the aim to adjust gate bias conditions (DC current limitation) to achieve the desired IMD3 minimization.

Thus the dependence of the IMD optimum operating point with bias conditions, offers the possibility of properly control its appearance. In a relevant work reported in [19], it has been suggested to use a resistor in DC gate path as a means to dynamically adjust the gate voltage bias V_{GS}. The use of an adequate gate bias resistor was shown to be useful in producing a wide linearity sweet-spot in junction FET devices. However the use of high value of gate bias resistor could result in an important power added efficiency reduction. This problem can be corrected by the use of a diode in the gate DC path as a means to dynamically adjust the gate voltage bias V_{GS}, while maintaining high power performance.

Assuming a piece-wise linear approximation for the Schottky input gate-source junction, whose built-in voltage is V_{bi}, and dynamic conductance is G_{gs}, subject to a biased two-tone excitation $V_{GS}(t)$ expressed as [19]:

$$V_{GS}(t) = V_{gs1} \cdot \cos(\omega_1 t) + V_{gs1} \cdot \cos(\omega_2 t) + V_{GS} \tag{7}$$

The resulting rectified gate DC current can be approximated by [19]:

$$I_G(\mathrm{DC}) = \frac{4}{\pi^2} \cdot G_{gs} \cdot \frac{(\sin\theta - \theta \cdot \cos\theta)^2}{1 - \cos\theta} \cdot V_{gs1} \tag{8}$$

where $\theta = \cos^{-1}(\frac{V_{bi} - V_{GS}}{V_{gs1}})$ and $V_{gs1} = \sqrt{8 \cdot R_s \cdot P_{in}}$.

Since this rectified DC current is directly proportional to the input voltage V_{gs1} and thus to the input power level P_{in}, it can be employed for the desired dynamic control of the active device V_{GS}. For this purpose, Schottky diode in the gate DC path can be added, as shown in Figure 1, where the resistor Rg is used for the active device stabilization. For the latter, a value lower than $100\,\Omega$ is recommended to avoid power performances deterioration.

Due to the diode insertion, the DC voltage across the device can be written as:

$$V_{GS} = V_{GG} - Rg \cdot I_G(\mathrm{DC}) - V_D \tag{9}$$

where for the semiconductor diode, the following standard equation relating its current to its voltage can be used to extract the voltage across the diode V_D:

$$I_G(\mathrm{DC}) = I_0 \cdot \left[e^{\frac{qV_D}{nKT}} - 1 \right] \tag{10}$$

The insertion of diode in gate DC path has also a benefit in limiting dynamically the DC gate current. The diode converts nonlinearly the average gate current into a voltage drop in series with the gate voltage supply (Equation (9)). Depending on the input RF power, the resultant DC voltage applied to the gate is dynamically adjusted in order to reduce the gate current when high input RF power is driven into the active device, thus linearity improvement is predicted by DC current limitation approach. A small change in current DC results in change in the voltage dropping across the diode; this gives the possibility to adjust the DC voltage in small and large signal, while a resistor Rg is used to control the change in DC Voltage.

3. LINEARITY IMPROVEMENT OF TL PA

To demonstrate the effect of this technique on linearity, two tuned load (TL) PAs are designed using bias circuits with and without diodes. It

is to highlight that TL approach consists in short circuiting input and output voltages harmonic terminations, as result the drain voltage is a sinusoidal and the output current is a rectified waveform as shown in Figure 4.

The corresponding layouts of the two designed TL amplifiers are given in Figures 2 and 3, respectively, whose simulated performances

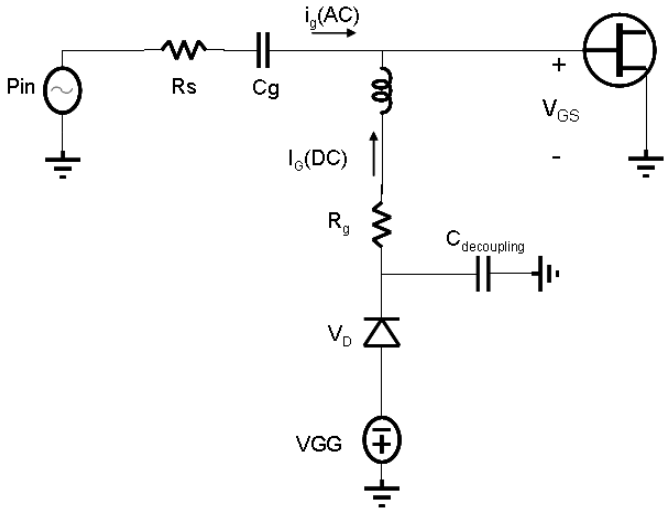


Figure 1. Gate bias circuit employed for limiting the gate current using a diode.

Table 1. Performances of stabilized TL PA designed using gate bias resistor and diodes compared to TL PA designed using only gate bias resistor in gate DC path at 1 dB compression point.

	P_{in} (dBm)	P_{out} (dBm)	PAE (%)	Gain (dB)	$C/I3$ (dBc)
TL PA (without diodes: Figure 2)	25.4	36.65	34.46	11.25	19
TT PA (using diodes: Figure 3)	25.21	36.23	34.35	11.01	40

at 1 dB compression are resumed in Table 1. From these results, we can observe that the addition of two series diodes in gate DC path with purpose to improve linearity doesn't cause any loss in power performances, while a remarkable improvement in Carrier over Third order intermodulation ($C/I3 = P_{out@f1}/P_{out@2f1-f2}$) performance is experienced, enhancing from 19 to 40 dBc when diodes are used in the gate bias path.

In Figure 5 are reported the 2 tones simulation, performed at the center frequency of 2.5 GHz and tone spacing of 10 MHz. From this figure we remark that the use of the stabilizing resistor Rg results on appearance of a sweet spot at an input power level $P_{in} = 21$ dBm, with an associated $C/I3$ of 45 dBc. The $C/I3$ corresponding to this sweet spot has been further improved by 20 dBc, adding 2 series diodes in DC gate path (Figure 3). Moreover the linearity has been improved for all

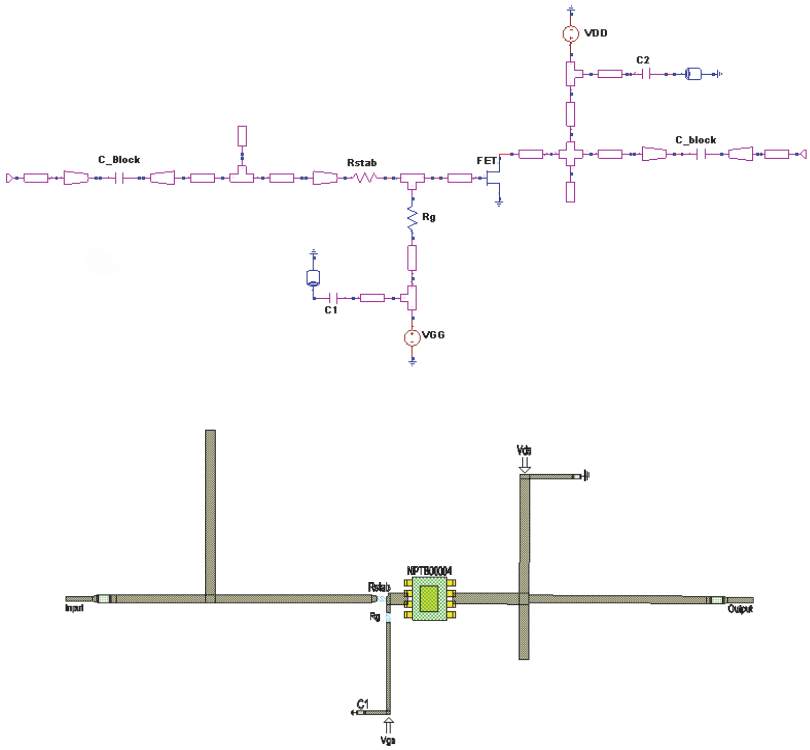


Figure 2. Layout of stabilised TL PA and its corresponding schematic designed using only resistor in gate DC path.

the input power range, introducing diodes in gate DC path, compared to the case where only the gate resistor Rg is used. Finally, it has to remark that approaching the saturation zone, where the output power and efficiency are optimal, the use of diodes results in an interesting

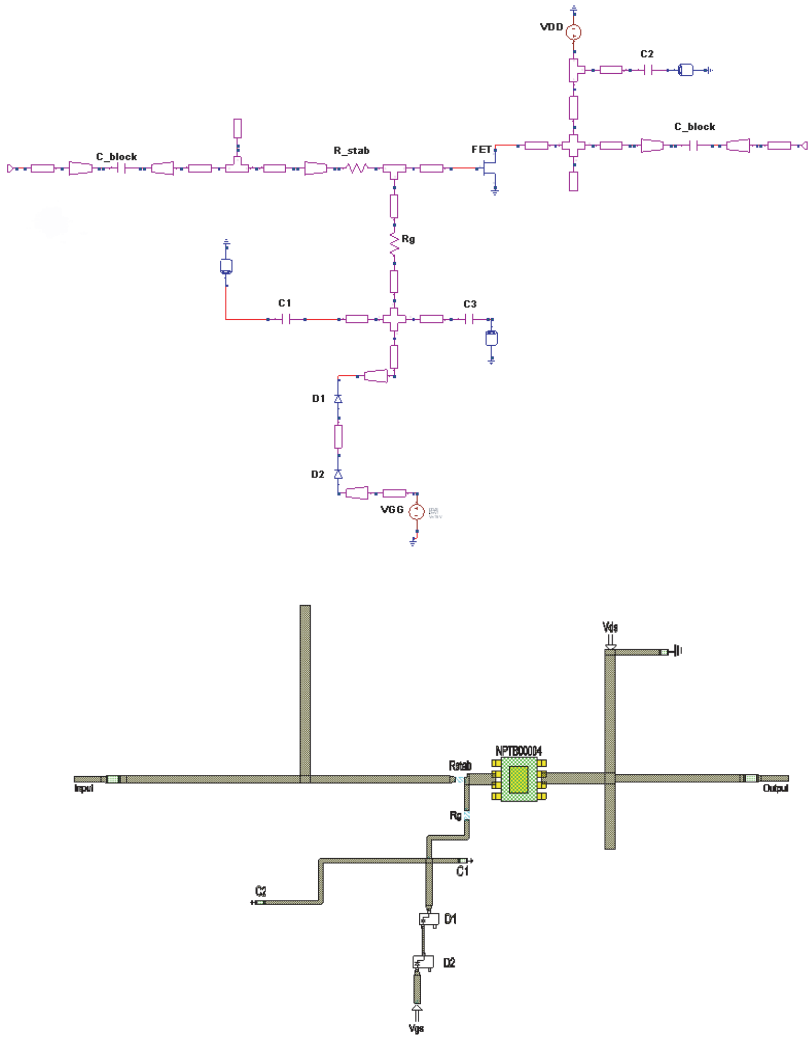


Figure 3. Layout of stabilised TL PA and its corresponding schematic designed using gate bias resistor and diodes in gate DC path.

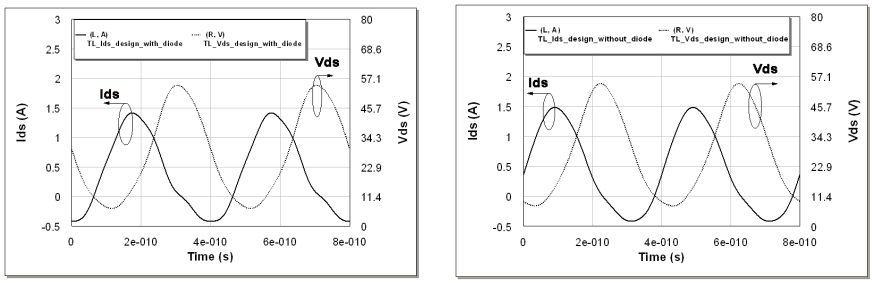
improvement of the third order intermodulation. In fact, a second sweet spot of $C/I3 = 40$ dBc has been generated at the input power around 1 dB compression point.

4. LINEARITY IMPROVEMENT OF 2HT PA

In the following, we focus to apply the proposed techniques to enhance linearity by a dynamic adjustment of DC gate voltage VGS using diodes, to a 2nd HT PA design. As in the TL design previously described, the device used is a Nitronex NPTB00004 GaN HEMT. The 2nd HT PA is designed to operate at 2.5 GHz and the device quiescent bias point was settled to $V_{DD} = 28$ V and $V_{GG} = -1.5$ V. The device has been preliminary stabilized for all operating frequencies using losses elements on the gate site.

It is to highlight that for the 2nd HT PA, the fundamental frequency and second harmonic input and output terminations have been optimised by means of the approach described in [1–4], while the third harmonic is short circuited. This approach results in drain voltage waveform that is roughly half sinusoidal.

After finding the adequate value of the resistor Rg for stabilisation of power amplifier, a 2nd HT power amplifier has been designed without considering the diode in the gate path, resulting in the layout depicted in Figure 6. Output matching circuit is optimised to short circuit the third harmonic and to terminate the fundamental and the second harmonic by its proper values, using topology given in [20]. Later, the design was modified by adding a single diode or a couple of diodes on the gate DC access point, as shown in the layout reported



(a) (b)

Figure 4. Simulated time domain current and voltage waveforms of designed TL PAs using (a) diode in gate DC path and (b) without diode.

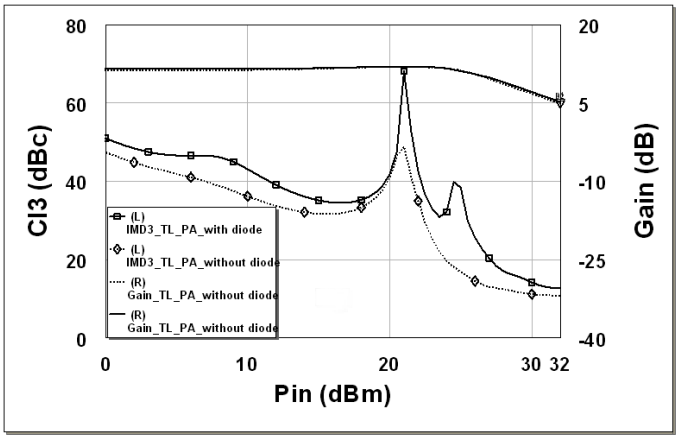


Figure 5. Simulated $C/I3$ performances of stabilised TL PAs using gate bias resistor and diodes compared to TL PA designed using only gate bias resistor in gate DC path.

Table 2. Simulated power performances of designed 2HT amplifiers with gate bias circuit composed by a single diode, 2 series diodes and without diodes.

	P_{in} (dBm)	P_{out} (dBm)	Gain (dB)	PAE (%)	$\text{PAE}_{\max}$ (%)
2HT PA (without diode: Figure 6)	25.1	37.95	12.85	47.98	49
2HT PA (single diode)	24.9	37.28	12.38	49.3	51.5
2HT PA (2 diodes: Figure 7)	24.9	37.28	12.38	49.3	51.5

in Figure 7. The resultant drain current and voltage waveforms of designed 2HT amplifiers are given in Figure 8.

The simulated power performances are summarized in Table 2 at 1 dB compression point, making a comparison between the different approaches on the DC gate access point, i.e., comparing the classical design to the case where a single diode or a couple of diodes were used. From these results we remark that power performances are quite close. The introduction of diodes in the gate DC path doesn't

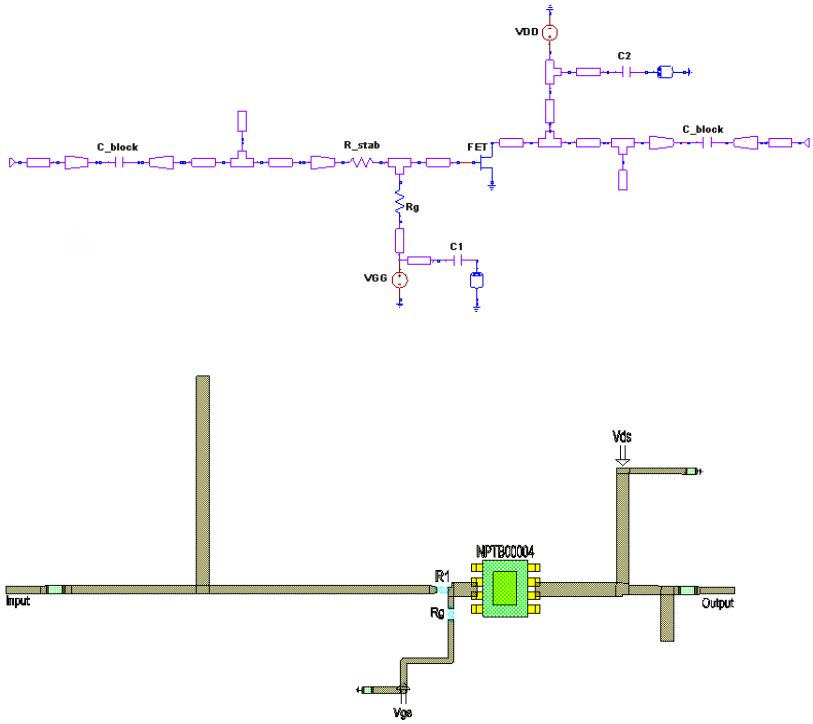


Figure 6. Layout of stabilised 2HT PA and its corresponding schematic designed using gate bias resistor of 68 Ω in gate DC path.

cause an important loss in power performances. Compared to power performances of TL amplifier, results obtained by designed 2HT amplifiers demonstrate the expected improvement of roughly 41% as was reported in [1–4].

Regarding current harmonic components evolution in Figure 9, we remark that the insertion of diode in the gate DC path results in reduction of DC current consumption and an increase of current component at the fundamental. Thus the use of diode has also the benefit to increase the power performances, and in particular the efficiency, as can be seen from Table 2. However the use of high gate resistor value for current limitation with the purpose to improve linearity as was reported in [19], results in efficiency deteriorations. Therefore the use of diode has a benefit of improving linearity as well as improving power performances or at least maintaining same level of power performances obtained before the insertion of diodes. Current

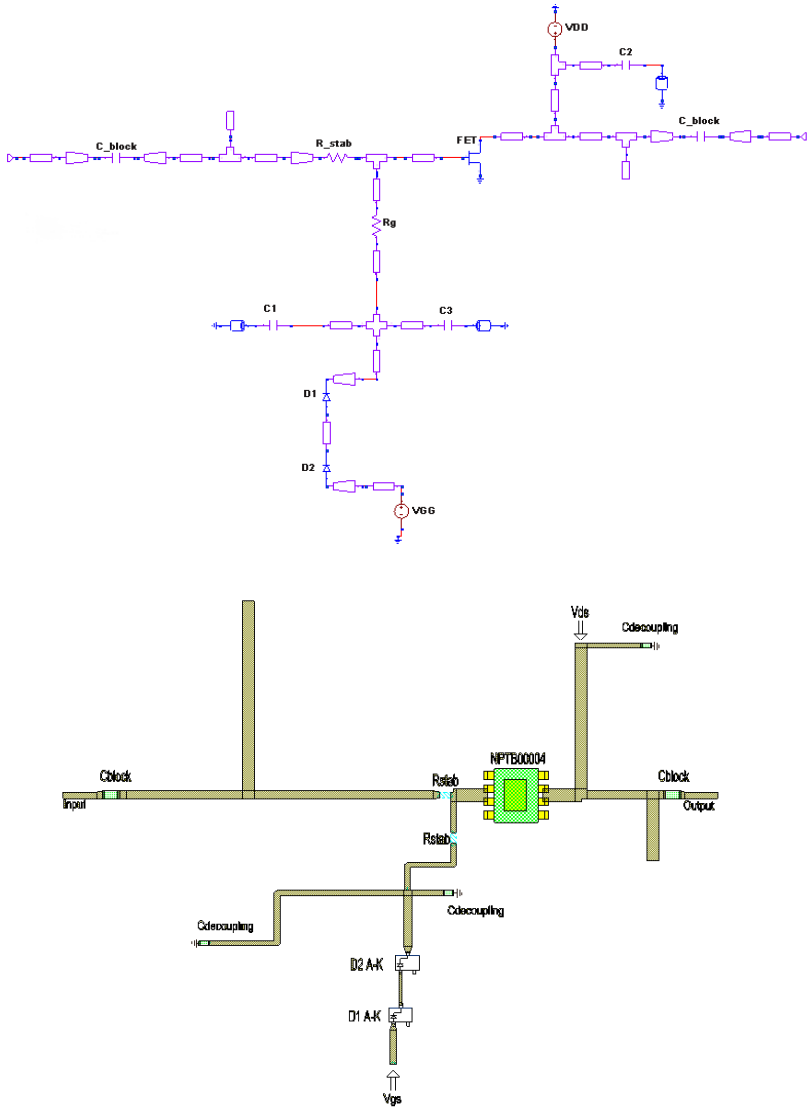


Figure 7. Layout of stabilised 2HT PA using two series diodes in the gate DC path and its corresponding schematic.

components evolution using single or a couple diodes are quite closes, that justify the fact that there is no change in power performance using single or couple diodes in Table 2.

To illustrate the evolution of input harmonics after the insertion

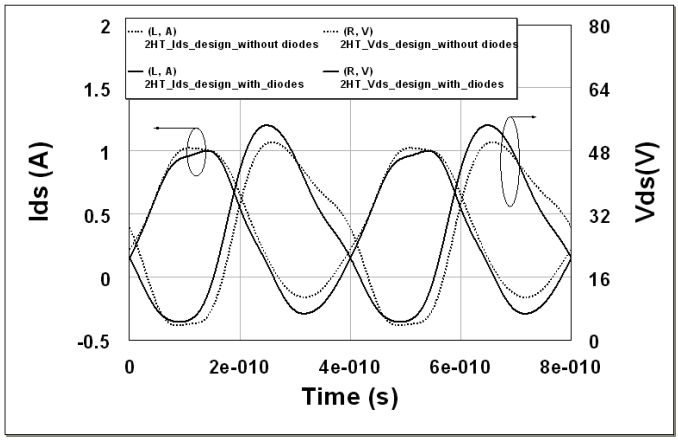


Figure 8. Simulated time domain current and voltage waveforms of designed 2HT PAs using diode in gate DC path and without diode.

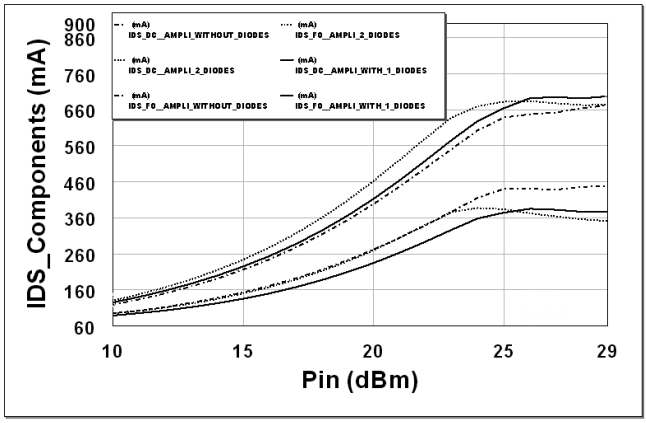


Figure 9. Current harmonic components for 2HT design without diode and with single and a couple of diodes.

of diode, output power at the fundamental and at the second and third harmonics are presented in Figure 10, where no significant change is observed in input power harmonics after the insertion of diodes, particularly in large signal conditions.

The result of 2 tones simulation with tone spacing of 10 MHz is illustrated in Figure 11. In term of linearity, the benefit of the use of diodes in the gate DC path can be seen clearly from this figure, where

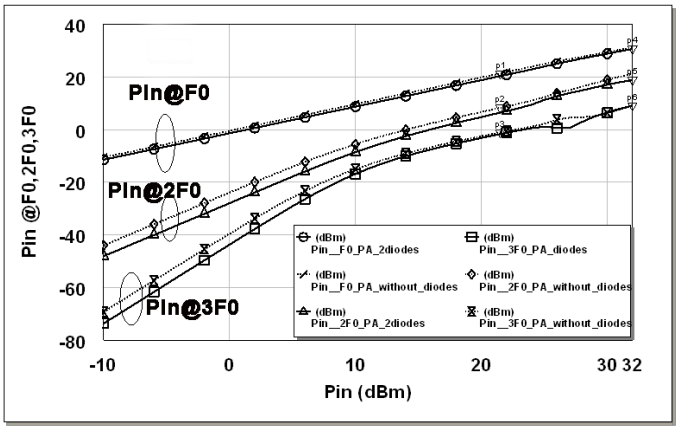


Figure 10. Power in the device input at the fundamental (f), second (2f) and third hramonic (3f) frequencies.

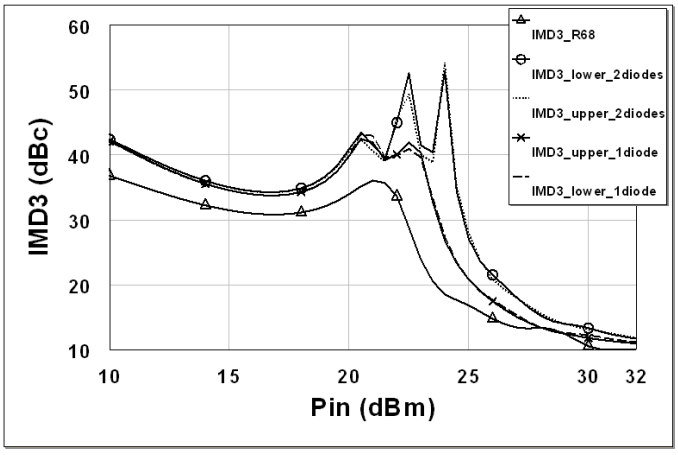


Figure 11. IMD3 of stabilised 2HT PAs with gate bias circuit composed by only a resistor and using single and two diodes.

the simulated $C/I3$ performance of the power amplifiers designed using a single diode, two diodes (Figure 6) or without diodes, i.e., considering only the stabilizing resistor $Rg = 68\,\Omega$ (Figure 5), are presented as function of the input power. An enhancement of $C/I3$ for all input power range can be clearly observed from this figure when using single or two series diodes in DC gate path.

For input power less than 21.5 dBm the same level of linearity is obtained using a single or two series diodes, whereas for input power near saturation region, a remarkable enhancement of $C/I3$ using 2 diodes is obtained compared to the case where a single diode is used. Two maximums of $C/I3$ of 43 dBc and 42 dBc are obtained using a single diode at $P_{in} = 21$ dBm and $P_{in} = 22.5$ ($P_{in,\,1\,\mathrm{dBcomp}} - 2.4$ dBm), respectively, whereas using two diodes two maximums of $C/I3$ of 50 dBc and 54 dBc are observed for input power levels of 22.5 dBm and 24 dBm ($P_{in,\,1\,\mathrm{dBcomp}} - 0.9$), respectively. Thus, using tow series diodes the remarkable sweet spot are moved toward PA saturation zone. For driving power range between 20 and 24 dBm, the $C/I3$ is higher than 39.5 dBc. At the input driving level corresponding to the maximum of power added efficiency, $C/I3$ is equal to 21 dBc. The obtained $C/I3$ performance of a 2nd HT PA design using single and

Table 3. $C/I3$ of 2nd HT PAs using gate bias composed by a single or two series diodes.

	P_{in} = 20.5 dBm	P_{in} = 22.5 dBm	P_{in} = 24 dBm
Without diodes (Figure 6)	35.18	28.81	18.52
With single diode	43	41	26.81
With 2 series diodes (Figure 7)	**43**	**50**	**54.3**
	$P_{in} = 24.9$ dBm 1 dB compression	P_{in} corresponding to $\mathrm{PAE_{max}}$: 26 dBm	-
Without diodes (Figure 6)	16.99	14.76	-
With single diode	21.22	17.47	-
With 2 series diodes (Figure 7)	**29.3**	**20.89**	-

2 series diodes, compared to the case where no diodes were used are summarised in Table 3, at input power marked by the appearance of sweet spots and for input powers corresponding to 1 dB compression and maximum PAE.

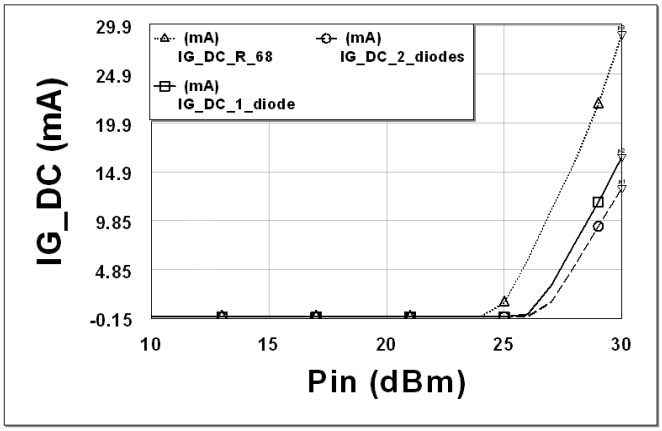


Figure 12. DC gate current evolution of 2HT PA with gate bias circuits composed by 2 series diodes, a single diode and without diodes vs. P_{in}.

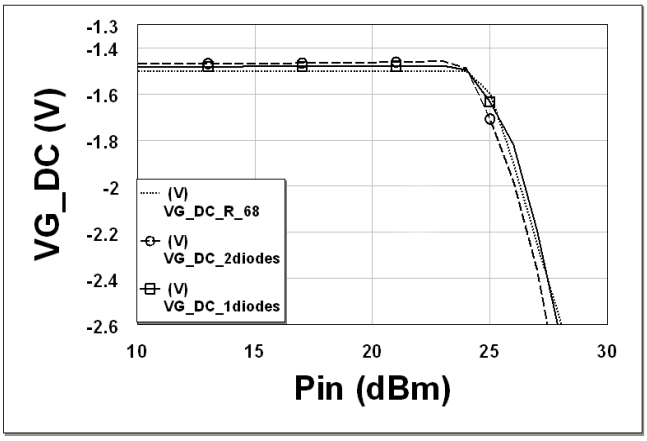


Figure 13. DC voltage evolution of 2HT PA with gate bias circuits composed by 2 series diodes, a single diode and without diodes vs. P_{in}.

In Figures 12 and 13, the simulated gate DC current and voltage of the 2nd HT PAs designed with gate bias composed by only resistor $Rg = 68\,\Omega$ and with gate bias circuit designed using the proposed approach to dynamically adjust V_{GS} by the introduction of a single and 2 series diodes, are presented as function of the input power. From Figure 12, the insertion of diodes in gate DC path assures a good current limitation compared to the case where only the resistor was used. Near saturation zone (from P_{in} of 22 dBm to P_{in} of 26 dBm) where the major linearity improvement is observed (Figure 11), it is clearly seen from Figure 12(a) current limitation using a couple of diodes ($P_{in} = 22\,\text{dBm}$, $IG = 4.2e - 6\,\text{mA}$) and ($P_{in} = 26\,\text{dBm}$, $IG = 0.03\,\text{mA}$), compared to the case where no diodes were used ($P_{in} = 22\,\text{dBm}$, $IG = 4.2e-6\,\text{mA}$) and ($P_{in} = 26\,\text{dBm}$, $IG = 5.8\,\text{mA}$).

To better understand the effect of the insertion of diodes in gate DC path on current limitation and thus linearity, a cascade of 3 and 4 diodes is used. The behaviour of $C/I3$ of 2HT designed using a couple of diodes, 3 and 4 diodes compared to the case where only a resistor was used for current limitation is given in Figure 15. The third order intermodulation output (IDS_2f2-f1) and the input DC (IG_DC) bias currents are presented in Figure 14. Observing Figures 14 and 15, we remark that the sweet spot marked by the point A ($P_{in} = 22.5\,\text{dBm}$) is obtained in three cases (using a couple or 3 or 4 diodes). The appear of this sweet spot is caused by the change of sign in the IMD3 current (interaction between small and large signal) observed using diodes, leading to IMD3 current equal to zero in this point (Figure 14). This

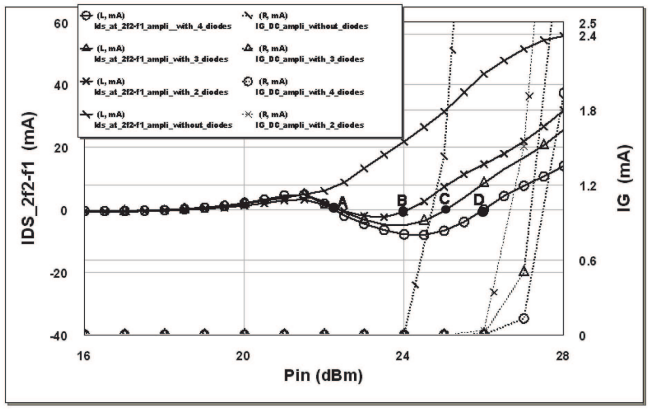


Figure 14. IMD current as long with DC gate current vs. P_{in}.

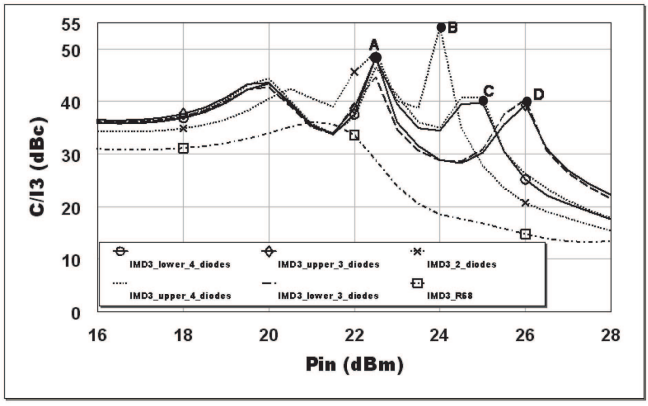


Figure 15. IMD3 of stabilised 2HT PAs with gate bias circuit composed by only a resistor and using a cascade of 2, 3 and 4 diodes.

change is not observed in the case where no diode is used. The IMD current change of sign (or phase change) results from the decrease of the gate DC current caused by the introduction of diodes for P_{in} equal or higher than 24 dBm. Using a couple of diodes, we remark the raise of other sweet spot in point B ($P_{in} = 24$ dBm) in Figure 15. This sweet spot can be moved toward higher input power by the addition of another diode. From Figure 15, we observe the appear of this sweet spot in point C ($P_{in} = 25$ dBm), by a further decrease in IG (DC) for P_{in} equal higher than that of point C (the point where IMD3 current is null is moved from point B to point C). Using an additional diode (a cascade of 4 diodes), sweet spot in point C can be further moved to point D ($P_{in} = 26$ dBm) due to a further decrease in Gate DC current in P_{in} equal or higher than P_{in} 25 dBm. To illustrate the gate DC current evolution, its values are given in Table 4 for input power corresponding to major change in IMd3 performances.

At 1 dB compression, power performances of 2HT amplifier using a cascade of 3 and 4 diodes are given in Table 5. compared to results of 2HT design using 2 diodes given in Table 2, from which it can be observed that the results are quite closes. Using same output network the evolution of drain average current a long with current fundamental component is plotted in Figure 16, where we can observe that in small signal there is no change, while a slight change is observed in large signal where the DC gate current is limited. After the insertion of each diode, average current decreases while current component at the

Table 4. Gate current DC evolution for 2HT design without diodes and after the insertion of 2, 3 and 4 diodes.

	P_{in} = 21 dBm	P_{in} = 22.5 dBm	P_{in} = 24 dBm
Without diode: (Figure 6)	6e-6	4.2e-6	3.9e-3
2 diodes (Figure 7)	5.7e-6	5.7e-6 **A**	4.2e-6 **B**
3 diodes	5.7e-6	5.7e-6	5.1
4 diodes	5.7e-6	5.7e-6	5.1
	P_{in} = 25 dBm	P_{in} = 26 dBm	P_{in} = 27 dBm
Without diode: (Figure 6)	1.42	5.832	10.96
2 diodes (Figure 7)	2.1e-4	0.003	1.5
3 diodes	6.6e-5 **C**	0.006	0.5
4 diodes	3.4e-5	0.001 **D**	0.13

Table 5. Simulated power performances of designed 2HT amplifiers with gate bias circuit composed by a single diode, 2 series diodes and without diodes.

	P_{in} (dBm)	P_{out} (dBm)	Gain (dB)	PAE (%)	$\text{PAE}_{\max}$ (%)
2HT PA (3 diodes)	24.55	37	12.5	49.5	51.4
2HT PA (4 diodes)	24.55	37	12.5	49.3	51.4

fundamental increases by roughly the same amount, that explain why power performances are unchanged after insertion of diode.

5. 2HT PA IMPLEMENTATION AND MEASUREMENT

The AWR layout shown in Figure 7 was used in the manufacturing process, where the 2nd HT amplifier was built on Rogers RT/DUROID 6010 board with a dielectric constant of 10.2. Figure 17 shows a photo of the implemented power amplifier.

Figures 18 and 19 show the measured power performances (gain, PAE and output power) at 2.5 GHz. Also shown on Figures 18 and 19 for comparison are the gain, PAE and output power predicted by the AWR harmonic-balance simulation, showing a good agreement.

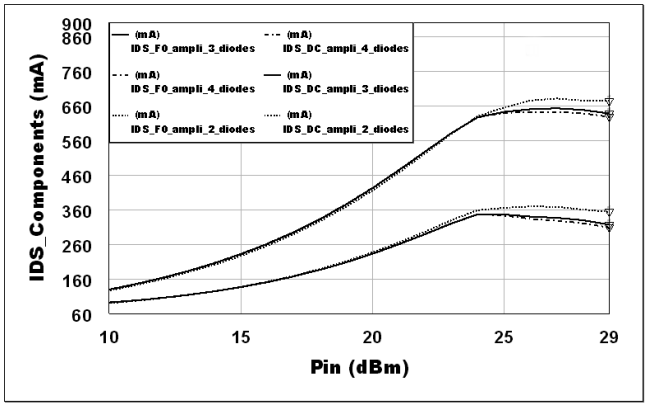


Figure 16. Current harmonic components for 2HT design using a couple of diodes and a cascade of 3 and 4 diodes.

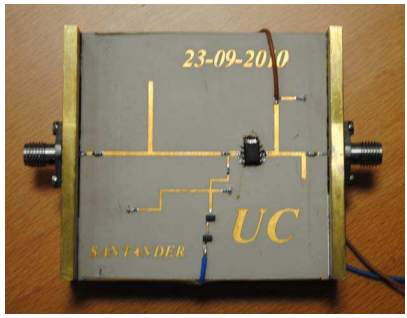


Figure 17. Photo of the implemented 2HT PA.

A linear maximum gain of 13.8 dB was measured, while a measured saturated power higher than 37 dBm is obtained. At 3 dB compression gain, a maximum power added efficiency of 53% is measured with an associated output power of 37.6 dBm. At 1 dB compression point, measured power performances, compared to simulated ones are summarized in Table 6.

In order to evaluate the linearity of implemented PA, two-tone excitations (tone centred at 2.5 GHz, with a frequency separation of 10 MHz) were applied at our PA input.

Figure 20 shows the measured $C/I3$ vs. P_{in}, compared to the simulated one. As seen from the data depicted in this figure, the

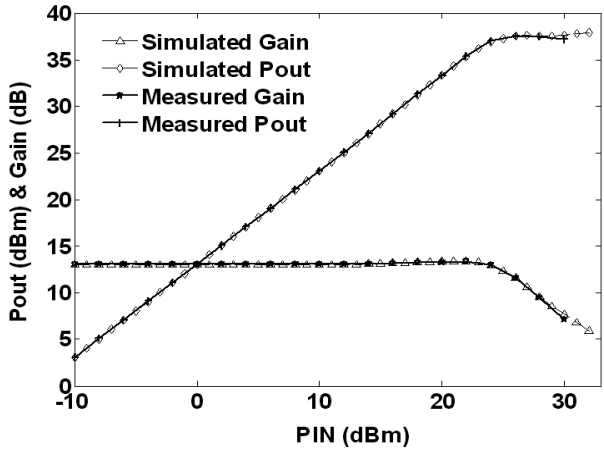


Figure 18. Measured and simulated output power vs. input power of 2nd HT amplifier.

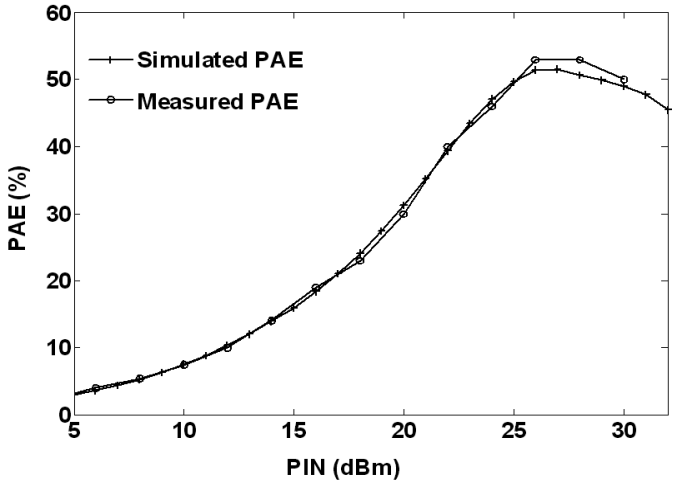


Figure 19. Measured and simulated PAE vs. input power of 2nd HT amplifier.

linearity improvement predicted by simulation using diodes, compared to the case where no diode was used, is confirmed by measured data (measured and simulated $C/I3$ data are quite close). At input power level of 24 dBm ($P_{1\,\mathrm{dBcomp}} - 0.9\,\mathrm{dBm}$), the measured $C/I3$ results in 53.4 dBc where its associated power performances are given in Table 7.

For all input power range lower than 24.5 dBm, a $C/I3$ higher than 34 dBc was measured, while it is higher than 40 dBc near saturation zone, i.e., for P_{in} range 20–24.5 dBm, where the associated power added efficiency and output power range from 30–46% and from 33.5–37.3 dBm, respectively.

Figure 21 shows the measured CW gain, output power and power added efficiency, compared to simulated results vs. the frequency band (2.3–2.7 GHz). At 1 dB compression, output power ranges from 35 to

Table 6. Performances of 2nd HT PA compared with simulated ones at 1db compression, $P_{in} = 24.9$ dBm.

	IMD3 (dBc)	Gain (dB)	Pout (dBm)	PAE (%)
Simulated data	29.3	12.38	37.28	49.3
Measured data	**28.5**	**12.4**	**37.4**	**50**

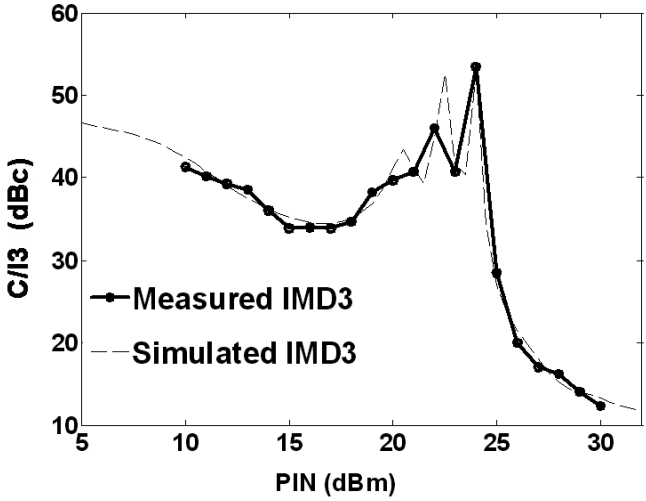


Figure 20. Measured and simulated PAE vs. input power of 2nd HT amplifier.

Table 7. Performances of 2nd HT PA compared with simulated ones at $P_{in} = 24$ dBm.

	IMD3 (dBc)	Gain (dB)	Pout (dBm)	PAE (%)
Simulated data	54.3	12.97	36.97	47.04
Measured data	**53.4**	**13**	**37**	**46**

36.9 dBm and a gain of 12.9 ± 0.9 dB is measured across the full 2.3–2.7 GHz band. Power added efficiency is typically 40–46% across this frequency range.

In Figure 22 are reported the simulated S-parameters of the 2nd

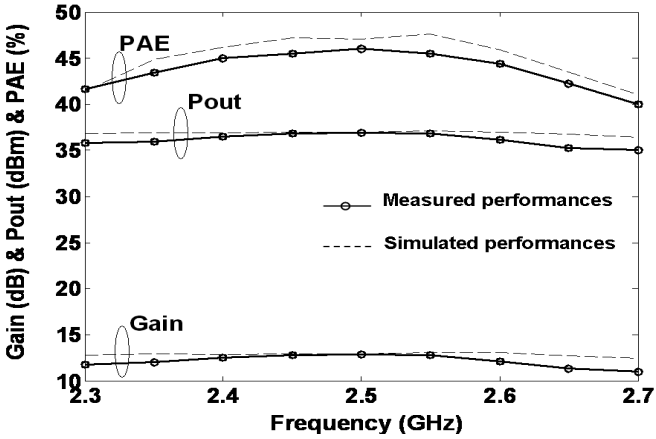


Figure 21. Measured and simulated PAE as well as gain and P_{out} vs. frequency of 2nd HT amplifier.

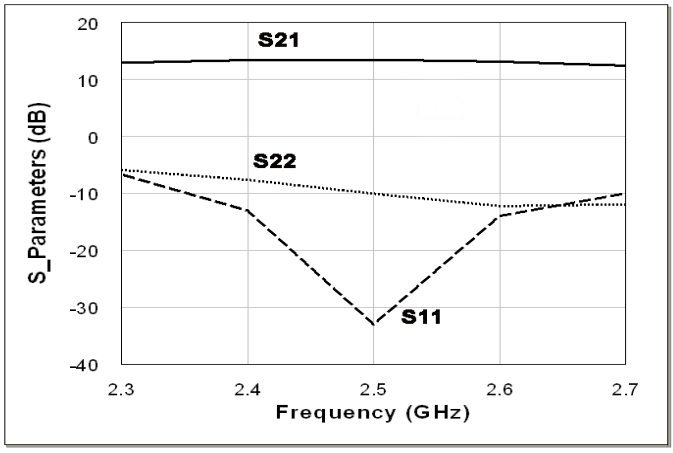


Figure 22. Simulated S-parameter 2nd HT PA with gate bias circuit composed by 2 series diodes.

HT PA, showing a large signal gain (S_{21}) of 12.92 ± 0.32 dB over WiMAX band of 2.3–2.7 GHz, and an input matching of 10 dB was obtained in a bandwidth of 330 MHz. An output matching of 10 dB is observed in a bandwidth of 200 MHz.

6. CONCLUSION

A high linearity RF power amplifier is reported in the AlGaN/GaN HEMT technology. The use of a pre-linearization diode in the gate DC path was shown to be useful in producing a wide sweet-spot in junction FET devices and in improving linearity, near saturation zone. This behaviour has been tested under two-tone excitation in TL and 2HT operating modes. The solution proposed by using diodes offers a good manner to improve linearity near PA saturation conditions, compared to the approach using only a DC gate resistor. A 2HT power amplifier circuit was built and measured data confirms the linearity improvement, as was predicted by simulation at 1 dB compression, maintaining higher power performances. An output power of 36.8 dBm has been measured with an associated power added efficiency of 46.5% and $C/I3$ of 53.4 dBc. A 2HT PA exhibits also good performances across the full 2.3–2.7 GHz band. An output power ranging from 35 to 36.9 dBm with an associated gain of 12.9 ± 0.9 dB and a power added efficiency ranging from 40 to 46% are measured across the full 2.3–2.7 GHz band.

ACKNOWLEDGMENT

Our acknowledgment to the financial support provided by the Spanish Ministry of Science and Innovation (MICINN) through projects TEC2008-06684-C03-01 and CONSOLIDER-INGENIO 2010 CSD2008-00068.

REFERENCES

1. Colantonio, P., F. Giannini, and E. Limiti, *High Efficiency RF and Microwave Solid State Power Amplifiers*, John Wiley & Sons, Inc., England, 2009.
2. Cripps, S. C., *RF Power Amplifiers for Wireless Communications*, 2nd Edition, Artech, Boston, MA, 2006.
3. Colantonio, P., F. Giannini, R. Giofrè, E. Limiti, A. Serino, M. Peroni, P. Romanini, and C. Proietti, "A C-band high efficiency second harmonic tuned hybrid power amplifier in

GaN technology," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 54, No. 6, Part 2, 2713–2722, Jun. 2006.

4. Wright, P., J. Lees, J. Benedikt, P. J. Tasker, and S. C. Cripps, "A methodology for realizing high efficiency class-J in a linear and broadband PA," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 57, No. 12, Part 2, 3196–3204, Dec. 2009.
5. Colantonio, P., F. Giannini, G. Leuzzi, and E. Limiti, "High-efficiency low-IM microwave PA design," *IEEE MTT-S Int. Microwave Symp. Dig.*, Vol. 1, 511–514, Phoenix, AZ, May 2001.
6. Colantonio, P., F. Giannini, G. Leuzzi, and E. Limiti, "Theoretical facet and experimental results of harmonic tuned PAs," *International Journal of RF and Microwave Computer-Aided Engineering*, Vol. 13, 459–472, 2003.
7. Colantonio, P., F. Giannini, G. Leuzzi, and E. Limiti, *Class G Approach for Low Voltage, High-efficiency PA Design*, 366–378, John Wiley & Sons, Inc., 2000.
8. Colantonio, P., F. Giannini, G. Leuzzi, and E. Limiti, "IMD performances of harmonic-tuned microwave power amplifiers," *Proc. European Gallium Arsenide Applications Symposium*, 132–135, Paris, France, Oct. 2000.
9. Moazzam, M. R. and C. S. Aitchison, "A low third order intermodulation amplifier with harmonic feedback circuitry," *IEEE MTT-S Int. Microwave Symp. Dig.*, 827–830, 1996.
10. Raab, F. H., P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Power amplifiers and transmitters for RF and microwave," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 50, 814–826, Mar. 2002.
11. Cripps, S., *Advanced Techniques in RF Power Amplifier Design*, Artech House, 2002.
12. Eun, C. and E. J. Powers, "A new Volterra predistorter based on the indirect learning architecture," *IEEE Trans. Signal Processing*, Vol. 45, 223–227, Jan. 1997.
13. Zhu, A. and T. J. Brazil, "An adaptive volterra predistorter for the linearization of RF high power amplifiers," *IEEE MTT-S*, 461–464, 2002.
14. Kim, J. and K. Konstantinou, "Digital predistortion of wideband signals based on power amplifier model with memory," *Electronics Letters*, Vol. 37, No. 23, 1417–1418, Nov. 8, 2001.
15. Nizamuddin, M. A., P. J. Balister, W. H. Tranter, and J. H. Reed, "Nonlinear tapped delay line digital predistorter for power amplifiers with memory," *IEEE Wireless Communications and*

Networking, Vol. 1, 607–611, Mar. 2003.

16. Carvalho, N. and J. Pedro, "Large and small signal IMD behavior of microwave power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 47, 2364–2374, Dec. 1999.
17. Pedro, J. and N. Carvalho, *Intermodulation Distortion in Microwave and Wireless Circuits*, Artech House, 2003.
18. Cabral, P. M., J. C. Pedro, and N. B. C. Carvalho, "A unified theory for nonlinear distortion characteristics in different amplifier technologies," *Microwave Journal*, Dec. 2004.
19. Gómez, C., J. A. García, and J. C. Pedro, "IMD sweet-spot control on junction FET devices using a gate bias resistor," *34th European Microwave Conf. Proceedings*, Amsterdam, 2004.
20. El Maazouzi, L., P. Colantonio, A. Mediavilla, and F. Giannini, "A highly efficient PA design for WiMAX applications: Theory and experiment," *International Journal of RF and Microwave Computer-Aided Engineering*, 2010.
21. Carvalho, N. B. and J. C. Pedro, "Large- and small-signal IMD behaviour of microwave power amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 47, No. 12, 2364–2374, Dec. 1999.
22. Chang, C.-P., W.-C. Chien, C.-C. Su, and Y.-H. Wang, "Linearity improvement of cascade CMOS LNA using diode connected NMOS transistor," *Progress In Electromagnetics Research C*, Vol. 17, 29–38, 2010.