Progress In Electromagnetics Research C, Vol. 22, 179–193, 2011

ANALYSIS OF ELECTRO STATIC DISCHARGE ON GAAS-BASED LOW NOISE AMPLIFIER

C.-H. Kim[1], S.-M. Hwang[1,*], and J.-H. Choi[2]

[1]Reliability Technology Research Center, Korea Electronics Technology Institute (KETI), Republic of Korea

[2]Department of Radio Engineering, Hanyang University, Republic of Korea

Abstract—This paper studies static effect of communication Low Noise Amplifier (LNA) that utilizes GaAs wafer. It analyzes the Electro-Static Discharge (ESD) effect, which occurs within communication components, such as GaAs LNA, and describes testing standard and methods. In order to find out GaAs LNA's susceptibility to static, two well-recognized communication GaAs LNA IC models were selected to be tested. Commercial program allowed measuring of static energy inserted within LNA's internal circuit by running a simulation about static discharge of GaAs LNA. Then we analyzed malfunctions caused by static and discussed about architectural problem and improvement according to the test and simulation result, from the perspective of GaAs LNA's electro static discharge.

1. INTRODUCTION

As a substitution for silicon semiconductor, Gallium Arsenide (GaAs) element is getting the spotlight today. GaAs is a compound of gallium and arsenic, which is efficient for high-frequency circuit by having faster operation speed and lower heat generation than silicon semiconductor [1]. ESD is a well-known reliability aspect in Si technologies, and it has been seriously addressed during last years in many research papers [2]. It is generally believed that GaAs circuits have a low susceptibility to ESD.

ESD is the most common cause of malfunction for low-powered components, such as large scale integration. Among semiconductor product failures, more than 50% of them are caused by ESD and

Received 27 April 2011, Accepted 24 June 2011, Scheduled 4 July 2011

* Corresponding author: Soon-Mi Hwang (asfara@keti.re.kr).

overvoltage. In the case of static discharge, electric charge transfer happens instantly and results in dielectric breakdown or metallization melt within semiconductor device from discharged voltage and induced current [3]. Figure 1 illustrates common failure of integrated circuit, and Table 1 shows ESD susceptibility of various electronic devices.

LNA is a component that amplifies the signal while lowering the noise figure of high-frequency signal so that it is widely used for telecommunication. The low-noise amplifiers that were selected as the subjects of the reliability assessment were chip-on-board products

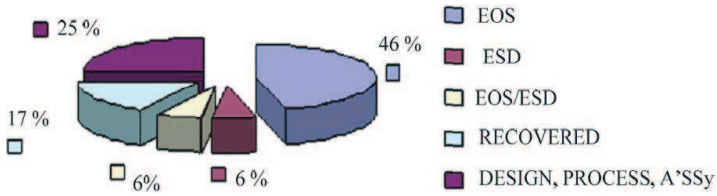


Figure 1. Common failure of integrated circuit [4, 5].

Table 1. ESD Susceptibility of electronic devices (to human body ESD) [6, 7].

Device Type	Range of ESD Susceptibility (V)
VMOS	30 ∼ 1800
MOSFET	100 ∼ 200
GaAsFET	100 ∼ 800
EPROM	100
JFET	140 ∼ 7000
SAW	150 ∼ 500
OP AMP	190 ∼ 2500
CMOS	250 ∼ 3000
Schottky diodes	300 ∼ 2500
Film resistors	300 ∼ 3000
Bipolar transistors	380 ∼ 7000
ECL	500 ∼ 1500
SCR	680 ∼ 2500
Schottky TTL	1100 ∼ 2500

that have gallium arsenide semiconductor (GaAs Phemt) on a ceramic substrate. High-frequency signal loss can be reduced by using an amplifier transistor in bare chip and directly mounting the components around the circuit connected with the bare chip transistor on a ceramic substrate. Moreover, thermal stability and reliability, the most vulnerable part of active modules, can be improved because bare transistor chip is 10 times better in thermal conductivity than existing plastic packaging type transistor and easier in heat sink dissipation to ceramic substrate.

Despite its features, weak resistance to ESD causes product malfunction and damage to the business. So high-frequency circuit concepts as LNA need specific requirements for possible HF ESD protection.

2. TEST STANDARD AND METHOD FOR ESD

2.1. Test Standard

An ESD event can be subdivided into HBM (Human Body Model), MM (Machine Model), and CDM (Charged Device Model). HBM resistance has been most widely used standard for ESD evaluation [8, 9]. Including human body, electrical equivalent circuit of discharge path has the form of double-exponential, and ESD waveform is determined by human body's charged capacitance and discharge resistance. Figure 2 illustrates HBM's equivalent circuit and waveform.

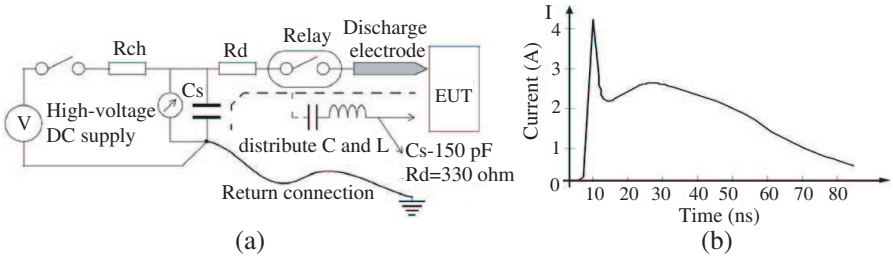


Figure 2. (a) HBM's equivalent circuit, (b) HBM's waveform.

As for HBM, the international test method standard for ESD can be categorized into Component and System. Component testing standard has MIL-Std 883 and EIA/JEDEC, while System testing standard includes IEC61000-4-2 and ANSI C.63-16. Table 2 shows the summary of current and proposed HBM ESD standards.

Table 2. Summary of current and proposed HBM ESD standards.

Category		Max. Voltage (Pol. +/-)	Discharge Network
For Component	MIL-Std 883	2 kV ~ 8 kV	100 pF/1500 Ω
	EIA/JEDEC Test Method 5.1	0 ~ 8 kV	100 pF/1500 Ω
For System	IEC61000-4-2 (former IEC801-2)	0 ~ 8 kV (Contact) 0 ~ 15 kV(Air)	150 pF/330 Ω
	ANSI C.63-16	0 ~ 8 kV (Contact) 0 ~ 15 kV(Air)	150 pF/330 Ω

2.2. Test Method

There are two discharge methods for ESD simulator, air discharge mode and contact discharge mode. In air discharge mode, a spark is formed between the tip and ground [10]. Most of the responses from linear simulator and non-linear arcs determine discharge current. In this case, the simulator current can be modeled using the impedance as seen from ground plane into the discharge tip. This impedance can be trans-formed in the time domain and convoluted with the non-linear arc [11, 12]. This yields the discharge current. Fully modeling the arc via differential equations in a time stepping algorithm is principle possible, but require additional measures to avoid divergence, as the ionization equations are highly sensitive to errors in the electric field across the gap [13, 14].

Most ESD testing is done in contact mode. As the discharge is initiated by a relay and as the impedances as seen from the relay contacts are neither known, nor easy to measure, a different simulation approach needs to be used.

It is not a straightforward task to simulate contact mode discharge, although the system can be regarded as linear (provided the relay switched more or less like ideal switch). In contact mode a capacitor and some elements of the simulator are pre-charged. To initiate the discharge a relay is closed.

In this paper, we carried out a ESD experiment according to IEC61000-4-2 standard, in contact mode.

Figure 3. Testing figure.

Table 3. Test condition.

Test Standard	Test Condition	
IEC61000-4-2	Discharge	330 Ω, 150 pF
	Test Mode	Contact Discharge
	Test Voltage	From 1 kV to 4 kV, 1 kV step
	Test Polarity	Positive and Negative
	Test Interval	Over 1 sec.
	Number of Sample	5 ea/test level

Table 4. Test result.

Test Result / Test Voltage		A type		B type	
		Number of Sample	Number of Failure	Number of Sample	Number of Failure
ESD Test Voltage	1 kV	5	0	5	0
	2 kV	5	5	5	0
	3 kV	5	5	5	5
	4 kV	5	5	5	5

3. TEST RESULT OF ESD

3.1. Test Result

ESD test was done on two communication GaAs LNA IC models according to IEC 61000-4-2 standard, in contact mode. Testing equipment was Mini Zap (MZ-15) of Key-Tek. Table 3 shows test condition and Figure 3 illustrates the testing figure.

The measurement items are S_{11} (Input Return Loss), S_{22} (Output Return Loss), S_{21} (Gain), Noise figure, IIP3 (Third-order intercept point) and Power consumption. As a result, the failure of sample A was reported at 2 kV, and failure of sample B was reported at 3 kV.

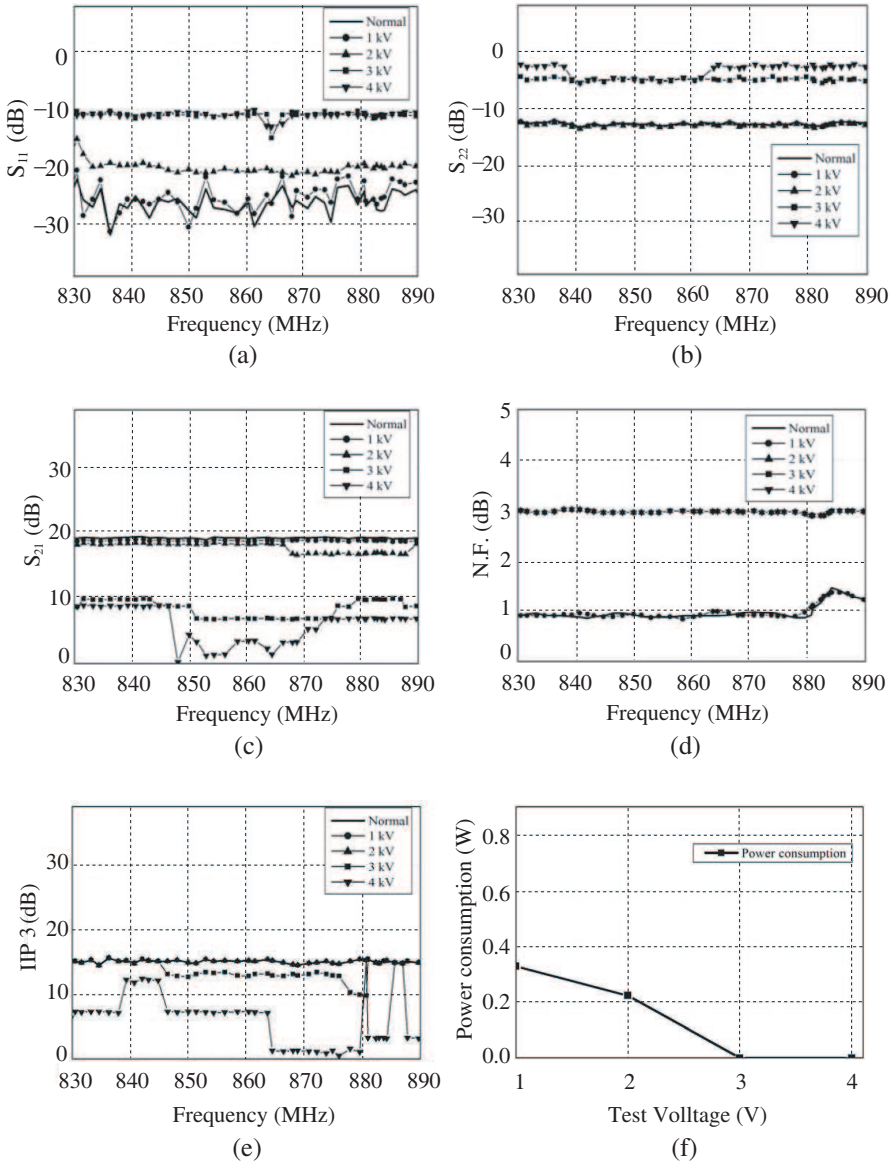


Figure 4. Measurement performance of Sample A according to different applied voltage. (a) S_{11}, (b) S_{22}, (c) S_{21}, (d) noise figure, (e) IIP3, (f) power consumption.

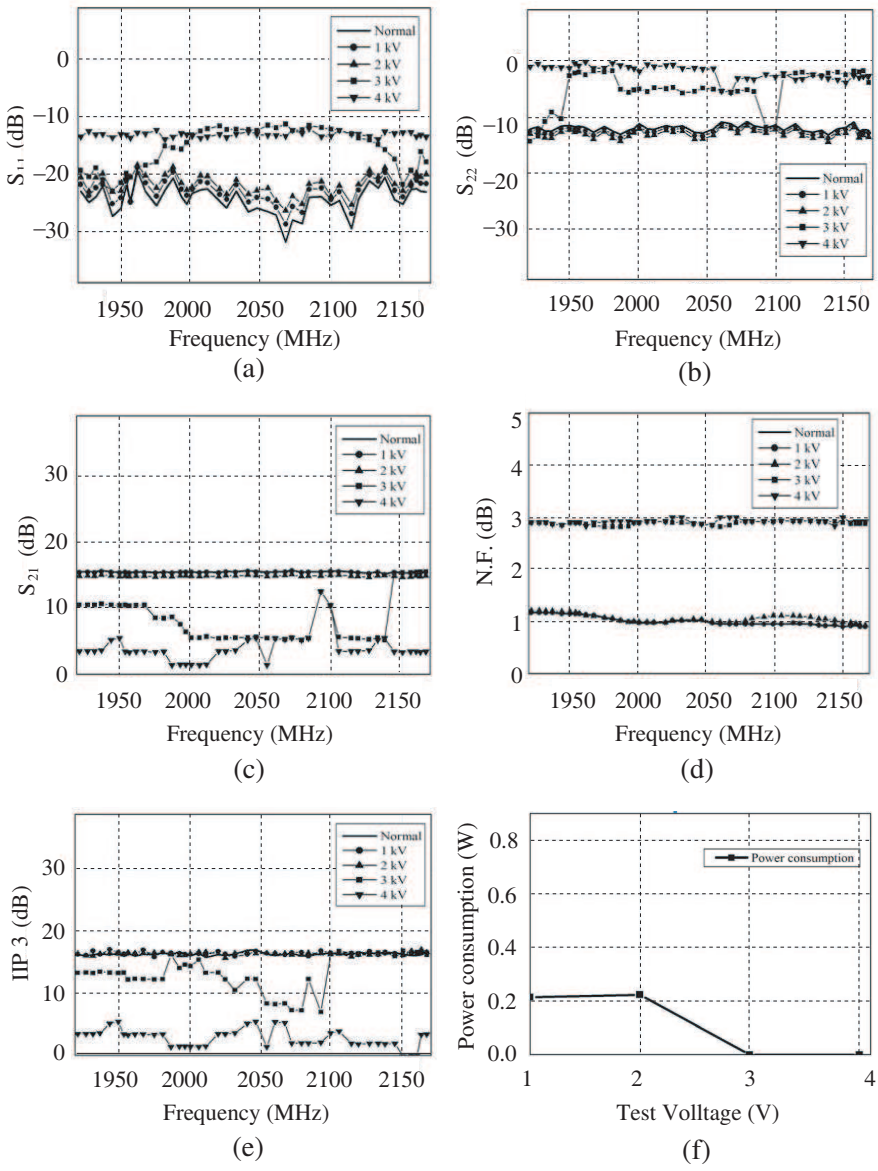
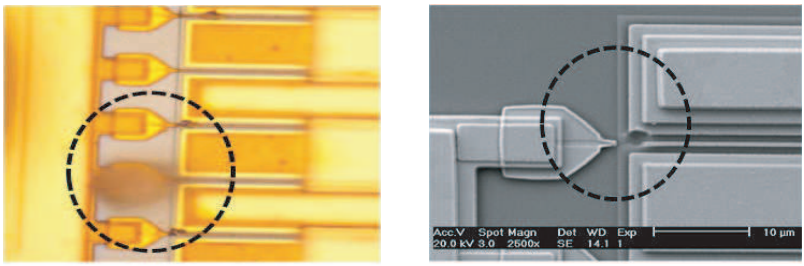
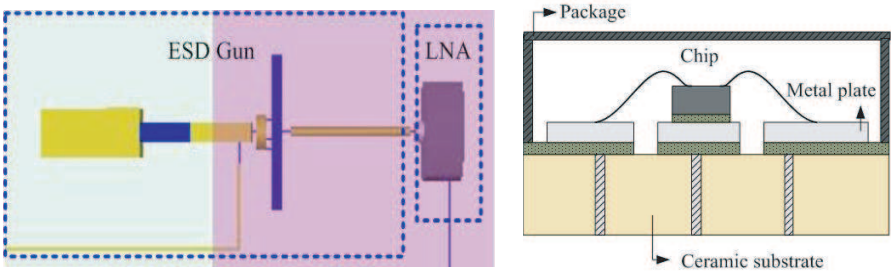


Figure 5. Measurement performance of Sample B according to different applied voltage. (a) S_{11}, (b) S_{22}, (c) S_{21}, (d) noise figure, (e) IIP3, (f) power consumption.



(a) (b)

Figure 6. ESD induced failure (at 4 kV HBM ESD impulse). (a) Metallization burn-out, (b) line open.



(a) (b)

Figure 7. Modeling of GaAs LNA. (a) FLO/EMC model, (b) consisting of LNA.

Table 4 shows the test result, and Figures 4 and 5 show measurement performance of Samples A, B according to different applied voltages.

3.2. Failure Analysis

After the ESD test, the failed samples were carefully examined with optical microscope and Environmental Scanning Electron Microscope (ESEM), for further analysis. From the analysis, either broken wire or burning trace could be observed in each sample. Figure 6 illustrates ESD induced failure at 4 kV HBM ESD impulse.

4. SIMULATION OF ESD

4.1. Numerical Modeling

For further analysis on ESD test result of GaAs LNA, a numerical modeling was implemented, using a commercial program,

FLO/EMC6.1 (Flomerics, Co., Ltd.) FLO/EMC's basic modeling approach is like the following [15, 16].

- Construct EMC model.
- Construct a Maxwell equation about the model and interpret 3D vector field using TLM (Transmission-Line Matrix) method.
- Find a value from time-domain.
- Calculates vector field and magnetic field.

Figure 7 illustrates FLO/EMC model of GaAs LNA. The model has two parts; ESD Generator and LNA device. LNA device consists of ceramic substrate, metal plate, and package part.

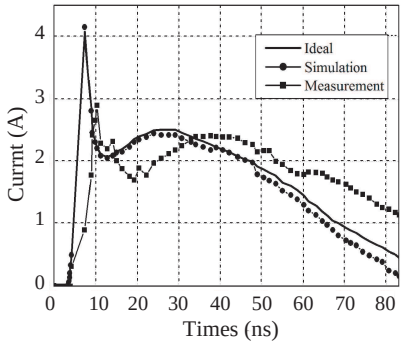


Figure 8. Input waveform of ESD (at 4 kV ESD impulse, defined in IEC61000-4-2).

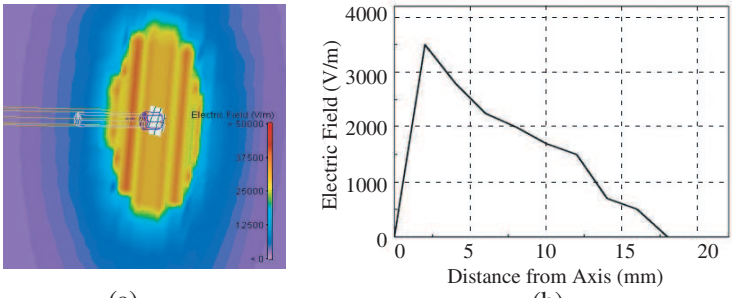


Figure 9. Analysis of electric field distribution (at 4 kV ESD impulse). (a) Electric field distribution, (b) electric field strength.

4.2. Simulation Result

Figure 8 illustrates and compares among input waveform of contact discharge 4 kV, defined in IEC61000-4-2, the actual waveform measured from GaAs LNA static discharge experiment, and input waveform from static discharge test modeling. The waveform from the actual experiment and the model are almost identical to the standard waveform. Figure 8 compares the accuracy of electro static wave which would be entered on testing sample. (This wave is not the one that passes through LNA). Simulated wave has a similar overall shape to that of the ideal wave but yet, not identical. Every time when a measurement is taken, there exists a slight difference. It seems to be a human or measurement error.

Simulation result suggests that LNA input circuit's energy rises as applied static level increases. Figure 9 illustrates analysis of electric field distribution, which occurred within LNA's circuit during the static discharge experiment. When 4 kV ESD was applied, maximum of 36,000 V/m electric field was distributed throughout the entire circuit.

5. ESD SOLUTION FOR GAAS LNA

LNA failure caused by ESD show disconnection or burning in LNA module's input/output port. This might occur during production or transportation process when a worker's accumulated static instantly flows into the product.

It happens more frequently for GaAs wafer than silicon wafer because GaAs is weak at statics. The best solution would be to increase its resistance to static, however, its physical property make it difficult. Hence this thesis took the next best solution to improve the circuit.

To solve a case where ESD current harms the circuit through

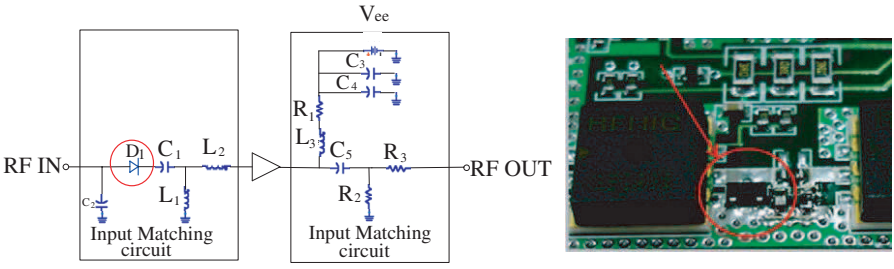


Figure 10. LNA with protective diode. (a) Matching circuit, (b) LNA.

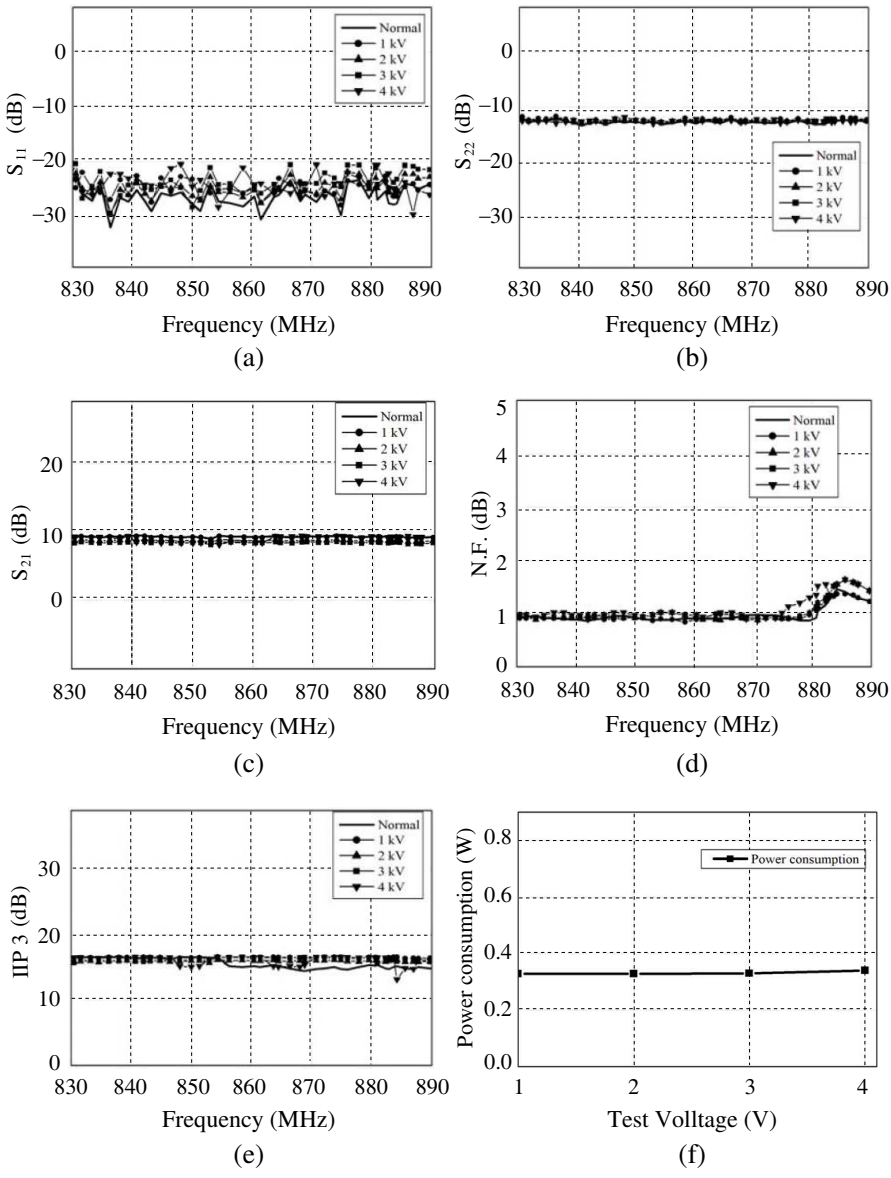


Figure 11. Measurement performance of improved Sample A according to different applied voltage. (a) S_{11}, (b) S_{22}, (c) S_{21}, (d) noise figure, (e) IIP3, (f) power consumption.

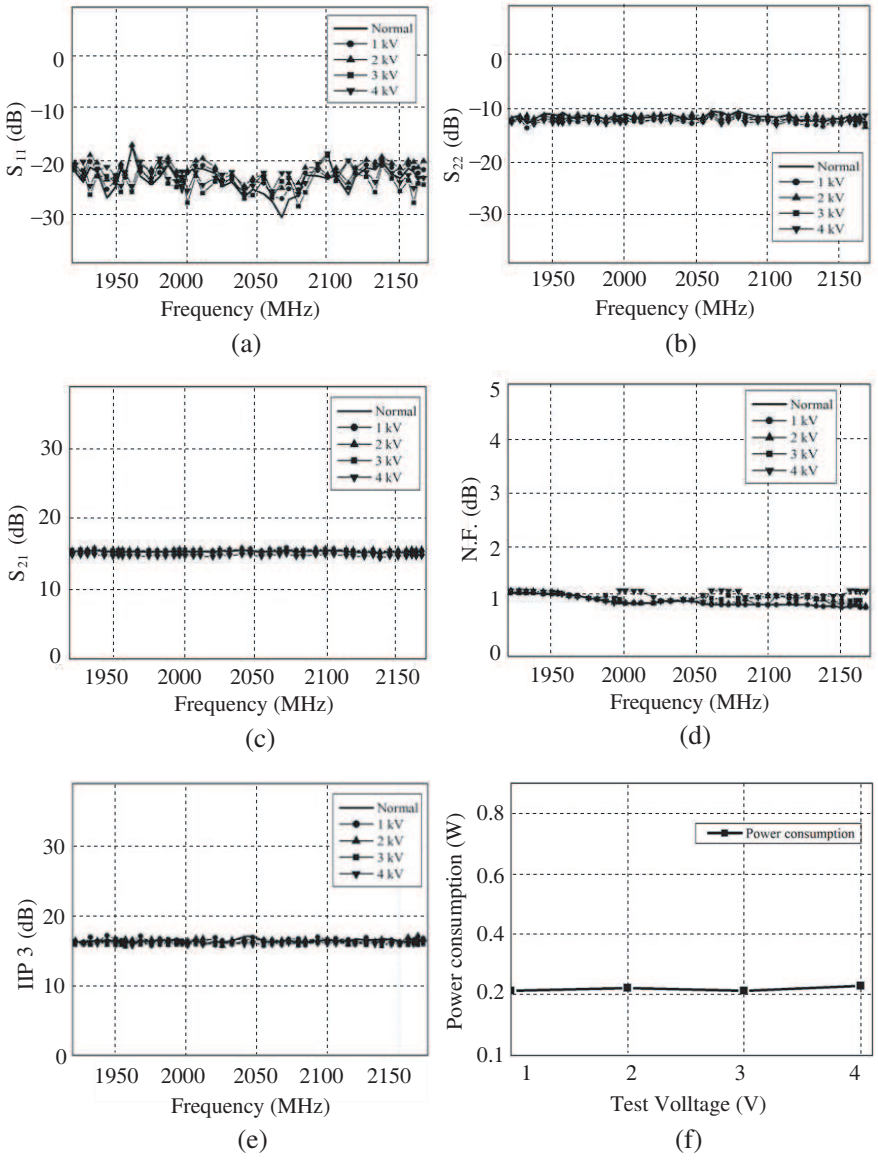
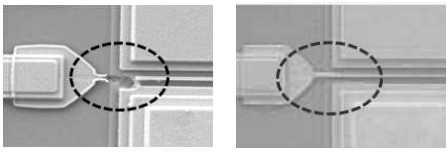


Figure 12. Measurement performance of improved Sample B according to different applied voltage. (a) S_{11}, (b) S_{22}, (c) S_{21}, (d) noise figure, (e) IIP3, (f) power consumption.



(a) (b)

Figure 13. Analysis of LNA (at 4 kV HBM ESD impulse). (a) Before improved circuit, (b) after improved internal circuit.

Table 5. ESD test result of the improved circuit.

Test Result / Test Voltage		A typle		B typle	
		Number of Sample	Number of Failure	Number of Sample	Number of Failure
ESD Test Voltage	1 kV	5	0	5	0
	2 kV	5	0	5	0
	3 kV	5	0	5	0
	4 kV	5	0	5	0

directly connected path inside a product, blocking and diverting will be the answer. Blocking increases impedance of ESD-induced noise current path, and Diverting changes current's path so that noise current would not pass internal circuit. Considering the size, blocking method shall be more appropriate for a product like LNA.

In this paper, we constructed a circuit with ideal protective diode, selected from series of tests. By inserting diode to the input, the input circuit's impedance has increased, and such increase could block the sudden flow of excess current induced by static. Figure 10 illustrates LNA and matching circuit in LNA with protective diode.

The identical ESD test was carried out, following IEC61000-4-2 standard, after the circuit improvement installed. As a result, both samples A and B showed resistance to at least 4 kV or more. Table 5 shows ESD test result of the improved circuit, and Figures 11 and 12 show each sample's new measurement property for different applied voltages. Figure 13 shows analysis of LNA's improved internal circuit, observed by ESEM.

6. CONCLUSION

This paper researches on the static effect of communication low-noise amplifier that utilizes GaAs wafer. It describes the effect of static on low powered circuit, such as GaAs LNA, and widely used static

test standard and method, which it implemented to carry out an experiment on GaAs LNA's resistance to statics.

ESD test was done on two communication GaAs LNA IC models, and the result showed that they both had weak resistance to ESD: less than 2 kV for sample A and less than 3 kV for sample B.

We simulated electro static discharge of GaAs LNA, using commercial software in order to confirm the amount of static energy flown into LNA's internal circuit. Analysis on failure of samples revealed LNA module's input/output port had disconnection or burning problem.

As a countermeasure, appropriate protective diode was installed on GaAs LNA's internal circuit, and the improved circuit was proved to be resistant to more than 4 kV.

REFERENCES

1. Bock, K., "ESD issues in compound semiconductor high-frequency devices and circuits," *Electrostatic Discharge Symposium*, 1–12, Sep. 23–25, 1997.
2. Howes, M. J. and D. V. Morgan, *Reliability and Degradation*, Wiley, New York, 1981.
3. Vinson, J. E. and J. J. Liou, "Electrostatic discharge in semiconductor devices," *Proc. of the IEEE*, Vol. 86, 399–420, 1998.
4. Green, T., "A review of EOS/ESD field failure in military equipment," *Proc. 10th EOS/ESD Symposium*, 1998.
5. Wunsch, D. C. and R. R. Bell, "Determination of threshold failure levels of semiconductor diodes and transistors due to pulse voltages," *Nuclear and Plasma Sciences Society*, Vol. 15, 244, Nov. 1968.
6. Schreier, L. A., "Electrostatic damage susceptibility of semiconductor devices," *Reliability Physics Symposium*, 151, Apr. 1978.
7. Lacrampe, N., F. Caignet, M. Bafleur, N. Nolhier, and N. Mauran, "Characterization and modeling methodology for IC's ESD susceptibility at system level using VF-TLP tester," *29th Electrical Overstress/Electrostatic Discharge Symposium*, 1, Sep. 16–21, 2007.
8. Amerasekera, A., W. Abeelen, L. Roozendaal, M. Hannemann, and P. Schofield, "ESD failure modes: characteristics mechanisms, and process influences," *IEEE Transactions on Electron Devices*, Vol. 39, 430–436, Feb. 1992.
9. Polgreen, T. L. and A. Chatterjee, "Improving the ESD failure threshold of silicided n-MOS output transistors by ensuring

uniform current flow," *IEEE Transactions on Electron Devices*, Vol. 39, 379, Feb. 1992.

10. Soohoo, K. M. and C.-Y. Wu, "On component level ESD testing," *Industry Applications Society Annual Meeting IEEE Conference*, 872, Oct. 7–12, 1990.
11. MaCleod, L. M. and K. G. Balmain, "Compact traveling-wave physical simulator for human ESD," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 39, 89, May 1997.
12. Zaridze, R., D. Karkashadze, R. G. Djobava, D. Pommerenke, and M. Aidam, "Numerical calculation and measurement of transient fields from electrostatic discharges," *IEEE Transactions on Components, Packaging, and Manufacturing Technology*, Vol. 19, 178, Jul. 1996.
13. Jobava, R., D. Pommerenke, D. Karkashadze, P. Shubitidze, R. Zaridze, S. Frei, and M. Aidam, "Computer simulation of ESD from voluminous objects compared to transient fields of humans," *IEEE Transactions on Electromagnetic Compatibility*, Vol. 42, 54, Feb. 2000.
14. Giannetti, R. and B. Tellini, "Equivalent network modeling to simulate electrical discharges," *IEEE Transactions on Magnetics*, Vol. 36, 971, Jul. 2000.
15. Caniggia, S., "Circuit and numerical modeling of electrostatic discharge generators," *IEEE Trans. on Industry Applications*, Vol. 42, 1350–1357, 2006.
16. Smedt, R. D., K. Vervoort, E. V. Oerle, and D. V. Troyen, "Effect of a board on the shielding effectiveness of a box," *EMC Europe International Symposium on EMC*, 413–418, 2002.