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A HIGH-GAIN CMOS LNA FOR 2.4/5.2-GHZ WLAN APPLICATIONS

S. Wang and B.-Z. Huang

Graduate Institute of Computer and Communication Engineering
National Taipei University of Technology
1, Sec. 3, Chung-Hsiao E. Road, Taipei 10608, Taiwan, R.O.C.

Abstract—This paper describes a high-gain CMOS low-noise amplifier (LNA) for 2.4/5.2-GHz WLAN applications. The cascode LNA uses an inductor at the common-gate transistor to increase its transconductance equivalently, and therefore it enhances the gain effectively with no additional power consumption. The LNA is matched concurrently at the two frequency bands, and the input/output matching networks are designed with two notch frequencies to shape the frequency response. The dual-band LNA with the common-gate inductor is designed, implemented, and verified in a standard 0.18-μm CMOS process. The fabricated LNA which consumes 7.2 mW features gains of 14.2 dB and 14.6 dB, and noise figures of 4.4 dB and 3.7 dB at the 2.4-GHz and 5.2-GHz frequency bands, respectively. The proposed LNA demonstrates a 4.9–7.8 dB gain enhancement compared to conventional cascode LNAs, and the chip size is 1.06 mm × 0.79 mm including all testing pads.

1. INTRODUCTION

Recently, dual-band and multi-band transceivers draw much attention for the versatile functionality of such communication systems [1–4]. Conventional dual-band transceivers are implemented by switching two separate receiver chains [5–7]. The switched receivers cannot operate simultaneously, and the implementation of the switching system increases the circuit complexity, power dissipation, and chip size. Although efforts have been made to realize a compact and switchable dual-band LNA for alleviating the large chip area of the RF

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Corresponding author: Sen Wang (wangsen@ntut.edu.tw).

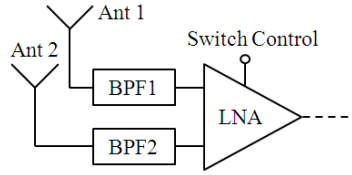

Figure 1. A dual-band receiver with a switchable LNA.

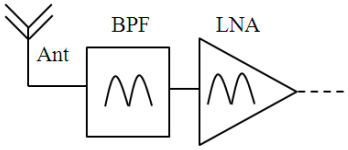

Figure 2. A dual-band receiver with a concurrent LNA.

front-ends [8, 9], it is difficult to achieve reconfigurable antennas and BPFs or to reduce the number of these single-band circuits as shown in Fig. 1. Moreover, these LNAs for dual-band are implemented by RF switches, switched capacitors or switched inductors [9–11]. However, the additional elements contribute more noise and degrade the gain of the amplifiers.

Compared to the switchable LNA, a concurrent LNA facilitates the integration and simplifies the architecture of the RF front-ends due to the feasible dual-band antennas and BPFs [12–14] as shown in Fig. 2. The concurrent receiver enables simultaneous dual-band operations in the same circuitry, and therefore it presents lower power consumption and reduced chip area. Typically, gains of concurrent LNAs are also degraded by the more of low-Q CMOS inductors in the matching networks [15], and therefore the LNAs are based on cascode topology at microwave or millimetre-wave frequencies for high-gain considerations [16–20]. In this paper, a high-gain, low-power, and concurrent CMOS LNA based on cascode topology is designed for 2.4/5.2-GHz WLAN applications. The high-gain LNA with acceptable noise figure utilizes a common-gate inductor. The design method is detailed in the following sections. Section 2 describes the gain enhancement resulted from a common-gate inductor, the frequency response shaped by the input/output matching networks, and the tradeoff considerations of the LNA. Moreover, the fabrication and experimental results of the LNA in a 0.18-μm CMOS process are also reported in Section 3. Finally, Section 4 concludes this work.

2. CIRCUIT DESIGN

2.1. Gain-enhanced LNA with the Common-gate Inductor

Figure 3 shows the complete schematic of the proposed dual-band LNA for 2.4/5.2-GHz WLAN applications. The intrinsic transconductance of the transistor is inherently wideband. Thus the LNA can be designed at dual-band frequencies simultaneously with appropriate matching networks including bandpass and bandstop networks to shape the

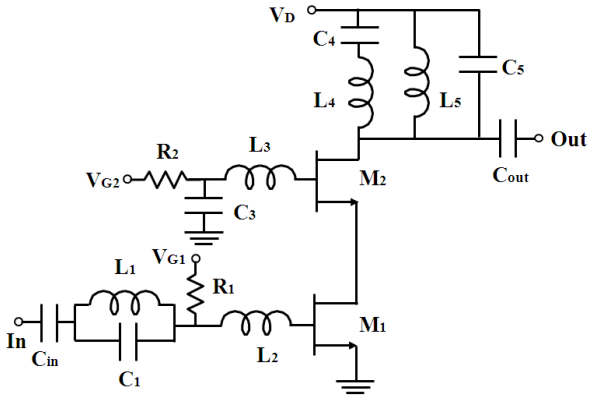

Figure 3. Schematic of the proposed dual-band LNA for WLAN applications.

frequency response. The cascode configuration features high gain and good reverse isolation performances due to the combination of common-source and common-gate stages. Each gate is biased through a 5-kΩ resistor (R_1 and R_2), and bypass capacitors are added to stabilize the supply voltage and to isolate the supply noise. L_3 and C_3 at the gate of the transistor M_2 are designed for gain enhancement and AC ground, respectively. Other LC components are for dual-band matching network, and will be discussed later. No inductive source degeneration is added to common-source stage because it will degrade the gain of the LNA, especially the gain at 5.2 GHz. However, the absence of the inductive degeneration results in inferior noise figure and linearity distortion.

To investigate the gain enhancement of the amplifier, an equivalent circuit of the common-gate transistor with L_3 is illustrated in Fig. 4. Based on the small-signal analysis and neglecting the gate-to-drain capacitance C_{gd2}, the V_{gs2} and can be expressed as

$$V_{gs2} = \frac{-\left(\frac{1}{j\omega C_{gs2}}\right) V_{\mathrm{in}}}{\frac{1}{j\omega C_{gs2}} + j\omega L_3} = \frac{-V_{\mathrm{in}}}{1 - \omega^2 L_3 C_{gs2}} \tag{1}$$

where ω and C_{gs2} are the operating frequency and gate-to-source capacitance of M_2, respectively. According to Eq. (1), the amplitude of V_{gs2} is increased if $|1 - \omega^2 L_3 C_{\mathrm{gs2}}| < 1$. Consequently, the transconductance (g_{m2}) is enhanced equivalently and the gain of the amplifier is boosted effectively [21]. However the gain enhancement is limited by the value of L_3, or the inequality mentioned above. The large L_3 will results in circuit instability with a negative resistance in the common-gate stage. The reason can be explained by deriving

the input current (I_{in}) and then the input impedance (Z_{in}) in Fig. 4. As expressed in Eq. (3), the presence of large L_3 leads to a negative resistance in Z_{in}.

The design procedure of the gain-enhanced LNA is summarized as follows. Firstly the aspect ratios of cascode transistors M_1 and M_2 are chosen to obtain the maximum small signal gain of the LNA, and the LNA is under class-A bias condition to achieve good linearity. Once the bias condition and the aspect ratio of M_2 are decided, the C_{gs2} is also determined. Secondly, a large value of L_3 has to be chosen properly which also meets the inequality such that the LNA is still operated at stable regions. Moreover, large values of C_3 and bias resistors are required for achieving good AC ground. Finally, the input/output matching networks to shape the frequency responses of the LNA are designed.

$$I_{\text{in}} = \frac{V_{\text{in}}}{\frac{1}{j\omega C_{gs2}} + j\omega L_3} + \frac{g_{m2}\left(\frac{1}{j\omega C_{gs2}}\right) V_{\text{in}}}{\frac{1}{j\omega C_{gs2}} + j\omega L_3} \tag{2}$$

$$Z_{\text{in}} = \frac{V_{\text{in}}}{I_{\text{in}}} = \frac{1}{g_{m2} + j\omega C_{gs2}} \cdot \left(1 - \omega^2 L_3 C_{gs2}\right). \tag{3}$$

2.2. Matching Networks

The concurrent dual-band LNA is realized by the input and output matching networks without any switching operations. Fig. 5 depicts the frequency response ($|S_{21}|$) of the LNA which is determined by the bandpass and bandstop networks. The operating frequencies of the dual-band LNA are ω_1 and ω_2. The two notch frequencies (ω_3 and ω_4) are realized by the notch filters of input and output matching networks, respectively, as shown in Fig. 5. In the input matching network, the relation between the notch frequency (ω_3) and the resonator (L_1 and

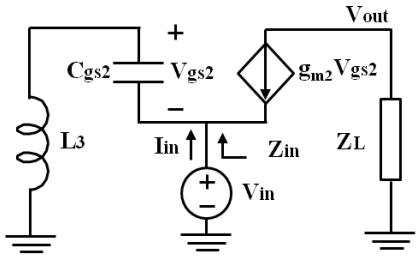

Figure 4. Small-signal equivalent model of the common-gate transistor with L_3.

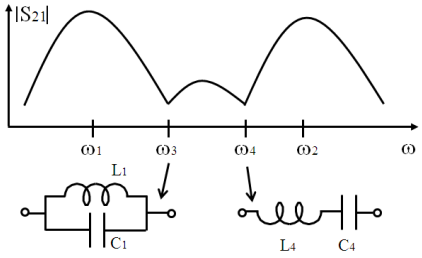

Figure 5. Frequency response ($|S_{21}|$) of the dual-band LNA.

C_1) can be expressed as

$$L_1 C_1 = \frac{1}{\omega_3^2}. \tag{4}$$

The input matching network is realized by the resonator, L_2 and the transconductance ($C_{\rm gs1}$) of M_1. At ω_1, the resonator and the series network of L_2 and $C_{\rm gs1}$ are inductive and capacitive, respectively. On the contrary, the resonator and the series network at ω_2 are capacitive and inductive, respectively. Therefore the imaginary part of the input impedance is cancelled, and then the dual-band operation at ω_1 and ω_2 of the input matching network is achieved concurrently. As discussed before, the design equations of input matching network can be expressed as Eq. (5) and Eq. (6). The design procedure is that the aspect ratio of M_1 is first chosen for high-gain and low-power considerations, and then the $C_{\rm gs1}$ is also decided. Once the $C_{\rm gs1}$ is decided, the L_1, L_2, and C_1 can be obtained from Eq. (4) to Eq. (6).

$$\frac{\omega_3^2 L_1}{\omega_3^2 - \omega_1^2} = \frac{1}{\omega_1^2 C_{gs1}} - L_2 \tag{5}$$

and

$$\frac{\omega_3^2 L_1}{\omega_2^2 - \omega_3^2} = L_2 - \frac{1}{\omega_2^2 C_{gs1}}. \tag{6}$$

In the output matching network, the relation between the notch frequency (ω_4) and the resonator (L_4 and C_4) can be expressed as

$$L_4 C_4 = \frac{1}{\omega_4^2}. \tag{7}$$

The output matching network is realized by the resonator, L_5 and C_5 as shown in Fig. 3. The L_4C_4 resonator is capacitive ($C_{\rm p}$) at ω_1, and is inductive ($L_{\rm p}$) at ω_2. Therefore the output matching network can be achieved concurrently at the two frequencies by the following equations as shown in Eq. (8) and Eq. (9). A similar analysis can be carried out to choose the values of the output LC elements. Firstly, practical values of L_4 and C_4 on a CMOS process are decided by a fixed notch frequency, and then L_5 and C_5 can be also obtained by Eq. (8) and Eq. (9).

$$L_5(C_5 + C_p) = \frac{1}{\omega_1^2} \tag{8}$$

$$\left(\frac{L_5 L_p}{L_5 + L_p}\right) C_5 = \frac{1}{\omega_2^2} \tag{9}$$

where $C_p = \frac{\omega_4^2 C_4}{\omega_4^2 - \omega_1^2}$ and $L_p = \frac{\omega_2^2 - \omega_4^2}{\omega_4^2 \omega_2^2 C_4}$.

Although the analysis of the matching networks discussed above neglects the effect of input and output capacitance (C_{in} and C_{out} are bypass capacitors), and parasitic capacitances of the cascode transistors, the simplified analysis still provides a useful and quick assessment. Therefore the calculated values of the elements from Eq. (4) to Eq. (9) must be optimized for a practical design.

2.3. Noise and Nonlinearity Analysis

In this section, the impact on the noise and nonlinearity of the high-gain LNA will be discussed. Fig. 6 shows the noise model of the LNA with L_3 at the common-gate stage. Assuming that the input and output port is matched to $50\,\Omega$, and the model is available for the dual-band operation. The noise current of each transistor is included in Fig. 6. Firstly, the voltage gain of the model is given by

$$A_v = \frac{R_L}{Rs} \cdot \frac{\omega_T}{\omega_o} \cdot \frac{1}{1 + \frac{1}{g_{m2}(\frac{1}{j\omega C_{gs2}} + j\omega L_3)}}, \tag{10}$$

where $\omega_T = \frac{g_{m1}}{C_{gs1}}$ and $\omega_o = \frac{1}{\sqrt{L_2 C_{gs1}}}$. Then the noise factor (NF) derived from the voltage gain can be also expressed as

$$\text{NF}=1 + \gamma_1 g_{d1} R_s \left(\frac{\omega_o}{\omega_T}\right)^2 \left(1 + \frac{\gamma_2 g_{d2}}{\gamma_1 g_{d1}} \times \left(1 + \frac{\omega_T L_3}{R_s}\right)^2 \left(\frac{\omega_o C_{gs2}}{g_{m2}}\right)^2\right) \tag{11}$$

where γ is the coefficients to be equal to 2/3 for long-channel transistors, and may need to be replaced by a larger value for submicron transistors [22]. And g_{d} is the drain-source channel conductance in triode regions. As shown in Eq. (10), the presence of L_3 enhances the voltage gain of the amplifier. Due to the degradation of ω_{T}, the voltage gain decreases at high frequencies. The absence of inductive source degeneration results in higher noise figure compared

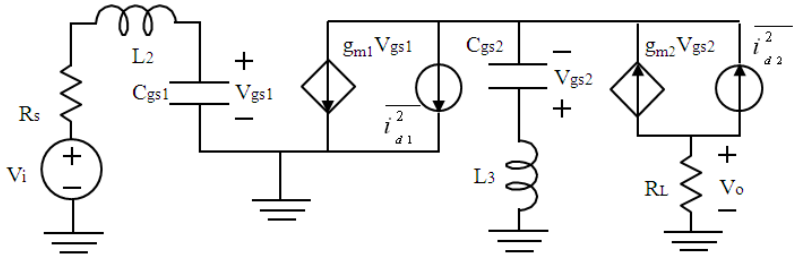

Figure 6. The noise model of the cascode LNA with L_3 at the common-gate stage.

to conventional cascode configurations [23]. Moreover, the presence of L_3 at the common-gate stage achieves high gain, but also contributes additional noises in the circuit as shown in Eq. (11). Therefore the design value of L_3 has to be determined by taking the circuit stability as well as the tradeoff between the gain and NF into consideration.

The nonlinearity of the proposed LNA can be investigated by the transconductance (g_{m}) common-gate transistor. If the body effect of the common-gate stage is neglected, harmonics in the stage are generated mainly from the g_{m} which can be expressed by a Taylor series expansion as follow [24, 25].

$$g_m = g_{m2} + g_{m22}V_{gs2} + g_{m23}V_{gs2}^2 + \cdots \tag{12}$$

Moreover, the corresponding drain current can be describes as a function of g_{m} and gate-to-source voltage (V_{gs2}). Then the third order harmonic distortion (HD_3) of the amplifier is defined as Eq. (14) [24].

$$i_d = g_{m2}V_{gs2} + g_{m22}V_{gs2}^2 + g_{m23}V_{gs2}^3 + \cdots \tag{13}$$

$$\mathrm{HD}_3 = \frac{1}{4}\frac{g_{m23}}{g_{m2}}V_{\mathrm{in}}^2 \tag{14}$$

where g_{m2}, g_{m22}, and g_{m23} are fundamental, second order, and third order transconductance of M_2. As discussed in Section 2.1, L_3 increases V_{gs2} of the M_2 and thereby enhances the amplifier gain or the transconductance (g_{m2}) equivalently However, the increase in g_{m23} is larger than the increase in g_{m2}, which results in higher the third order harmonic distortion as shown Eq. (14). Though the presence of L_3 improves the gain of the amplifier, it also degrades the noise figure and linearity of the amplifier.

3. CIRCUIT IMPLEMENTATION AND MEASUREMENT

The 2.4/5.2-GHz dual-band LNA for WLAN applications was fabricated in a standard mixed-signal/RF bulk 0.18-µm CMOS process, which provides single poly layer and six metal layers (from M_1 to M_6 layers) for interconnections. All capacitors are composed of the metal layers from M_1 to M_6, and the multi-finger capacitors achieve a capacitance density of 1.2-fF/µm^2. Inductors of the circuit are all implemented on the thickest metal layer (M_6) to reduce resistive losses and increase Q factors. Table 1 summarizes the design parameters of the dual-band LNA. The on-chip inductors are conducted by the full-wave electromagnetic simulator (HFSS), and the simulated inductances and Q factors are also extracted and plotted in Fig. 7 [15]. The input/output matching networks can be derived from Eq. (4) to Eq. (9), and each LC element is obtained as a frequency-independent

Parameters	Design Vaiue
M_1	90 μm/0.18 μm
M_2	140 μm/0.18 μm
C_{in}	1.1 pF
C_{out}	0.66 pF
C_1	0.88 pF
C_3	2 pF
C_4	0.22 pF
C_5	0.11 pF
R_1, R_2	5 kΩ

Table 1. Design parameters of the dual-band LNA.

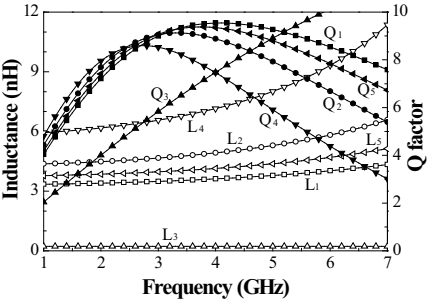

Figure 7. Inductance and Q factor.

value. However, on-chip inductors are strongly frequency-dependent elements [15] which make the design procedure need additional power-matching optimizations. Q factors of the inductors used in the LNA are all lower than 12, and each inductor features higher inductance at higher frequencies. For example, the inductance of L_3 at 2.4 GHz and 5.2 GHz is 0.22 nH and 0.23 nH, respectively.

On-wafer measurements of the dual-band LNA are carried out for gain, input and output return losses, noise figure, and input 1 dB gain compression point ($P_{1\,\text{dB}}$). The stability factor of the LNA is extracted from the measured two-port S parameters. The biasing conditions V_{G1}, V_{G2} and V_{D} of the LNA are 0.7 V, 1.2 V and 1.2 V, respectively. The total current consumption of the LNA is 6 mA. Fig. 8 shows the measured and simulated $|S_{21}|$. The measured results show that the gain of the LNA at 2.4 GHz and 5.2 GHz is 14.2 dB and 14.6 dB, respectively. Two notch frequencies are at 2.9 GHz and 3.9 GHz as shown in Fig. 8. The gains of the LNA without L_3 and with L_3 of 0.8 nH are also simulated for comparison. The maximum gain of the LNA without L_3 is 9.3 dB at 2.1 GHz and 6.8 dB at 4.8 GHz, and therefore the proposed LNA demonstrates a 4.9 dB–7.8 dB gain enhancement. Moreover, the higher L_3 results in higher gain performances of the LNA as shown in Fig. 8. The measured and simulated return losses of the LNA are also plotted in Fig. 9. The measured $|S_{11}|$at 2.4 GHz and 5.2 GHz is -13.5 dB and -13.2 dB, respectively. The measured $|S_{22}|$ at 2.4 GHz and -18.2 dB and -7.3 dB, respectively The poor output matching at 5.2 GHz results from L_3 which also affects the matching network, especially at high frequencies. All the measured and simulated results agree well because of the accuracy in device modeling and full-wave electromagnetic simulations.

Figure 10 shows the stability factor which is extracted from the S parameters to estimate the stability of the LNA. In order to drive the LNA in unconditionally stable and high-gain regions, the value

of L_3 is chosen to keep the stability factor larger than 1 as shown in Fig. 10. The stability factor of the LNA without L_3 which is a conventional cascode amplifier is also larger than 1. However, the high L_3 of 0.8 nH results in stability factor less than 1 beyond 5.8 GHz Then the LNA is potentially unstable. The measured noise figure at 2.4 GHz and 5.2 GHz is 4.4 dB and 3.7 dB, respectively, as shown in Fig. 11. The minimum NF is 3.3 dB at 2 GHz because the LNA is designed by power matching instead of noise matching. Moreover, the absence of L_3 contributes low NF, and the high L_3 of 0.8 nH contributes high NF as shown in Fig. 11. The measured input 1-dB compression point ($P_{1\,\mathrm{dB}}$) at 2.4 GHz and 5.2 GHz is -14 dBm and -13.5 dBm, respectively, as shown in Fig. 12. Fig. 13 presents the chip photo of the LNA with a chip size of 1.06 mm $\times$ 0.79 mm including all testing pads. The L_3 is the smallest inductor as shown in Fig. 13. A figure of merit (FOM)

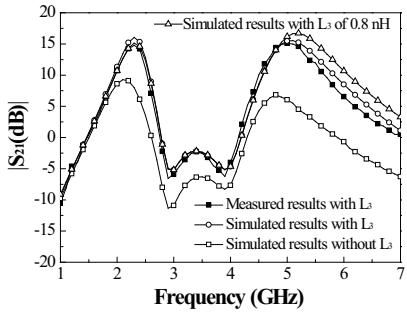

Figure 8. Measured and simulated $|S_{21}|$.

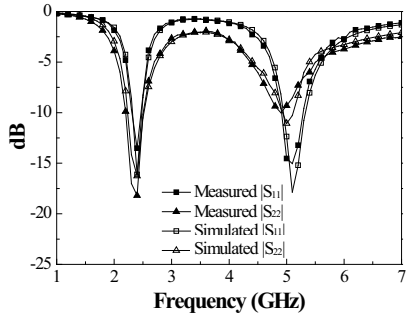

Figure 9. Measured and simulated $|S_{11}|$ and $|S_{22}|$.

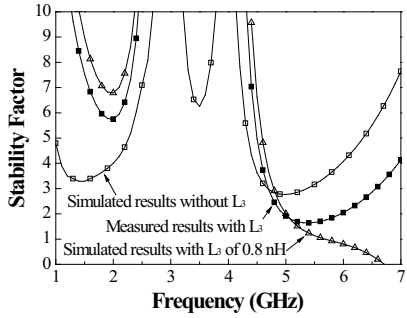

Figure 10. Measured and simulated stability factor.

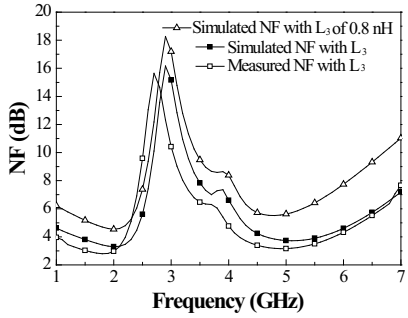

Figure 11. Measured and simulated noise figure.

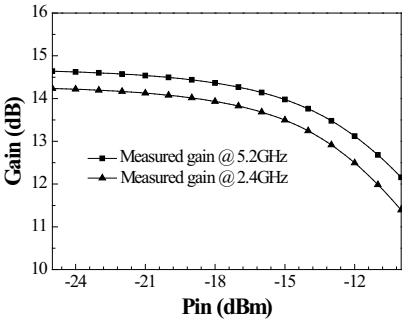

Figure 12. Measured input $P_{1\,\mathrm{dB}}$.

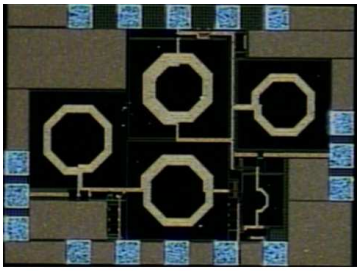

Figure 13. Chip photo of the LNA with a chip size of $1.06 \times 0.79\,\mathrm{mm}^2$.

Table 2. Comparisons of previously reported dual-band LNA.

Parameter	[9]		[16]		[1]*		[2]*		This work	
Process	0.18μm CMOS									
Type	Switchable		Concurrent							
f_0 (GHz)	2.4	5.2	18	24.5	2.4	5.2	2.2	4.6	2.4	5.2
$\|S_{21}\|$ (dB)	10.1	10.9	9.2	12	15	6.5	10.7	8.8	14.2	14.6
NF (dB)	2.9	3.7	5.7	6.4	2.5	2.4	3.53	2.52	4.4	3.7
Pin-1dB (dBm)	−7	−16	N.A.	N.A.	N.A.	N.A.	N.A.	N.A.	−14	−13.5
IIP3(dBm)	4	−5	−2	−3	N.A.	N.A.	−0.5	−5	−3.4	−2.7
P_{DC} (mW)	11.7	5.7	8		10		7.76		7.2	
Gain/P_{DC} (dB/mW)	0.86	1.91	1.15	1.5	1.5	0.65	1.38	1.13	1.97	2.03
FOM (mW^{-1})	0.92	1.61	0.38	0.59	4.07	0.61	1.21	1.24	2.08	2.98
Chip Size (mm^2)	N.A.		0.72 × 0.46		N.A.		N.A.		1.06 × 0.79	

* Simulated results

which allows comparison between LNAs is given as follow [26]

$$\mathrm{FOM}\left[\mathrm{mW}^{-1}\right] = \frac{\mathrm{Gain[abs]}}{(\mathrm{NF}-1)[\mathrm{abs}] \cdot \mathrm{P_{DC}[mW]}}. \tag{15}$$

Table 2 summarizes the previously reported dual-band CMOS LNAs. It reveals that this work demonstrates the highest gain with low-power consumption and the highest FOM. However, the proposed LNA features higher noise figure and lower linearity than the works operated at 2.4/5.2 GHz. Therefore the tradeoff between the gain, NF, and nonlinearity must be considered.

4. CONCLUSION

This work investigates the potential of a high-gain CMOS LNA design using the common-gate inductor at the dual-band frequencies of interest. The inductor aims to increase the gain of the LNA, and the input/output matching networks are used to shape the frequency responses of the LNA rejecting undesired signals. The tradeoffs between the gain, noise figure, and nonlinearity of the LNA are also detailed. Moreover, the LNA is successfully designed, implemented, and verified in a standard 0.18-μm CMOS process. The good agreements between simulated and measured results prove the feasibility of the proposed LNA. Compared to other dual-band LNAs, the proposed LNA exhibits higher gain and FOM with low-power consumption. The design concept of the concurrent LNA facilitates the hardware complexity of dual-band transceivers, and can be applicable to further multi-bands or multi-standards systems.

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