Progress In Electromagnetics Research Letters, Vol. 23, 75–87, 2011

C-BAND PULSED SOLID STATE POWER AMPLIFIER FOR SPACEBORNE APPLICATIONS

J. Dhar, S. K. Garg, R. K. Arora, and B. V. Bakori

MSTD/MSTG/MRSA
Space Applications Centre, ISRO, DOS, Ahmedabad, India

S. S. Rana

Space Applications Centre
ISRO, DOS, Ahmedabad, India

Abstract—The basic applications of pulsed solid state power amplifier are for airborne and spaceborne pulsed Radar and these applications have always demanded well performance over different environmental conditions. The success of the electronic systems for these applications relies on the ability to design high performance; reliable and high yield circuits, which will function against the demanded environmental specifications. This paper describes the detailed design and development of a spaceborne C-band pulsed solid state power amplifier to deliver 12-watt output power, 45 dB gain with 22 microsecond pulse width and 8% duty cycle. The salient features of this paper are drain modulated pulse driver circuit design, non-linear design of the power stages and electronic package design. The paper also describes pulsed SSPA configuration, RF section, Electronic Power Converter Module, RF design and other space aspects to realize the pulsed solid state power amplifier. It is fabricated on the three-layer metallized alumina substrate, integrated with power converter module; and tested under simulated space environment. The test result validates the design specification of the pulsed solid state power amplifier, implemented at miniaturized configuration.

Received 9 February 2011, Accepted 6 April 2011, Scheduled 19 April 2011
Corresponding author: Jolly Dhar (jolly@sac.isro.gov.in).

1. BACKGROUND

Paper [1] shows LDMOS based pulsed power amplifier to deliver 100 watt output power, but not for space usage. Paper [2] refers X-band 17 watt SSPA developed for JPL's Mars Exploration Rover mission, qualified for continuous operation. Paper [3] refers X-band single stage GaAs MMIC, designed as final stage of downlink satellite transmitter, to provide 10 watt saturated power with 12.4 dB gain at 11.7 GHz. The paper referred in [4] describes CW SSPA designed for ESA programme to provide 10 watt output power with 63 dB gain and 24% efficiency. The patent referred in [5] represents an RF amplifier comprising of multiple solid state sub-amplifiers connected in parallel using splitter and combiner technique to get large power for continuous operation of SSPA. This reported work will address the detailed design and development of C-band pulsed solid state power amplifiers designed for space environment. The salient features of this SSPA are non-linear power design, reduced drain to source voltage operation to reduce the voltage stresses and to improve device reliability, drain pulsing for all the stages to reduce the power stress on the devices, resonance free cavity design and space qualification through test and evaluation sequences. The five stage C-band pulsed solid state power amplifier (SSPA) is designed over the frequency range of 5350 ± 112.5 MHz, with 22 microsecond pulse width and 8% duty cycle to feed the pulsed power to the Transreceive modules through the distribution network. The integrated pulsed SSPA block schematic and its specifications are shown in Figure 1 and Table 1, respectively. The SSPA amplifies input pulsed power of -4.2 dBm to output pulsed power of $+40.8$ dBm, with a compressed gain of 45 dB. The SSPA is comprised of two sections namely RF section and dc-dc power converter module.

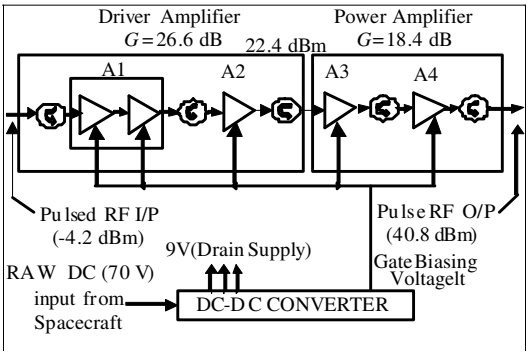

Figure 1. Block schematic of solid state power amplifier.

Table 1. Specifications and test results of pulsed SSPA.

Parameters	Specifications	Achieved Results
Frequency (MHz)	5350 ± 112.5	5350 ± 112.5
O/P saturated Pulse Power	12 W	12.85 W
Gain@5.35 GHz	45 dB	44.5 dB
Gain Flatness	± 1.0 dB	± 0.8 dB
Pulse Width	22 µs	21.75 µs
Duty Cycle	8%	8.3%
Rise Time	100 ns	37 ns
Fall Time	100 ns	89 ns
Gain Ripple	± 4.5 mV	± 3.12 mV
Droop	0.5 dB	0.15 dB
Input Return Loss	15 dB	< -16 dB
Output Return Loss	15 dB	< -15.23 dB
Out of Band suppression	< -45 dBc	< -46 dBc
Total Pulse Current	5.65 A	5.51 A

2. RF SECTION DESCRIPTION

The RF section of the pulsed SSPA [6] consists of driver amplifier and power amplifier. The driver and power stages are designed using GaAs MESFET devices. The driver amplifier is a three stage amplifier, while the power amplifier is a two-stage amplifier. The first stage of the driver amplifier A_1 is a two-stage amplifier based on an integrated approach. The second stage A_2 is a single stage, medium power design. The power amplifier stages A_3 and A_4 are selected based on higher efficiency, higher output power capability and plated heat sink based hermetic package to provide better thermal power dissipation. The driver amplifiers of RF section are designed based on maximum gain, linear approach and power stages by nonlinear approach.

3. DC-DC POWER CONVERTER MODULE

The dc-dc power converter module (PCM) [7] of the pulsed SSPA, as shown in Figure 2, converts the 70-volt raw dc power coming from the satellite bus to the required voltages. The PCM is a DC-DC converter, which is a multi output switch mode power supply, having pulsed as well as continuous outputs. Positive voltages are required for drain biasing, while negative voltages for gate biasing. The 9 V pulsed dc voltages are applied to all drains of the driver and power

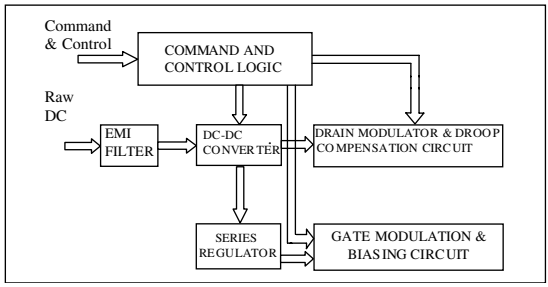

Figure 2. Block diagram of power converter module.

amplifiers. The gate bias voltages required for the respective devices are derived from continuous negative supply of (−5 V). The proper on/off sequences of bias voltages are implemented in PCM to protect the active MESFET devices. During turn-on, gate voltages are applied prior to drain voltages and during turn-off; the drain voltages are removed prior to gate voltages.

4. PULSE DRIVER USING DRAIN MODULATION

The SSPA operates in pulsed mode and remains off 92% of the time. In order to minimize the rise and fall time of the RF output, the drain voltages are pre and post triggered by 1 μs, with respect to the input RF signal. The pulsing arrangement for pulsed SSPA can be either gate or drain modulation. Here, drain pulsing is implemented to realize 12 watt SSPA. The function of the drain modulator and droop compensation circuit, shown in Figure 3, is to modulate the drain voltage from zero to the required 9 V, with fast rise and fall times and minimum voltage droop over the pulse period. Power MOSFET is used as a drain modulator switch. A pulse at the input of driver turns on the modulator switch. Dynamic resistance of the MOSFET is varied over the pulse duration by a closed loop feedback amplifier circuit to compensate the voltage droop at the drain of GaAs MESFET. The drain modulation based pulsed SSPA results in enhanced performance in terms of RF parameter, such as pulsed RF output power, gain flatness and RF detected output characteristics namely gain ripple, rise time, fall time, detected pulsed width and duty cycle. The other objective of the implementation of drain modulation is to save the dc power and to reduce voltage stress on the devices, which in turn, leads to highly reliable pulsed operation of the Pulsed SSPA. Here drain voltage is switched between a zero voltage to a higher positive voltage of 9 V for higher reliable operation since SSPA is off 92% of the time.

5. LINEAR AND NONLINEAR DESIGN AND SIMULATION

The total driver amplifier consisting of A_1 and A_2 is configured to give linear gain of 26.6 dB and output power of 22.4 dBm. The first stage (A_1) is realized with interstage approach based on small signal S-parameters, and designed to deliver an output power of 14.4 dBm with a gain of 18.6 dB and a gain flatness of ± 0.2 dBm over the band of interest. The input and output impedance of the amplifier A_1 is transformed to the 50-ohm source and load impedances respectively, whereas inter-stage impedance matching is used to match the output impedance of first stage to the input impedance of the second stage. This amplifier is unconditionally stable over the interested band, but to ensure the stability over the device operating frequency, a series resistive loading is used. The second stage of the driver amplifier is a medium power, class A design, realized by small signal S-parameters using simultaneous conjugate matched concept to deliver 22.4 dBm output power with a linear gain of 8.3 dB.

The power amplifier design [8, 9] is done using a non-linear model of the power devices to achieve the required power of 12 Watt with 18.4 dB gain. For non-linear design, each device has been modeled using nonlinear equivalent circuits [10, 11]. Matching circuits of both devices are realized using S-parameters. The non-linear design is carried out based on a harmonic balance (HB) technique in which harmonics up to third order are considered. Single carrier non-linear simulation using load pull technique is used at the fundamental frequency 5.35 GHz, to find out the optimum load reflection coefficient to maximize output power. The simulated load reflection co-efficient is shown in Figure 4.

The non-linear output power and gain has been simulated over the discrete values of drain to source voltage (V_{DS}) and for swept input

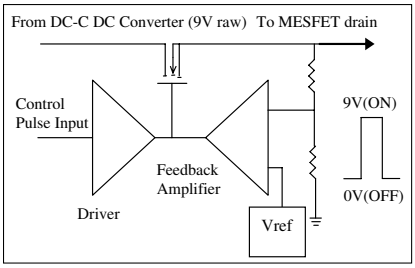

Figure 3. Drain modulation circuit.

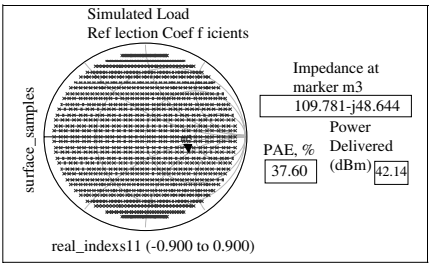

Figure 4. Simulated output load reflection co-efficient.

power. The non-linear design is carried out for better production yield. A guaranteed output power of 12 watt at reduced V_{DS} of 9 V is designed to reduce stress on the device and to increase the reliability. Each individual amplifier has been designed in the non-linear mode and EM simulation is carried out for input and output matching circuit layouts. During EM simulation, a three layer metallized substrate with thickness of 0.635 mm, dielectric constant of 9.9, dielectric loss tangent of 0.0007 and metallization thickness of 8–13 μm was used. Performance optimization is carried out for the individual power stages and also for the integrated power amplifier at the frequency of 5.35 GHz with 250 MHz bandwidth. The simulated output power and gain of the integrated SSPA, at various frequencies and drain to source voltages are shown in Figures 5 and 6 and input-output return loss in Figure 7. The CAD based performance and yield optimization of this SSPA is carried out to improve the unit performance and production yield. The circuit is first analyzed and then optimized until the acceptable performance is achieved. Later on, a yield analysis is performed to determine the manufacturing yield of the circuits.

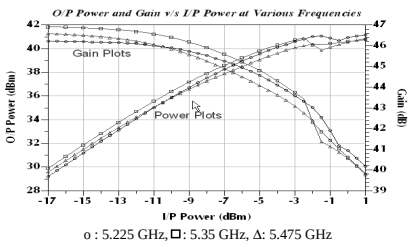

Figure 5. Simulated output power and gain of SSPA over swept input power at various frequencies.

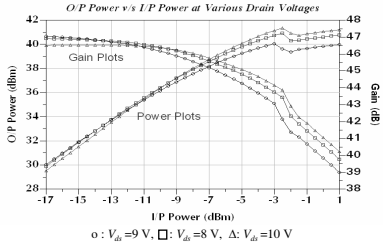

Figure 6. Voltage dependent output power and gain over swept input for SSPA (simulated).

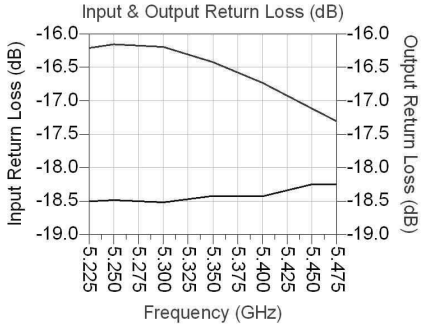

Figure 7. Input and output return loss of SSPA (simulated).

6. EMI/EMC, STRUCTURAL AND THERMAL DESIGN

The reported SSPA is pulsed in nature so it can cause electromagnetic radiation and can affect other subsystems in proximity. It is essential, therefore, to take care of these aspects at the design stage itself. The radiation level is minimized in avoiding sharp corners in the layout; using decoupling capacitor in the microwave circuit; using EMI filters for power supply lines; proper choice of box material [12] and proper electronic package design. The theoretical resonance frequency of the rectangular cavity is calculated from the given equation:

$$f_{mnp} = \frac{c}{2\pi\sqrt{\mu_r \varepsilon_r}} \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2 + \left(\frac{p\pi}{c}\right)^2} \tag{1}$$

where "μ_r" is complex relative permeability, "ε_r" is complex relative permittivity, "a" is width, "b" is height and "c" is length.

The High Frequency Structural Simulator (HFSS) [13] is used to find the resonance frequencies of the cavity. Package is designed to use optimum space. A rectangular package with three separations is used, in which one side contains the driver portion, whereas other part contains the power stages; the DC circuit occupies the interior space of the box. A separation wall is used for separating the RF circuit from the DC circuit. The separation wall contains the required number of holes for EMI filters needed for device biasing. Here total cavity of width of 116.8 mm, height of 12 mm and length of 125.4 mm and multi cavities for driver of inner cavity of width 29.8 mm, height 12 mm, and length 125.4 mm and power amplifiers of inner cavity of width 33 mm, height 12 mm, and length 125.4 mm are considered. The resonance modes obtained from the theoretical equation and analysis are furnished in Table 2. The analysis shows that single cavity approach results into resonance frequencies, which are falling in the

Table 2. Resonance frequencies of the SSPA package.

Different Modes	SSPA Package		Power Amplifier cavity	Driver Amplifier Cavity
	(Theoretical)	(Analysis)	(Theoretical)	(Theoretical)
Mode_1	3.51 GHz	3.51 GHz	4.70 GHz	5.17 GHz
Mode_2	4.41 GHz	4.42 GHz	5.14 GHz	5.57 GHz
Mode_3	5.43 GHz	5.20 GHz	5.79 GHz	6.18 GHz
Mode_4	6.50 GHz	5.33 GHz	6.60 GHz	6.94 GHz
Mode_5	7.62 GHz	5.56 GHz	7.51 GHz	7.82 GHz

frequency band of the SSPA. On the contrary, the partition approach of the whole SSPA cavity into driver cavity, power cavity and dc power distribution cavity as per Figure 8, result no resonance frequency components in the frequency band of solid state power amplifier.

To analyze the structural stability of two SSPAs, placed one above another, structure simulation is carried out by FEM simulator to find out the natural frequency of the structure having random vibration parallel to mounting plate and normal to the mounting plate for different frequency, vibration level and time duration. The simulated structure shows resonance frequency of 989 Hz for the magnitude of displacement from 0 to 35 mm, where middle portion of the top cover shows maximum and mounting lugs portion indicates minimum, as shown in Figure 9. The vibration test was carried out for SSPA packages in X, Y and Z axis. The purpose of carrying out this test is to identify the design and the workmanship related defects. The resonance search was also carried out at 0.5 g, 2000 Hz, 4 Oct/min sweep. The vibration test results for the SSPA structure is shown in Table 3.

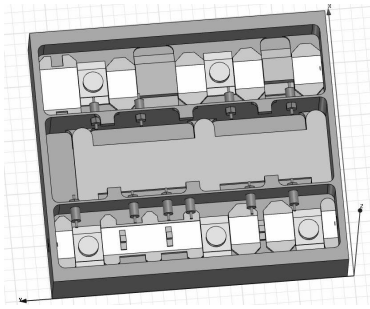

Figure 8. Partition concept of SSPA package.

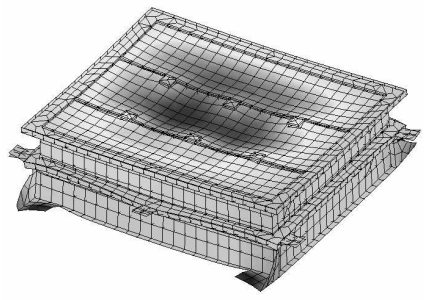

Figure 9. Structural simulation of SSPA package.

Table 3. Vibration test results of the SSPA packages.

Resonance Test at 0.5 g, 2–2000 Hz, 4 Oct/min sweep		Pre Random	Post Random
X	Frequency (Hz)	949	949
	Amplification (g/g)	7.88	7.66
Y	Frequency (Hz)	1210	1210
	Amplification (g/g)	11.66	10.84
Z	Frequency (Hz)	929	905
	Amplification (g/g)	46.4	62.4

The thermal design also carried out for proper heat removal from the package. The device operating junction temperature directly affects reliability and performance of SSPA. Since, the power handling capacity of the device decreases with increase in temperature; again, heat generated degrades the device and reduces device life. The maximum power that can be handled by the junction is dependent upon the type of semiconductor material used. GaAs devices can be operated at a junction temperature of 110°C from a reliability point of view; junction temperature [14] can be expressed as,

$$T_j = T_a + \theta \cdot P_{diss} = T_a + (\theta_{jc} + \theta_{cs} + \theta_{sa}) \cdot P_{diss} \tag{2}$$

where P_{diss}-power to be dissipated, θ-thermal resistance, T_j-junction temperature, T_a-maximum ambient temperature, θ_{jc}-junction-to-case thermal resistance, θ_{cs}-case-to-sink thermal resistance, θ_{sa}-sink-to-ambient thermal resistance. The thermal resistances (θ_{jc}) are 1.6°C/W, 5°C/W and the operating currents are 4.1 A and 1 A at the operating drain voltage of 9 V for the two power devices. The total thermal resistance (θ) for the respective power devices are 1.82°C/W and 5.32°C/W respectively, which are calculated considering all the factors like thermal resistance across interface of device flange and groove of box, thermal resistance across bottom thickness of the box, thermal resistance across side, thermal resistance across interface of

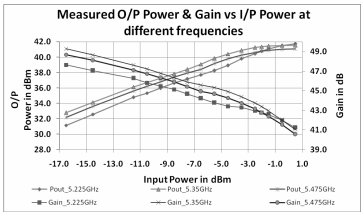

Figure 10. Measured transfer characteristics of microwave amplifier.

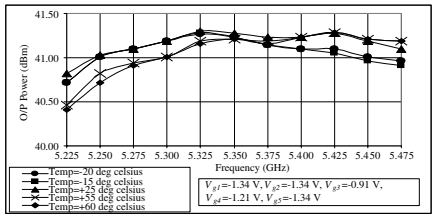

Figure 11. Output power Vs frequency at different temperature.

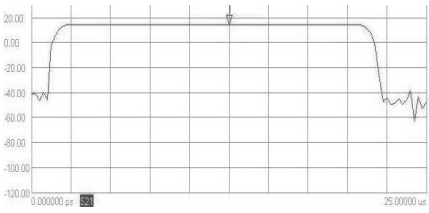

Figure 12. Pulse profile of SSPA gain (mag).

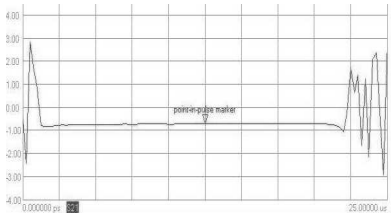

Figure 13. Pulse profile of SSPA gain (phase).

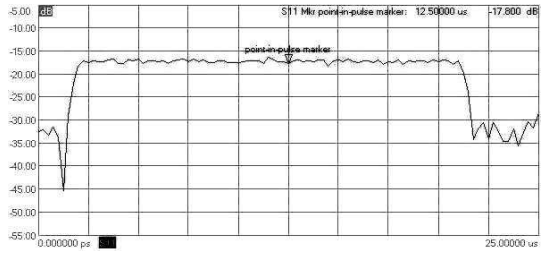

Figure 14. Pulse profile of S_{11} (mag).

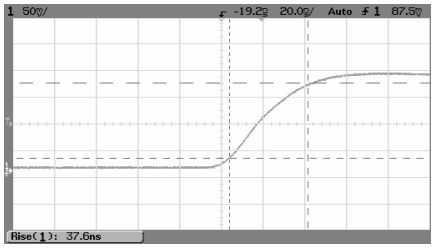

Figure 15. Rise time of the detected signal.

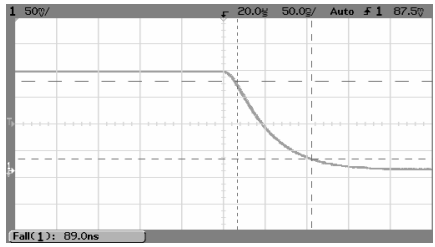

Figure 16. Fall time of the detected signal.

box and heat sink surface. The power dissipation for power devices are 0.72 and 2.95 watt for 8% duty cycle. The calculated junction temperature for the power devices is 56 and 70°C, where maximum temperature rise will be for the final power device. The measured case temperature of the final power device is 65°C, which is below 110°C.

7. DESIGN VALIDATION AND MEASUREMENT OF RF AND PULSE PROFILE

The Flight Model SSPA is developed using space grade components. Alumina substrate with three-layer metallization (Cr-Cu-Au) is selected due to high dielectric constant (9.8), low loss tangent ($\tan\delta$) 0.0007, high thermal conductivity (0.37 W/cm/°C) and its ruggedness at high temperatures. The passive chip components are assembled on the substrate by reflow soldering. The SSPA box is fabricated using Aluminium alloy 6061 T. The size and weight of the SSPA is $156 \times 140 \times 25.4\,\text{mm}^3$ and 400 g. The integrated pulsed SSPA is tested with PCM. The output power and gain at three different frequencies are displayed in Figure 10 and frequency dependent pulsed

Table 4. International scenario of space borne C-band SSPA.

Features	Make		
	Thales Alenia	Comdev	SAC, ISRO work
Frequency (GHz)	5.355–5.455	5.1–5.25	5.35
Bandwidth(MHz)	100	150	225
Power Output(dBm)	≥ 37.8	37	≥ 40.8 dBm
Gain(dB)	-	35.12	44.5
DC power(watt)	Pulsed, DC	21.9	3.8 W (avg) with 8% duty cycle
Mass(g)	600	-	450
Size(mm)	$262 \times 145 \times 50$		$155.4 \times 139.2 \times 24.5$
I/P RL(dB)	< -19	-	< -15
O/P RL(dB)	< -12	-	< -15
Device	-	GaN(power) HBT, Driver	GaAs MESFET
Heritage	RADARSAT-2	M3M Mission	RISAT-1

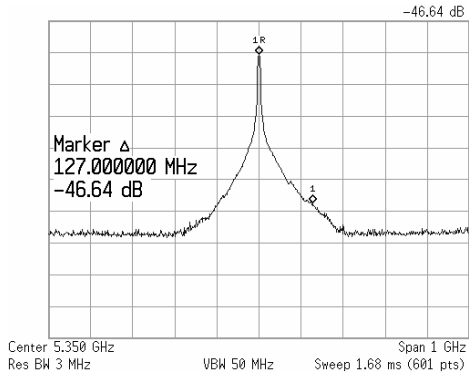

Figure 17. Out of band suppression.

output power measured at constant input power is shown in Figure 11. Figures 12–16 show the pulse profile measurement of magnitude and phase of transfer gain, input return loss, rise time, fall time plots of detected pulse output. The outer band suppression plot is shown in Figure 17. The performance summary, photographs of RF section and integrated SSPAs are shown in Table 1; and Figures 18 and 19 respectively. The international scenario of the space borne SSPAs are shown in Table 4.

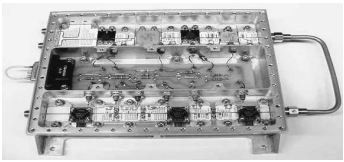

Figure 18. Photograph of RF section.

Figure 19. Photograph of SSPA with PCM.

8. CONCLUSION

The 12 watt SSPA designed, developed and integrated with HMC based pulsed power converter module at a frequency of 5.35 GHz $\pm$112.5 MHz has gone through test and evaluation sequences involving burn-in, EMI-EMC test, vibration tests and thermovaccum test over temperature extremes from -15°C to 65°C. From the simulated (Figure 5) and measured test plots (Figure 10), it is cleared that saturated output power is 40.8 dBm and 41 dBm respectively and SSPA gain is 44 dB and 44.5 dB at 5.35 GHz at the operating voltage (V_{ds}) of 9 V with input power of -4 dBm. The measured plot of input return loss given in Figure 14 verifies the simulated input return loss (Figure 7) better than -16 dB. The maximum temperature rise and the structural stability also have been verified by the thermovaccum and vibration tests. The rigorous environmental test carried out on this SSPA qualifies it for space usage and the overall performances of SSPA are well within its specified boundary limits. As per international scenario given in Table-4 for the space borne SSPAs operating almost at near frequency range, it shows that the reported SSPA in the miniaturized package of 155.4 mm $\times$ 139.2 mm $\times$ 24.5 mm with reduced mass is providing more than 12 watt pulsed rf output power and 44.5 dB gain over the frequency band of 225 MHz with average dc power consumption of 3.8 watt.

ACKNOWLEDGMENT

The authors are thankful to the MIC facility, workshop, STAD and mechanical package designer for their kind cooperation. We would also like to thank Dr. P. K. Srivastava, Deputy Director, SIPA and Shri Santanu Chowdhury, Group Director, AIPG for reviewing and giving valuable suggestions. We are also very grateful to Dr. R. R. Navalgund, Director, SAC and Shri Tapan Misra, Deputy Director, MRSA for motivating us to write this paper and allowing us to present and publish it. The authors would also like to express thanks to the reviewers and editors for their valuable advice and suggestions.

REFERENCES

1. Yi, H. and S. Hang, "Design of L-band high speed pulsed power amplifier using LDMOS FET," *Progress In Electromagnetics Research M*, Vol. 2, 153–165, 2008.
2. Boger, W., et al., "X-band 17 watt SSPA for space applications," *IEEE MTT-S International on Microwave Symposium Digest*, 2005.
3. Scappaviva, F., et al., "10 watt high efficiency gaas mmic power amplifier for space applications," *European on Microwave Integrated Circuit Conference, EuMIC*, 2008.
4. Czech, J., A.-M. Khilla, and M. Schunzel, "A 10 watt C-band GaAs FET power amplifier for satellite down-link communications systems," *14th European Microwave Conference*, 1984.
5. Rector Robert, M., "Solid state microwave power amplifier," Patent # WO 2007146052, December 21, 2007.
6. Dhar, J., S. K. Garg, R. K. Arora, B. V. Bakori, and S. S. Rana, "Space borne C-band pulsed solid state power amplifier," *IEEE Applied Electromagnetics Conference, AEMC*, 2009.
7. Dhar, J., S. K. Garg, R. K. Arora, and S. S. Rana, "Performance enhancement of pulsed solid state power amplifier using drain modulation over gate modulation," *IEEE ISSCS 2009 Proceeding*, 1–4, July 9–10, 2009.
8. Cripps, S. C., *Advanced Techniques in RF Power Amplifier Design*, Artech House, Norwood, MA, 2002.
9. Golio, M. and J. Golio, *The RF and Microwave Circuits, Measurements and Modeling*, CRC Press, New York, 2008.
10. Dhar, J., S. K. Garg, R. K. Arora, and S. S. Rana, "Nonlinear design of a C-band power amplifier using EEHEMT nonlinear model," *IEEE ISSCS 2007 Proceeding*, Vol. 1, 89–92, 2007.
11. Dhar, J., S. K. Garg, R. K. Arora, and S. S. Rana, "Nonlinear model based power amplifier," *IEEE Applied Electromagnetics Conference, AEMC*, 2009.
12. Dhar, J., R. K. Arora, A. Dasgupta, and S. S. Rana, "Enclosure effect on microwave power amplifier," *Progress In Electromagnetics Research C*, Vol. 19, 163–177, 2011.
13. Ansoft High Frequency Structure Simulator, Version 10, User's Manual.
14. Allan, W. Scott, *Cooling of Electronic Equipment*, John Wiley & Sons.