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A WIMEDIA COMPLIANT CMOS RF POWER AMPLIFIER FOR ULTRA-WIDEBAND (UWB) TRANSMITTER

S.-K. Wong and F. Kung

Faculty of Engineering
Multimedia University
Jalan Multimedia
Cyberjaya 63000, Malaysia

S. Maisurah and M. N. B. Osman

Telekom Research and Development
Malaysia

Abstract—A WiMedia compliant CMOS RF power amplifier (PA) for ultra-wideband (UWB) transmitter in the 3.1 to 4.8 GHz band is presented in this paper. The proposed two-stage PA employs a cascode topology on the first stage as driver while the second stage is a simple common source (CS) amplifier. In order to improve the efficiency and output power, the output impedance of the driver amplifier (first stage) is optimized so that it falls on the source-pull contours of the second stage amplifier. On-wafer measurement on the fabricated prototype showed a maximum power gain of +15.8 dB, 0.6 dB gain flatness, +11.3 dBm of output 1 dB gain compression and up to a maximum of 17.3% power added efficiency (PAE) at 4 GHz using a 50 Ω load termination, while consuming only 25.7 mW from a 1.8 V supply voltage. Measurement results obtained are used to create a non-linear power-dependent S-parameter (P2D) model for wideband input and output matching optimizations and co-simulations with the UWB modulated test signals. Using the created P2D model, the PA achieved a maximum output channel power of +3.48 dBm with an error vector magnitude (EVM) of −23.1 dB and complied with the WiMedia mask specifications.

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Corresponding author: Sew-Kin Wong (skwong@mmu.edu.my).

1. INTRODUCTION

At present, the emerging of high speed and high data-rate wireless communications has encouraged intensive research in both academic and industrial fields. Ultra-wideband (UWB) system, compared to Bluetooth and WiMax, has emerged as a new technology capable of offering a high data-rate and wide spectrum of frequency (low frequency band from 3.1 to 5 GHz and high frequency band from 6 to 10.6 GHz) with very low power transmission [1]. Two organizations have been actively promoting both the MB-OFDM UWB and DS-UWB applications outside the IEEE task group. They are the WiMedia Alliance [2] for MB-OFDM and the UWB Forum [3] for DS-UWB. For the first generation UWB system deployment, both the approaches use a low frequency band of 3.1 to 5 GHz (Band Group 1) as a mandatory mode to transmit data up to 480 Mbps. This group has three bands, 3.168 to 3.696 GHz (Band 1), 3.696 to 4.224 GHz (Band 2) and 4.224 to 4.752 GHz (Band 3). As proposed by WiMedia Alliance [2], UWB could be used as general USB cable replacement (also known as Wireless USB) and short-range high data rate communications between mobile phones, laptop, and digital consumer products such as camera, TV and camcorder.

The power amplifier (PA) circuit design in the UWB transmitter is a challenging task in order to meet stringent requirements such as high power gain and optimum power efficiency across wide bandwidth while maintaining low power consumption. Various topologies have been used in the implementation of wideband amplifiers. Among that have been reported are the resistive shunt feedback with current reused topology [4], feedback with negative group delay circuit topology [5], differential architecture [6, 7] and the RLC matching and filtering topology [8–11]. In this paper, the proposed PA relies on a two-stage amplifier to achieve optimum output power, efficiency and gain while maintaining a wide bandwidth. Using 0.18 µm standard RF CMOS process, the PA employs a cascode topology on the first stage as driver amplifier with a current mirror circuit while the second stage is a simple common-source (CS) stage PA. Driver amplifier is used in the first stage to provide sufficient power amplification to drive the second stage, in order to maintain a high efficiency and gain of the overall power amplifier [12]. This paper is organized as follows. Section 2 explains the overall circuit description, design and analysis of the proposed driver amplifier and CS PA. The source pull analysis is also discussed in this section. The chip layout and on-wafer measurement results are reported in Section 3. In Section 4, the post measurement results analyses explored the effect of wideband input

and output matching and co-simulations with the UWB modulated test signals, using nonlinear behavioural model (P2D data file) are reported. Finally, Section 5 presents the conclusion of this work.

2. CIRCUIT IMPLEMENTATION

In order to produce large output power, it is usually necessary to have large DC current across the active component in the PA. This may leads to high DC dissipation across the parasitic resistance in the bias path [13]. Among the CMOS amplifiers discussed in [14], the CS configuration is the most suitable configuration for PAs due to its large small-signal current and voltage gains. On top of that, the transistor biasing under CS configuration can also be easily achieved by using current mirror. Usage of current mirror allows large DC current into transistor with minimal DC resistance in the path. Cascode topology with high output impedance is seldom used in PA design because the CG stage can lead to instabilities associated with large RF shunt capacitor at the gate resonating with the inductance of the non-ideal ground connection [13]. Nevertheless, due to its high gain, the cascode circuit can be used for pre-amplifier or driver amplifier implementation [15]. The proposed PA employs a cascode topology on the first stage as a driver amplifier while the second stage is a simple CS PA. The proposed two-stage PA is shown in Figure 1. Transistor M_1

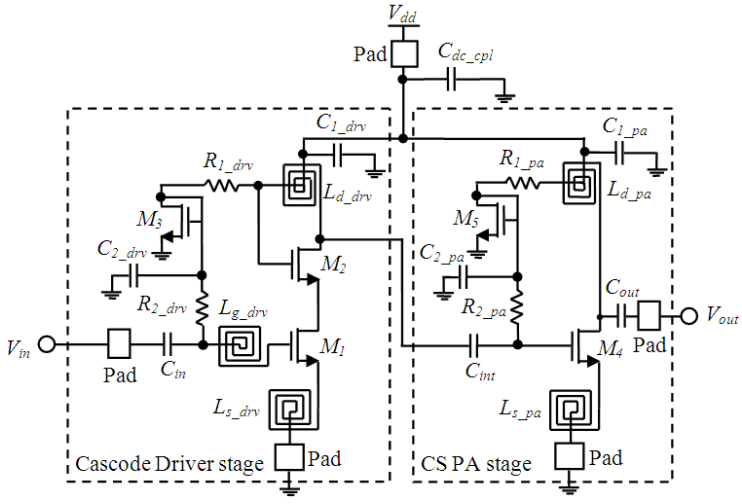

Figure 1. Two-stage UWB PA with cascode driver amplifier and CS PA.

and M_2 form the cascode pair, while M_3, M_5, R_{1_drv}, R_{2_drv}, R_{1_pa} and R_{2_pa} form current mirrors which set the DC bias of M_1 and M_4. This PA is initially targeted at a DC power consumption of 25 mW from a 1.8 V DC supply. This gives the total drain current of approximately 14 mA, to be distributed over the two-stage. The proposed design are simulated and optimized with Agilent Technologies's Advanced Design System (ADS) software before IC layout and fabrications.

Assuming a current of 10 mA to be drawn by transistor M_4 for second stage, the calculated size for NMOS transistor M_4 is approximately 209 µm under saturation [14]:

$$I_{D4} = \frac{1}{2}\mu_n C_{ox}\frac{W_4}{L}(V_{GS4} - V_{t4})^2 \tag{1}$$

where $\mu_n = 327.4\,\text{cm}^2/\text{Vs}$, $C_{ox} = 8.42 \times 10^{-3}\,\text{pF}/\mu\text{m}^2$, the threshold voltage, $V_{t4} = 0.5\,\text{V}$ and the gate-source voltage, $V_{GS4} = 0.75\,\text{V}$, for a typical 0.18 µm silicon CMOS process.

In general, a large transistor size M_4 is needed to provide high gain and output power of the amplifier at high frequency. However, large transistor size usually has high parasitic capacitance and transconductance, which will increase the power consumption [16]. For optimum power consumption, the transistor size of M_4 is chosen to be 160 µm. In order to produce V_{GS} of 0.75 V (for Class-A operation), the biasing resistors R_{1_pa} and R_{2_pa} are fixed at 2 kΩ respectively. The source degeneration inductor, L_{s_pa} is maintained as 0.5 nH for optimum stability and gain. The required RF choke inductor, L_{d_pa} is optimized using on-chip spiral inductor (with RLC equivalent circuits) for a reasonable output 1 dB gain compression ($P_{1\,\text{dB}}$) across the 3 to 5 GHz frequency range, as shown in Figure 2. As seen in Figure 2, L_{d_pa} of 4 nH is chosen, which produces an output $P_{1\,\text{dB}}$ of 7.5 dBm to 8.5 dBm across 3 to 5 GHz. In order to provide sufficient RF shunting, two large on-chip capacitors (C_{1_pa} and C_{2_pa}) of 10 pF are included in the circuit. Finally, capacitors (C_{int} and C_{out}) of 1 pF each are used as dc blocks.

Results of the large-signal analysis are shown in Figures 3 to 5 respectively. The simulated input and output return losses of the second-stage CS PA are less than −2.5 dB and −8.5 dB respectively over the frequency range of interest from 3 to 5 GHz. It is observed that across the frequency range from 500 MHz to 15 GHz, the PA is unconditionally stable since the Rollet's stability factor, K is greater than 1. The maximum power gain achieved in this stage is approximately +8.9 dB at 2.5 GHz and the simulated output $P_{1\,\text{dB}}$ for this stage at 3, 4 and 5 GHz are +8.51 dBm, +7.75 dBm and +7.67 dBm respectively.

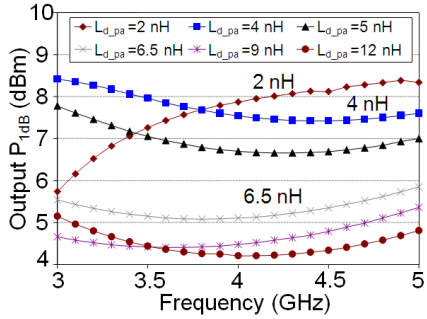

Figure 2. Output 1 dB gain compression ($P_{1\,\mathrm{dB}}$) of the second-stage CS PA for different values of L_{d_pa}.

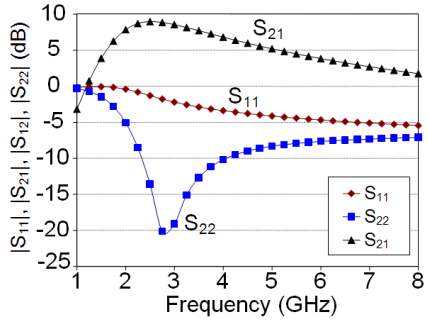

Figure 3. Simulated large-signal gain $|S_{21}|$, input return losses $|S_{11}|$ and output return losses $|S_{22}|$ of the second-stage CS PA. Input power, $P_{in} = -2\,\mathrm{dBm}$.

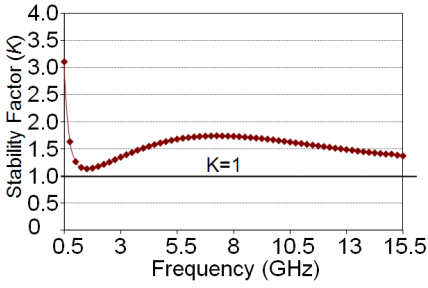

Figure 4. Simulated stability plot for the second-stage CS PA. Input power, $P_{in} = -2\,\mathrm{dBm}$.

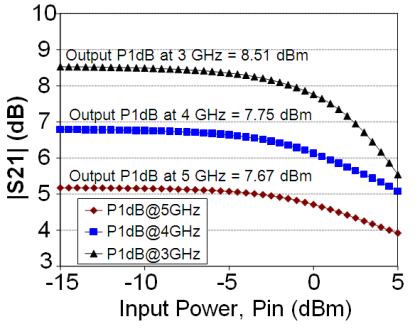

Figure 5. Simulated 1 dB gain compression for the second-stage CS PA.

A purely resistive source impedance and load impedance of 50 Ω are assumed in the simulation carried out previously. However, these assumptions are not always true [17]. In two-stage PA design, the output impedance of the driver amplifier (Z_{out_drv}) is the source impedance (Z_{s_pa}) "seen" by the CS PA stage (as shown in Figure 6). For optimum output power and efficiency across a wide bandwidth, both of these impedances must be equal. In order to investigate the effect of variable source impedance on the power delivered, a systematic way to vary the real and imaginary parts of the source impedance is needed. Contours of constant output power in the Smith chart are plotted, with varying source impedance. The processes of plotting the

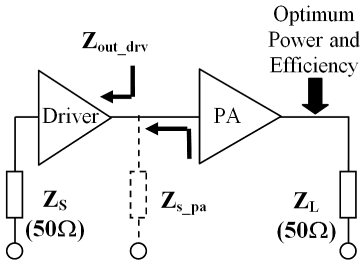

Figure 6. For optimum power delivery, $Z_{out\_drv} = Z_{s\_pa}$.

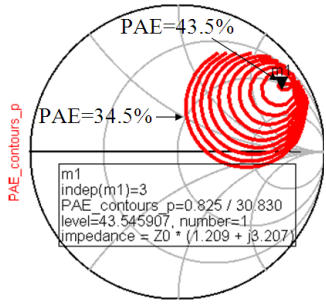

Figure 7. Constant PAE contours (in 1% step) at 3 GHz after source-pull simulation with the load impedance and input power are set to 50 Ω and 3 dBm respectively.

constant contours are collectively known as source-pull analysis [18].

In this work, the pre-configured source-pull simulation template in Agilent ADS software is used to determine the optimal conditions for maximum efficiency. Here, the output load impedance is fixed at 50 Ω while the available input power is maintained as 3 dBm, with the source impedance being varied. The simulated constant power added efficiency (PAE) contours at 3, 4 and 5 GHz using source-pull simulation are shown in Figures 7, 8 and 9 respectively. Based on these simulations, the second-stage CS PA has a maximum PAE of 43.5%, 33.4% and 22.7% at 3, 4 and 5 GHz respectively, with the output load impedance of 50 Ω. As seen in Figures 7 to 9, the required input source impedance for high PAE is located at the upper right quadrant (inductive region) of the Smith chart. This indicates that the output impedance of the first-stage driver amplifier (Z_{out_drv}) must be within these regions for optimum PAE and output power.

The first-stage driver amplifier is an inductive degeneration CS cascode amplifier, optimized for gain, instead of the output power and PAE. The cascode topology is considered in this design due to its high active load that increases the overall gain of an amplifier [14, 19]. Assuming that the remaining current of 4 mA (total current of 14 mA, 10 mA is drawn by second-stage) to be drawn by M_1 for first stage, the calculated size for transistor M_1 is approximately 80 µm based on Equation (1). This amplifier is designed using the same component values as the CS PA stage; $L_{s\_drv} = 0.5$ nH, $R_{1\_drv} = R_{2\_drv} = 2$ kΩ and $C_{1\_drv} = C_{2\_drv} = 10$ pF. The output impedance of the driver amplifier

is mainly determined by the drain inductor at transistor M_2, L_{d_drv}. The output impedance of the driver amplifier for different values of L_{d_drv} (2 nH, 4 nH and 6 nH) on the Smith chart is shown in Figure 10. Combining the output impedance plot and the constant PAE contours into one Smith chart, it is seen that the plot for $L_{d\_drv} = 4$ nH will overlap the constant PAE contours, as shown in Figure 11. The PAE at 3, 4 and 5 GHz, achieved by the second-stage CS PA with respect to the output impedance of the driver amplifier when $L_{d\_drv} = 4$ nH,

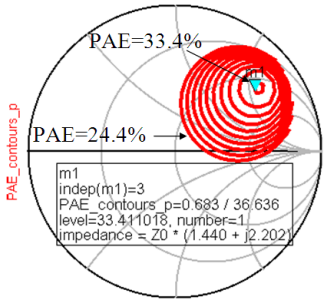

Figure 8. Constant PAE contours (in 1% step) at 4 GHz after source-pull simulation with the load impedance and input power are set to 50 Ω and 3 dBm respectively.

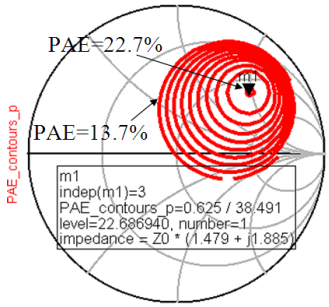

Figure 9. Constant PAE contours (in 1% step) at 5 GHz after source-pull simulation with the load impedance and input power are set to 50 Ω and 3 dBm respectively.

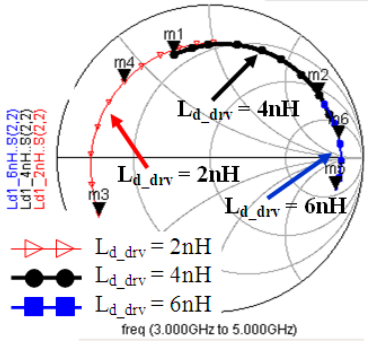

Figure 10. Output impedance of the driver amplifier for different values of L_{d_drv} (2 nH, 4 nH and 6 nH).

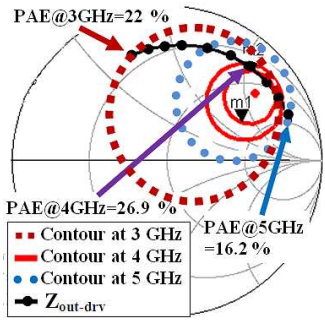

Figure 11. PAE achieved by second-stage CS PA at 3, 4 and 5 GHz, when $L_{d\_drv} = 4$ nH.

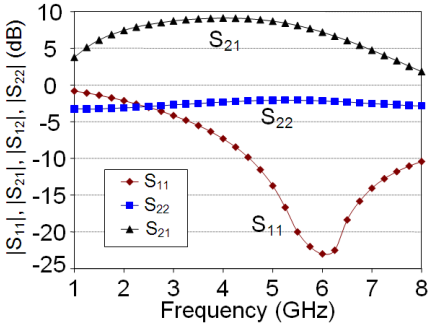

Figure 12. Simulated small signal gain $|S_{21}|$, input return losses $|S_{11}|$ and output return losses $|S_{22}|$ of the first-stage driver amplifier.

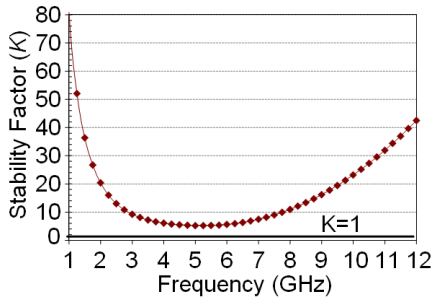

Figure 13. Simulated stability plot for the first-stage driver amplifier.

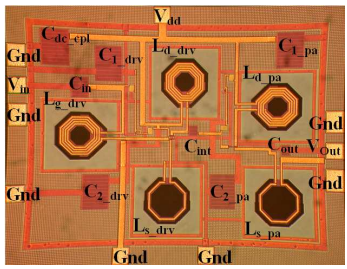

Figure 14. Die micrograph of the proposed two-stage PA.

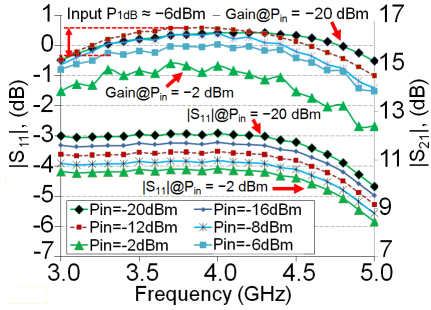

Figure 15. Measured $|S_{21}|$ and $|S_{11}|$ vs. input power, P_{in} for the two-stage PA.

are also depicted in Figure 11.

As shown in these figures, the second-stage CS PA will reach the PAE of approximately 22%, 26.9% and 16.2% at 3, 4 and 5 GHz respectively when the driver amplifier is cascaded into the input of the second-stage CS PA. As shown in Figure 12 on the small-signal simulation for the proposed amplifier, the simulated input and output return losses are less than -4 dB and -2 dB respectively over the frequency range of interest from 3 to 5 GHz. The driver amplifier achieved the maximum power gain of 9.1 dB at 4 GHz. This amplifier is also unconditionally stable since the stability factor, K is greater than 1 from 1 to 12 GHz, as shown in Figure 13.

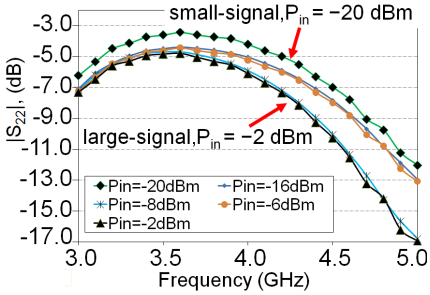

Figure 16. Measured $|S_{22}|$ vs. input power, P_{in} for the two-stage PA.

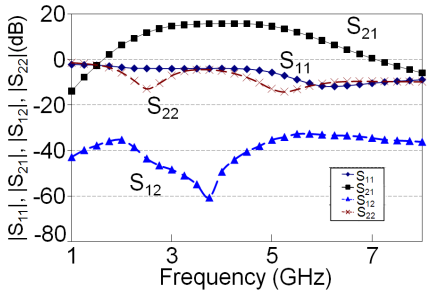

Figure 17. Measured large-signal S-parameters for the two-stage PA. Input power, $P_{in} = -7$ dBm.

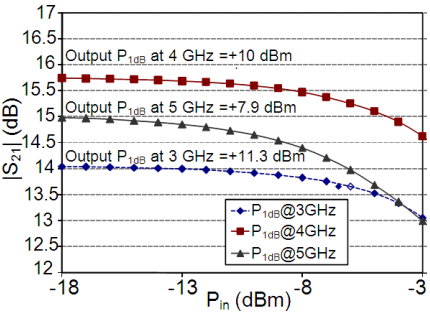

Figure 18. Measured Output $P_{1\,\mathrm{dB}}$ for the two-stage PA.

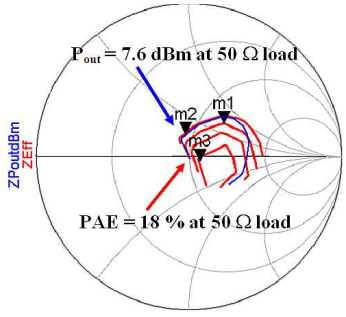

Figure 19. Measured load-pull contours at 3 GHz (at input power, $P_{in} = -7$ dBm)

3. EXPERIMENTAL RESULTS

The proposed two-stage PA has been fabricated in Silterra Malaysia Sdn Bhd using 0.18 µm CMOS process with bond pads. The die microphotograph is shown in Figure 14, with a size of 1.1 mm × 1.5 mm. On-wafer measurements are carried out for power gain, return losses and 1 dB gain compression ($P_{1\,\mathrm{dB}}$). Active load-pull measurement system from Maury Microwave Corporation and Agilent E8722ES network analyzer are used to determine the actual PAE and output power measurements [20]. The measured small-signal and large-signal S-parameter data are shown in Figures 15 to 17 respectively. As shown in Figure 15, the input $P_{1\,\mathrm{dB}}$ of the two-stage PA is approximately −6 dBm across 3 to 5 GHz. Also, the

input return loss improved when the PA approached the large-signal condition. In Figure 16, output return loss of the PA is optimum when the input power, P_{in} reached approximately -8 dBm. Based on these results, the input power to the proposed PA is set to be approximately -7 dBm. Figure 17 shows that the PA has a gain of approximately 15.2 ± 0.6 dB over the 3 to 5 GHz frequency range while maintaining a 3-dB bandwidth of 2.6 to 5.4 GHz, when P_{in} is set to -7 dBm. The $P_{1\,\mathrm{dB}}$ measurement is depicted in Figure 18. Here, the output $P_{1\,\mathrm{dB}}$ for the PA at 3, 4 and 5 GHz are 11.3 dBm, 10 dBm and 7.9 dBm respectively. The load-pull measurements at 3 to 5 GHz for PAE and output power are shown in Figure 19 and Table 1 respectively. Figure 19 shows that the PA achieved a maximum output power of 7.6 dBm with PAE of 18% in a 50 Ω load impedance, at 3 GHz. As indicated in Table 1, the performance of the PA drop significantly as the frequency reaches 5 GHz, with output power of 5.5 dBm and PAE of 9.1% at a 50 Ω load impedance. Table 2 shows measurement summary and comparison with other literatures. The discrepancies between the simulation and measurement results are probably due to the inaccuracies in large-signal transistor model and the parasitic capacitances and inductances in the on-chip components and metal layer interconnects. The parasitic effects are becoming more critical especially when high frequency circuit is involved. At higher frequencies, two loss mechanisms, namely the conductor and substrate

Table 1. Measured load-pull results from 3 to 5 GHz at input power, $P_{in} = -7$ dBm, input and output impedances are set at $Z_s = Z_L = 50\,\Omega$. The values of output $P_{1\,\mathrm{dB}}$ are inserted as reference.

Frequency (GHz)	PAE (%)	Output Power, P_{out} (dBm)	Output $P_{1\,\mathrm{dB}}$ (dBm)
3.0	18.0	7.60	11.3
3.2	19.1	7.92	11.5
3.4	19.3	7.90	11.4
3.6	19.8	8.02	11.6
3.8	18.3	7.80	11.4
4.0	17.3	8.10	10.0
4.2	17.0	7.78	9.9
4.4	16.2	7.73	9.3
4.6	14.7	7.42	8.8
4.8	11.4	6.45	8.2
5.0	9.1	5.50	7.9

Table 2. Comparison of wideband 0.18 µm CMOS PAs: Published and the present works.

Ref.	3 dB BW (GHz)	S_{11} (dB)	S_{22} (dB)	$S_{21\,\max}$ (dB)
[4] [Simulated]	3 to 7	< -5	< -7	10
[6]	3.1 to 7	< -8	< -11	10
[8]	3.1 to 4.8	< -10	< -8	19
[9]	3.1 to 10.6	< -9	< -8	15
[10]	3 to 12	< -10	< -8	10.5
[11]	3 to 4.6	< -10	< -10	17.5
This work [Simulated]	2.9 to 5.2	< -5.7	< -5.5	22.3
This work [Measured]	2.6 to 5.4	< -4	< -4.5	15.8
This work [P2D]*	2.9 to 4.9	< -8	< -8.5	18.4

Ref.	$P_{1\,\mathrm{dB}}$@4 GHz (dBm)	PAE@4 GHz (%)	Power (mW)	Area (mm^2)
[4] [Simulated]	> 0 (output)	12% (average)	15	0.9×1.0
[6]	1.25 (output)	11% at $P_{in} = 3.5$ dBm	35	1.3×1.4
[8]	-22 (input) -4.2 (output)	N/A	25	1.9×1.1
[9]	0 (output)	N/A	25.2	1.1×1
[10]	5.6 (output)	N/A	84	2.3×0.8
[11]	0.42 (output)	3.9%	N/A	1.6×1.0
This work [Simulated]	-11.5 (input) 9.8 (output)	26% at $P_{in} = P_{1\,\mathrm{dB}} = -11.5$ dBm	25	1.1×1.5
This work [Measured]	-3.4(input) 11.3 (output)	17.3% at $P_{in} = -7$ dBm, 24.2% at $P_{in} = P_{1\,\mathrm{dB}} = -3.4$ dBm	25.7	1.1×1.5
This work [P2D]*	-6(input) 11.5 (output)	27.7% at $P_{in} = -7$ dBm, 29.2% at $P_{in} = P_{1\,\mathrm{dB}} = -6$ dBm	25.7	-

*Post analysis with 3-stage multi-section LC matching using P2D model

loss are involved. Conductor loss is important due to skin effect while substrate loss will be dominant in the lossy medium of silicon [21–24].

4. POST MEASUREMENT ANALYSIS USING P2D NON-LINEAR MODEL

The nonlinear Microwave Data Interchange Format (MDIF) P2D (Power Dependent S-parameter) model serves as a simple behavioral model format for nonlinear microwave devices [25, 26]. In this work, the P2D data file is created manually from the measurement data obtained using a frequency sweep of 2.5 to 5.5 GHz, while the input power was set to sweep from −20 dBm to 0 dBm, with the s-parameter of the two-stage PA measured on the Agilent E8722ES network analyzer. The P2D data file contains a table of small-signal S-parameters data over frequency and a series of tables of Large-signal S-parameters (LSSP) data. Each table of LSSP data is plotted at a single frequency and contains LSSPs as a functions of the power incident at Port 1 and Port 2. The measurement-based MDIF P2D model could be used to estimate the performance of a high-frequency amplifier using software-based modulated signal [27, 28]. P2D model can also provide a higher level of accuracy since it includes the measured S-parameter as a function of power and frequency compared to a normal s-parameter data (S2P, as discussed in [29]) that only accommodate small-signal power level.

In this work, the UWB Transmitter Test Bench available in Agilent ADS software as shown Figure 20 is used to simulate the

Table 3. Summary of the overall co-simulation with the P2D model at input data rate and channel power of 320 Mbps and −12 dBm.

Parameters	Band 1	Band 2	Band 3	Specifications [2]
Output Channel Power (dBm)	3.17	3.48	2.85	> -9.9
Occupied BW, (MHz)	507.4	506.9	507.2	< 507.4
ACPR_L (dBc)[1]	−25.8	−25.7	−26	N/A
ACPR_H (dBc)[2]	−26.6	−26.5	−25.9	N/A
Error Vector Magnitude, EVM (dB)	−22.7	−23.1	−21.8	< -19.5

[1]: Lower band Adjacent Channel Power Ratio
[2]: Higher band Adjacent Channel Power Ratio

UWB modulated output spectrum based on the P2D model created for the two-stage PA. The simulated performances of the P2D model, demodulated by the Agilent 89600 Vector Signal Analyzer (VSA) software are shown in Figures 21 and 22 respectively. The overall co-simulation results with the P2D model across 3.1 to 4.8 GHz, at input data rate and channel power of 320 Mbps and −12 dBm are summarized in Table 3. Here, results shows that the proposed two-stage PA

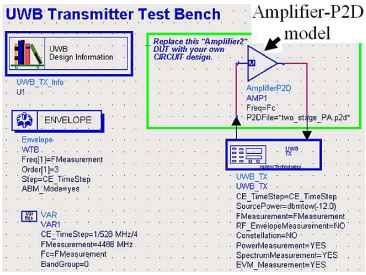

Figure 20. Simulation setup for testing the P2D model created for the two-stage PA with MBOFDM UWB signal. Note that, input power, $P_{in} = -12$ dBm.

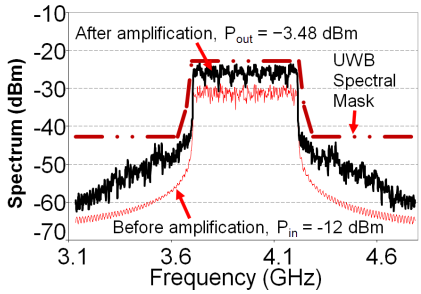

Figure 21. Simulated output spectrum at Band 2 (3.696 to 4.224 GHz). Input data rate and channel power are 320 Mbps and −12 dBm, respectively.

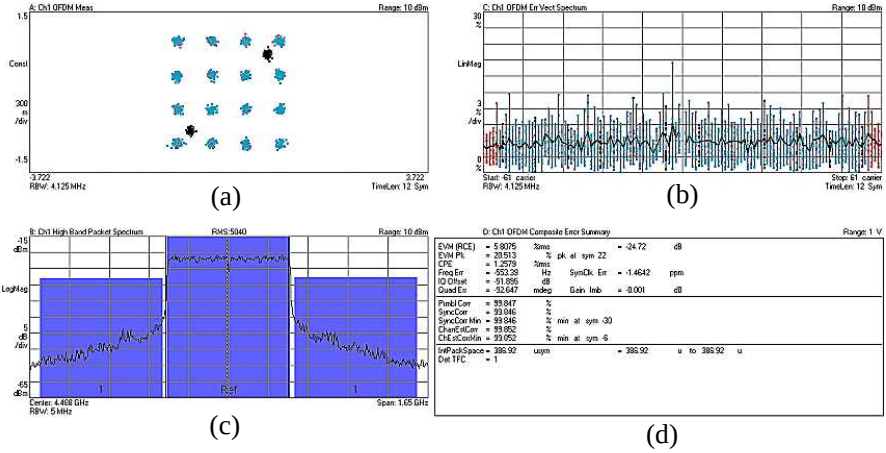

Figure 22. Simulated performance of the P2D model at Band 3 (4.224 to 4.752 GHz). (a) Constellation. (b) EVM versus time. (c) Adjacent Channel Power Ratio (ACPR). (d) EVM summary table.

achieved satisfactory performance towards the WiMedia specifications.

The measured input and output impedances of the two-stage PA (unmatched) are depicted in Figure 23. At frequencies across 3.1 to 4.8 GHz, the input and output impedances fall in the capacitive region. Using an approximately average value of 3.7 GHz, a multi-section low Q LC matching [30] are used to match over the frequency of 3.1 to 4.8 GHz. The optimal Q-factor and insertion loss (IL) of the multi-section LC network are expressed as [30]:

$$Q = \sqrt{\left(\frac{R_{hi}}{R_{lo}}\right)^{1/N} - 1} \tag{2}$$

$$IL = \frac{1}{1 + N\frac{Q}{Q_c}} \tag{3}$$

where, R_{hi} and R_{lo} are the maximum resistance and minimum resistance of the unmatched source or load resistance, N is the number of sections or order of the LC network and Q_c is the available Q-factor of the individual component.

The multi-section LC matching networks for both the input and output of the two-stage PA are shown in Figure 24. The calculated optimal Q-factor and insertion loss as a function of the number of sections (N), based on Equations (2) and (3) are listed in Table 4. From the table, it is obvious that the four sections yield the optimal solution, as the Q-factor saturates when the N is more than four. However, a three-section matching networks are applied in this work for simplification purposes. Applying these multi-section LC wideband matching techniques into the P2D model in Agilent ADS software, optimizations are performed towards the optimum output power over

Table 4. The optimal Q and insertion loss (IL) of input and output matching using multi-section LC networks. Assumed that the component Q-factor (Q_c) of 10.

Input Matching						
N	1	2	3	4	5	6
Q	1.77	1.02	0.78	0.65	0.57	0.52
IL (dB)	0.71	0.81	0.92	1.02	1.08	1.20
Output Matching						
N	1	2	3	4	5	6
Q	0.37	0.26	0.21	0.18	0.16	0.15
IL (dB)	0.16	0.22	0.27	0.30	0.33	0.37

the three bands (3.1 to 4.8 GHz). The schematic setup for optimizing the input and output matching using P2D file is shown in Figure 25. Additional resistors (R_1 and R_2) are added to the input matching for efficient wideband output power performance [31]. The performances before and after the multi-section LC wideband matching using the P2D file are plotted in Figure 26. As shown in these figures, the two-stage PA achieved an overall output power improvement across the three bands (3.1 to 4.8 GHz) after the input and output matching. The output power could reach as high as 10.5 dBm at 4 GHz, compared to its original unmatched condition producing an output power of 8.5 dBm. In addition, the input and output return losses and gain are also improved.

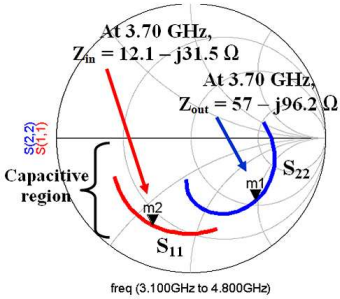

Figure 23. Input and output impedances of the unmatched two-stage PA (3.1 to 4.8 GHz).

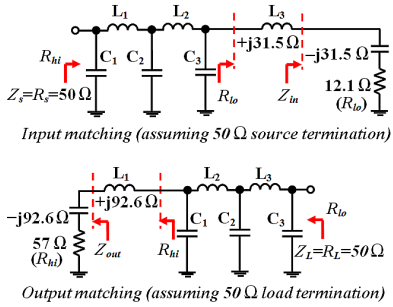

Figure 24. Wideband input and output matching using multi-section LC networks.

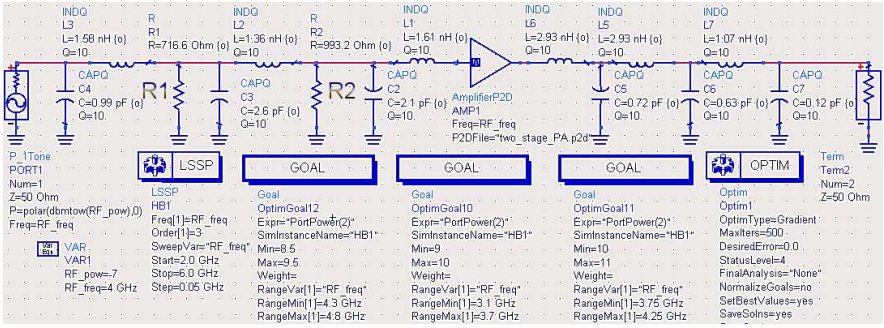

Figure 25. Optimizing the input and output matching towards output power in Agilent ADS.

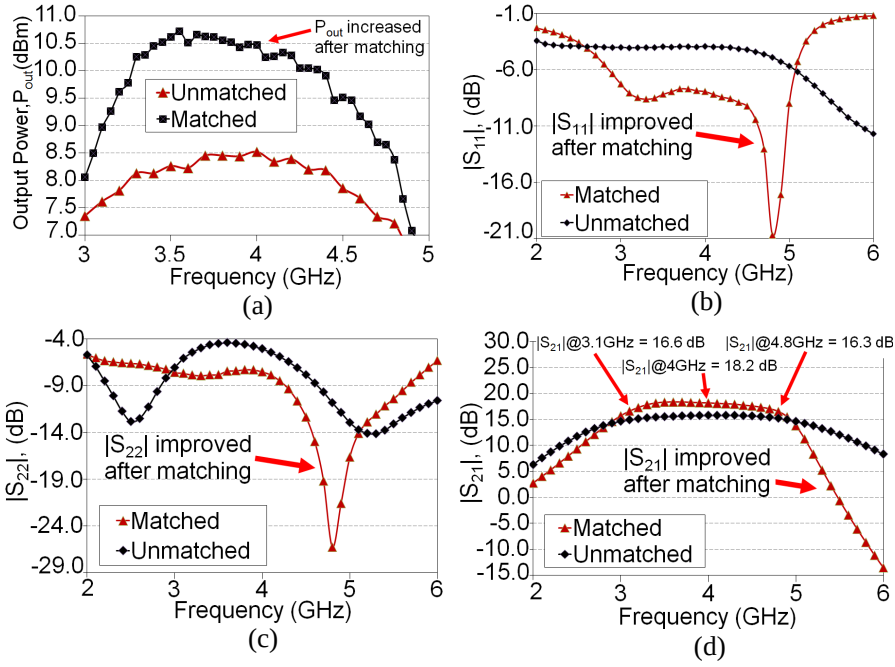

Figure 26. The large-signal performances before and after the multi-section LC wideband matching, simulated using the P2D file with input power, $P_{in} = -7\,\text{dBm}$. (a) Output power, (b) input return loss, (c) output return loss, (d) gain.

5. CONCLUSIONS

A WiMedia compliant 0.18 µm CMOS PA for lower band UWB system (3 to 5 GHz) is systematically designed, simulated and tested in this work. With careful optimization, the output impedance of the driver stage (first stage) is made to fall on the source-pull contours of the second stage amplifier. This has improved the overall efficiency and output power of the two-stage PA. According to the measured results, the proposed two-stage PA has the highest efficiency and output power among the reported UWB PA to date. The multi-section LC input and output matchings are also considered with the measurement based P2D model. In addition, the modulated UWB signal is also inserted into the P2D modeled PAs to determine the characteristic of the modulated signal. Compared to other broadband techniques, the proposed PA has less design complexity with only three main transistors in a two-stage topology and can be used as reference design for immediate UWB PA implementation.

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