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A K-BAND TRANSMITTER FRONT-END BASED ON DIFFERENTIAL SWITCHES IN 0.13-μm CMOS TECHNOLOGY

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Abstract—This paper presents the design and test results of a 20-GHz transmitter front-end implemented in the TSMC 0.13-μm CMOS process. The chip consists of a voltage-controlled oscillator (VCO), an RC phase splitter, and two differential switches. To realize the K-band transmitter function, the two different switches are designed to serve the purpose of frequency doubler and phase modulator, respectively. These two features are verified in the implemented chip and, as a result, the chip can serve as a transmitter front-end. The measured total current consumption of the chip core circuit is 26 mA under a DC supply voltage of 1.2 V. The chip size is $1.03 \times 0.93\,\mathrm{mm}^2$.

1. INTRODUCTION

The microwave band is suitable for delivering data at speeds in excess of Gb/s for ranging, data communication [1], radar applications [2, 3], or medical applications [4]. High carrier frequencies are desirable because they allow smaller antennas [5] and more bandwidth [6] to be used. Although several integrated transmitter solutions using CMOS technology have been proposed for microwave radio system applications [7–9], microwave communication systems based on simpler

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and more compact architectures remain desirable. For integrated circuits operated at the K-band, frequency doubler circuits [10] are important for single-chip solutions. However, for double-balanced quadrature frequency mixing operation of a frequency doubler, the subharmonic mixer [11–13] requires more complex and accurate phase local oscillator (LO) signals than those of a conventional one [14], demanding a high-quality phase shifting network [15, 16] in subharmonically pumped frequency conversion systems. Unfortunately, the use of CMOS for subharmonic mixers in the microwave range has not been extensively investigated. To our knowledge, there are currently no high-performance CMOS subharmonic mixers for applications above 20 GHz. In the present study, a 20-GHz transmitter front-end based on the differential switches is designed. It consists of a voltage-controlled oscillator (VCO) [17, 18], an RC phase splitter, a frequency doubler, and a phase modulator implemented in 0.13-μm CMOS technology. The differential switch pair [19], a component in the double-balanced mixer, is used to multiply the LO signal and the RF signal to achieve very high frequencies. The design and implementation of the differential switches make it possible to realize RF multiplexers, frequency doublers, and modulators/demodulators based on CMOS technology. The differential switch pair is thoroughly investigated and its application in a K-band frequency doubler and a phase modulator is examined.

2. ARCHITECTURE OF THE PROPOSED TRANSMITTER FRONT-END

Figure 1(a) shows the block diagram of the proposed transmitter front-end, which includes a VCO, an RC phase splitter, a frequency doubler and a modulator. It is realized in the TSMC 0.13-μm 1P8M CMOS process. A 10-GHz differential Colpitts VCO, which consists of only PMOS transistors is used in the circuit. The RC phase splitter which operates at half of the desired microwave frequency is attached immediately after the VCO. The RC phase splitter is used for splitting the complementary signals of the VCO into four orthogonal phases. The signals in the four phases are mixed in the first differential switch pair and the working frequency is thus doubled. Finally, the doubled signal is modulated in the second differential switch by the baseband signal. Fig. 1(b) illustrates the frequency doubler waveforms. In this figure, the two input waveforms at LO+ and LO− are of the same frequency, yet with 90-degree phase difference. Through the self-mixing or switching, the frequency of the output waveform is doubled.

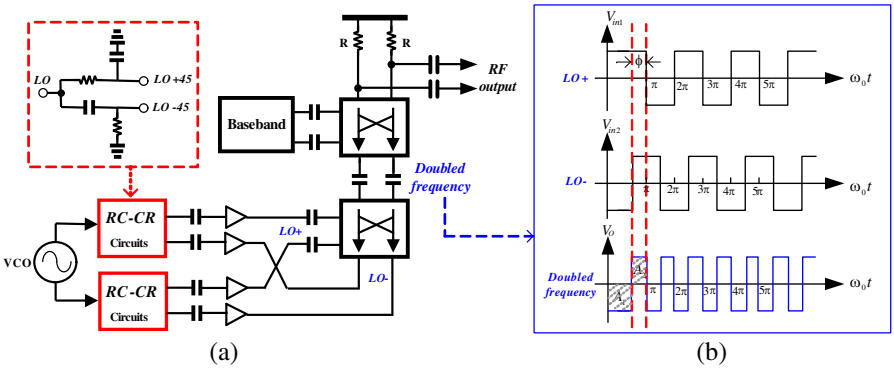

Figure 1. (a) Block diagram of the proposed transmitter front-end. (b) Illustration of the frequency doubler waveforms.

When the input frequency is in the range of 10 GHz, a 20 GHz output frequency can be obtained.

3. ANALYSIS OF DIFFERENTIAL SWITCH

In the paper, the differential switch pair which a component in the double-balanced mixer is used in realizing the functions of frequency doubler and modulation. In the following, the equilibrium circuit of the differential switch is investigated.

3.1. Basics of the Differential Switch

Figure 2 shows a schematic and the symbol of the differential switch. The switch consists of four NMOS transistors and is organized to have two input (V_i, V_{ib}), two output (V_o, V_{ob}), and two control (V_c, V_{cb}) terminals. Fig. 2(b) shows the symbol of the differential switch where the arrows indicate the direction of the internal current flow. The current flows from the output terminal to the input terminal in most applications. The two control voltages V_c and V_{cb} are complementary. When the control voltage V_c is high and V_{cb} is low, the two NMOS transistors M_1 and M_2 are both ON, whereas M_3 and M_4 are both OFF. As a result, the input terminal V_i is connected to the output terminal V_o and V_{ib} is connected to V_{ob}. On the other hand, when V_c is low and V_{cb} is high, the connections are exchanged. By controlling the voltages at the control terminals, the desired frequency doubling and modulation functions can be established.

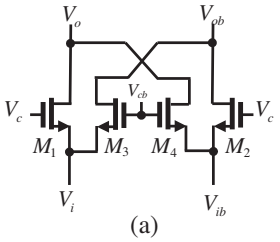

Figure 2. Differential switch, (a) schematic and (b) symbol.

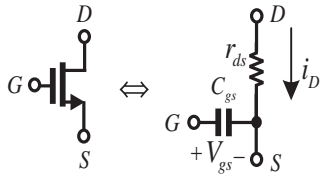

Figure 3. AC equivalent circuit of NMOS transistor in the triode mode.

3.2. Analysis of the Differential Switch in the Triode Mode

As the differential switch consists of four MOS transistors, the operation of each MOS transistor is described. In the design, the MOS transistor is biased in the triode region and can be functionally represented by the equivalent circuit in Fig. 3 which contains an input capacitor (C_{gs}) and a variable resistor (r_{ds}). Let V_{gs} and V_{ds} be, respectively, the voltages across the gate-source terminals and the drain-source terminals. Assume that the threshold voltage of the MOS transistor is V_t, the drain-source current (i_D) of the MOS transistor can be expressed as:

$$i_D = K\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right] \tag{1}$$

where $K = \mu_n C_{ox} W/L$ is the parameter of the NMOS transistor with a mobility of μ_n, an oxide capacitance of C_{ox}, a channel width of W, and a channel length of L. For a MOS transistor working in the triode mode, we have $(V_{gs} - V_t) \gg V_{ds}$. By differentiating (1) and applying this condition to (1), the variable conductance $(1/r_{ds})$ of the MOS transistor can be expressed as:

$$1/r_{ds} = \partial i_D/\partial V_{ds} = K(V_{gs} - V_t) \tag{2}$$

Assume that all MOS transistors (M_1–M_4) are the same, the equivalent circuit of the differential switch circuit of Fig. 2(a) with two loads (Z_L) attached is depicted in Fig. 4. Four sources, V_i, V_{ib}, V_c, and V_{cb} are connected to the four inputs of the circuit. From the figure, the four gate-source voltages of V_{gs1}, V_{gs2}, V_{gs3}, and V_{gs4} are equal to $(V_c - V_i)$, $(V_{cb} - V_i)$, $(V_{cb} - V_{ib})$, and $(V_c - V_{ib})$, respectively.

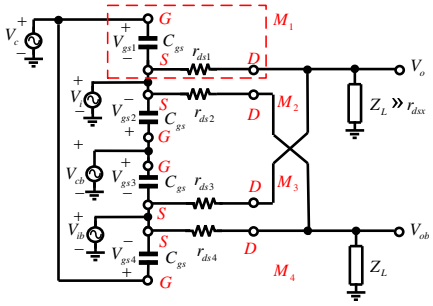

Figure 4. AC equivalent circuit of the differential switch in triode mode. The drain-source resistance is a function of the gate-source voltage which is the core function of the circuit.

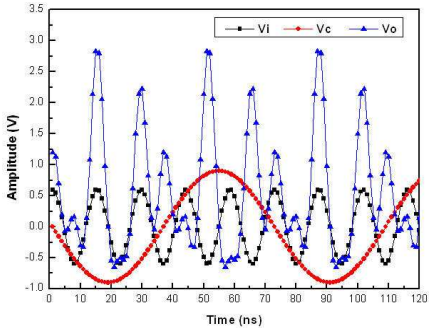

Figure 5. Numerical simulation results of the phase modulation function.

Hence, the four variable resistances of the circuit can be expressed as:

$$\begin{cases} r_{ds1} = [K(V_c - V_i - V_t)]^{-1} \\ r_{ds2} = [K(V_{cb} - V_i - V_t)]^{-1} \\ r_{ds3} = [K(V_{cb} - V_{ib} - V_t)]^{-1} \\ r_{ds4} = [K(V_c - V_{ib} - V_t)]^{-1} \end{cases} \tag{3}$$

The output voltages V_o and V_{ob} are given by

$$\begin{cases} V_0 = \dfrac{r_{ds3}V_i + r_{ds1}V_{ib}}{r_{ds1} + r_{ds3}} \\ V_{0b} = \dfrac{r_{ds4}V_i + r_{ds2}V_{ib}}{r_{ds2} + r_{ds4}} \end{cases} \tag{4}$$

Substituting (3) into (4), the output voltages of the differential switch can be expressed as

$$\begin{cases} V_o = \dfrac{(V_c - V_i - V_t)V_i + (V_{cb} - V_{ib} - V_t)V_{ib}}{V_c + V_{cb} - V_i - V_{ib} - 2V_t} \\ V_{ob} = \dfrac{(V_{cb} - V_i - V_t)V_i + (V_c - V_{ib} - V_t)V_{ib}}{V_c + V_{cb} - V_i - V_{ib} - 2V_t} \end{cases} \tag{5}$$

If the input differential signals are designed such that $V_{ib} = -V_i$ and

$V_{cb} = -V_c$, the output voltages become

$$\begin{cases} V_o = \dfrac{1}{V_t}\left(-V_c V_i + V_i^2\right) \\ V_{ob} = \dfrac{1}{V_t}\left(V_c V_i + V_i^2\right) \end{cases} \tag{6}$$

From (6), it is apparent that V_o and V_{ob} are not exactly complementary, especially in cases when the amplitude of V_i is large. Fig. 5 shows the numerical simulation results of the phase modulation function of the differential switch circuit. The phase of the output signal is either in phase or of opposite phase with respect to the input signal, indicating that the phase modulation function is realized in the circuit.

4. CIRCUIT DESIGN

Figure 6 shows the schematic of the proposed transmitter front-end. As mentioned, the front-end consists of a VCO, an RC phase splitter, and two differential switch pairs. The circuits provide frequency doubling and phase modulation in the microwave frequency range. The phase modulation function is realized through a differential switch which is comprised of four NMOS transistors (M_{11}–M_{14}) in which the baseband (BB) signals and LO signals are mixed to generate the

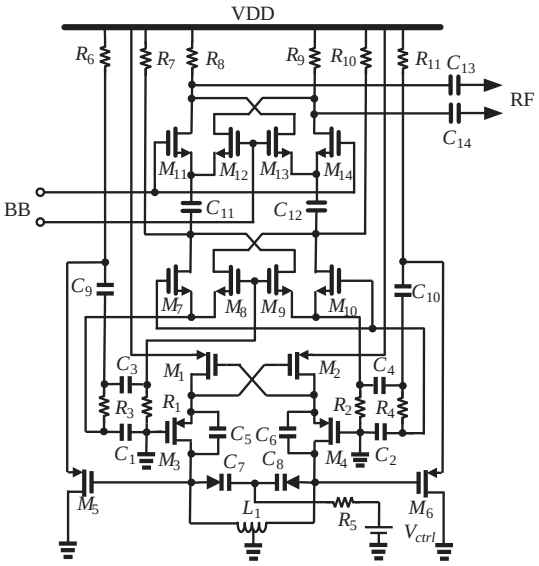

Figure 6. Schematic of the proposed K-band transmitter front-end.

RF output signals. The LO signals are obtained from the frequency doubler which is also realized through a differential switch with four NMOS transistors (M_7–M_{10}). For frequency doubling applications, four resistors (R_1–R_4) and four capacitors (C_1–C_4) are used to separate the complementary signals of the VCO into four orthogonal signals before they are connected to the differential switches. With the frequency doubler, the Colpitts VCO can operate at half of the desired microwave frequency, which allows the oscillator to use the PMOS transistors to enhance phase noise performance. As shown in Fig. 6, the differential Colpitts VCO consists of two PMOS-transistor (M_1, M_2) cross-coupled pairs, two PMOS amplifiers (M_3, M_4), two varactor diodes (C_7, C_8), and one center-tapped on-chip inductor (L_1). The PMOS-transistor cross-coupled pair of the current switch also provides a negative resistance to the Colpitts VCO to improve the oscillating conditions, especially the start-up condition. Conventionally, a transistor constant-current source is needed for biasing a differential VCO structure. The current source works as a DC short circuit to offer a sufficient current to let the differential pair work normally, and also works as a high-AC impedance to avoid a loading effect. However, in the proposed circuit, the differential pair is connected to the V_{DD} node directly as a trade-off between chip size and gain. Without the transistor constant-current source, the bias current is directly controlled by the transistor size. An on-chip symmetrical inductor (L_1) with a center tap is inserted in the VCO to act as a tank circuit.

5. CHIP IMPLEMENTATION AND MEASUREMENT

In the implementation, the PMOS transistors of the current-switch pair (M_1, M_2) have a width and length of 70 µm and 0.13 µm, respectively, which provide a negative resistance for the start-up operation. The amplifiers of two symmetrical single-ended Colpitts oscillators are PMOS transistors M_3 and M_4 with a width and length of 90 µm and 0.13 µm, respectively. Two varactor diodes (C_7, C_8) are selected to be 0.04 pF for zero biasing. Two shunt capacitors (C_5, C_6) are selected to be 0.1 pF. An on-chip symmetrical inductor L_1 with an inductance of 0.62 nH and a center tap is inserted in the oscillators to act as a tank circuit. The RC phase splitters, which are attached immediately after the VCO, are 200 Ω and 0.065 pF to form a corner frequency of around 10 GHz. Two differential switch pairs (M_7–M_{14}) have a width and length of 10 µm and 0.13 µm, respectively. The chip size is $1.03 \times 0.93\,\text{mm}^2$. The total current consumption of the chip, including the modulator and VCO, is 23.9 mA under a DC supply voltage of

1.2 V, as obtained from the simulation.

A photograph of the implemented modulator is shown in Fig. 7. The chip was measured on a probe station without wire bonding, as shown in Fig. 7. A DC power supply, an RF signal generator (R&S SMV100A), and a microwave spectrum analyzer (R&S FSP) were connected to the chip. A DC voltage of 1.2 V was applied to power the chip. The measured total current consumption of the chip core circuit was around 26 mA, which is slightly higher than that obtained from the simulation.

Figure 8 depicts the output spectrum of the frequency doubler. The frequency doubler increased the signal to 19.24 GHz. Fig. 9 shows the measured tuning range and output power of frequency doubler. The oscillation frequency range of the frequency doubler is 19.16 GHz to 19.7 GHz and the output power is −37 dBm to −27 dBm when

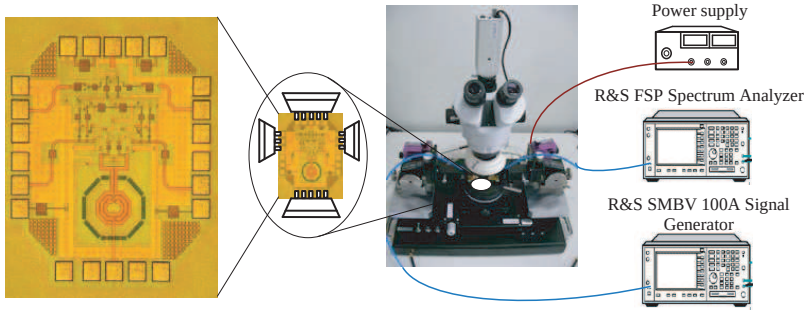

Figure 7. Chip micrograph and measurement of the proposed transmitter front-end.

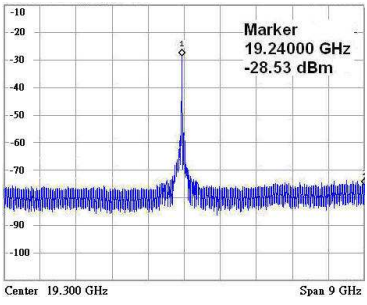

Figure 8. Output spectrum of frequency doubler.

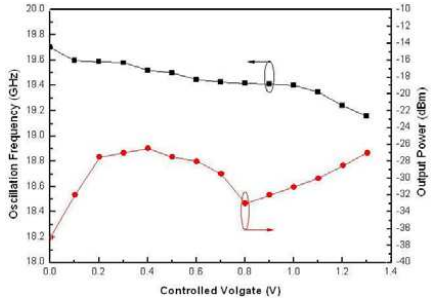

Figure 9. Measured tuning range and output power of frequency doubler.

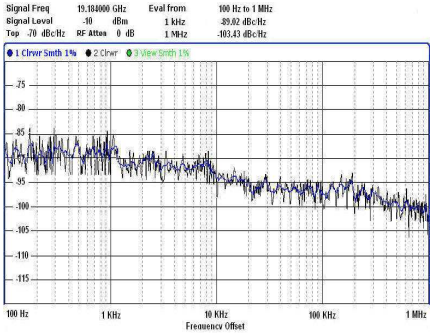

Figure 10. Measured phase noise of frequency doubler.

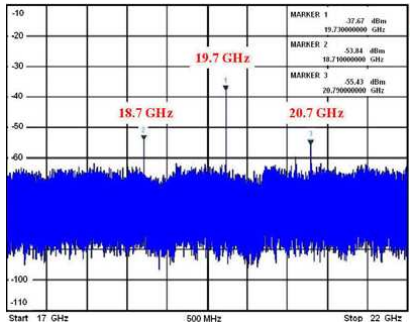

Figure 11. Modulated output spectrum of the modulator at 20 GHz with a 1-GHz baseband signal.

Table 1. Comparisons of transmitter front-ends.

Ref.	Process	Freq. (GHz)	Mod. Bandwidth (GHz)	Topology/ With Internal LO gen.	Tuning Range (MHz)	Core Power Consumption (mW)	Chip Size (mm^2)
[20]	CMOS 0.18 µm	24.15	2.45	single balanced mixer/No	N/A	127.8	1.9×1.9
[21]	SiGe:C 0.25µm	17	0.01	subharmonic mixer/No	N/A	16	0.9×0.7
[22]	GaAs HBT	20-40	1	Gilbert Cell mixer/No	N/A	981	4×3
This work	CMOS 0.13 µm	19.7	1	Gilbert Cell mixer/Yes	540	31.2	1×0.9

the controlled voltage is varied from 0 to 1.3 V. The measured phase noise of the frequency doubler as shown in Fig. 10 is −103.4 dBc/Hz at a 1-MHz offset from the 19.18-GHz carrier. In the modulation measurement, the SMV100A generated a 1-GHz baseband signal and the microwave spectrum analyzer was used to monitor the output of the chip. Fig. 11 shows three peaks in the obtained spectrum, at 18.7 GHz, 19.7 GHz, and 20.7 GHz respectively. The presence of the carrier, upper side band, and lower side band clearly verifies that the modulation function is realized in the chip.

Finally, the implemented K-band transmitter front-end is

compared with some reported literatures in Table 1. The proposed chip is the only one which includes an internal LO generator. The power consumption and the chip size of it are still superior to others.

6. CONCLUSION

An architecture of a 20-GHz transmitter front-end implemented in the TSMC 0.13-μm CMOS process was proposed. Two differential switches, an RC phase splitter and a VCO are realized in the circuit design. The differential switches are employed in the transmitter for frequency doubling and modulation. The working mechanism of the differential switch pair was investigated in detail. The differential switch pair is shown to be feasible for the implementation of a K-band transmitter front-end. The measurement results confirm that the chip transmits the modulated signal up to 20 GHz. The proposed transmitter front-end due to its simple architecture and CMOS process implementation can potentially be used in microwave transmitter applications.

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