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STUDY OF FRACTAL-SHAPED STRUCTURES WITH PIN DIODES USING THE MULTI-SCALE METHOD COMBINED TO THE GENERALIZED EQUIVALENT CIRCUIT MODELING

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Abstract—A multi-scale (MS) approach combined to the generalized equivalent circuit (GEC) modeling is applied to compute the input impedance of pre-fractal structures with incorporated PIN diodes. Instead of treating the whole complex problem at once, the MS method splits the complex structure into a set of scale levels to be studied separately. The computation is done gradually from the lowest level. Each scale level is artificially excited by N modal sources to compute its input impedance matrix. The MS method is based on converting this input impedance matrix into an impedance operator to achieve the transition toward the subsequent level. The PIN diodes were easily integrated in the MS approach thanks to their surface impedance model. The main advantage of the MS-GEC method is the significant reduction of the problem's high aspect ratio since fine details are studied separately of the larger structure. Consequently, the manipulated matrices are well conditioned. Moreover, the reduced size of matrices manipulated at each level leads to less memory requirement and faster processing than the MoM. Values obtained with the MS-GEC approach converge to those given by the MoM method when a sufficient number of modal sources are used at each scale level. For frequencies between 1 GHz and 6.8 GHz, the agreement between the two methods is conspicuous.

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1. INTRODUCTION

Since 1975 when Benoit Mandelbrot has defined fractals for the first time [1], many new shapes and applications for fractals continue to emerge [2]. The most well known examples are fractal-shaped antennas and frequency selective surfaces [3, 4]. Recently, PIN Diodes were integrated in active FSSs to obtain tunable frequency response and superior performances compared to conventional structures [5–9]. Since such structures combine fine details within large dimensions, uniform and adaptive spatial grid-based approaches (Finite Element Method, Transmission Line Matrix Method or Finite Difference Time-Domain Method) have been used. However, the need to finely grid the entire computational domain results in very long solution time and important memory resources. For planar structures, the Moment (MoM) method [10] remains interesting since it is employed in many electromagnetic simulators. However, when the structure's complexity increases, the requirements (processing time and memory storage) are important and the convergence is delicate to reach. To circumvent the difficulties encountered with the above listed methods, a scale changing technique (SCT) has been developed in [11–13]. Its key idea is to dissociate the initial complex structure into scale levels separating then fine details from larger dimensions. For each scale level, a Scale Changing Network (SCN) is determined. The transition from the lowest scale level to the highest one is done by cascading the SCNs of the various scale levels.

Another technique called the renormalization approach has been developed to treat the case of fractals at infinite scale [14–17]. It is a powerful technique since the solution consists of a recurrent relationship relating the lower scale to the one at infinite.

In this paper, we present the MS-GEC method and its advantages when applied to study complex structures and especially pre-fractal objects with incorporated PIN diodes offering tuneable characteristics. The MS-GEC consists of a multi-scale approach (MS) combined to the generalized equivalent circuit (GEC) modeling. Its main idea is to dissociate the complex structure into scale levels to be studied separately. The incorporated PIN diodes have been easily integrated in the approach thanks to their surface impedance model. For each scale level, a surface impedance matrix is computed and then converted to an impedance operator who facilitates the derivation of the integral equations describing the problem. The transition is done gradually from a scale level S_i toward the subsequent level S_{i+1} via the impedance operator of scale level S_i. When the structure complexity increases, the described MS-GEC method guarantees a significant gain in the

processing time and memory resources while preserving results close to those obtained by the MoM approach.

The paper is organized as follows: Section 2 describes the generalized equivalent circuits' concept. The multi-scale approach is detailed in Section 3. The MS-GEC method will be applied in Section 4 to some pre-fractal structures with incorporated PIN diodes; The PIN diode modeling and the surface impedance operator derivation are detailed. Section 5 presents the obtained numerical results compared to those of the Moment method. A comparison between MoM and MS-GEC in term of processing time and memory resources is performed in Section 6.

2. DESCRIPTION OF THE GEC APPROACH

The concept of generalized equivalent circuits [18–20] is based on the representation of the integral equations by an equivalent circuit in order to alleviate the resolution of Maxwell's equations. This electromagnetic representation made it possible to extend the Kirchhoff laws generally employed with the (V-I) concept to the Maxwell formalism (E-H).

The generalized test functions which describe the electromagnetic state on the discontinuity interface are modeled by an adjustable virtual source not storing energy. The environment of the studied structure is expressed by an admittance (or an impedance) operator. The excitation is depicted within the GEC using a field source or a current source.

2.1. THE ADJUSTABLE VIRTUAL SOURCES

Lets S be a surface where the continuity conditions of the investigated electromagnetic field have to be checked. Based on the field properties, the surface S can be written as $S = S_{01} \cup S_{02}$ where S_{02} is the sub-domain on which the field is null, S_{01} is the complementary sub-domain where the field remains not null. This electromagnetic state may be depicted by a virtual source defined over S_{01} and being null elsewhere. In fact, a virtual source indicates by definition a non null vector quantity on a domain included in S and whose dual size is null in this domain. As an example, let consider a surface S consisting of an insulating part S_{01} and a metallic part S_{02}. As well known, the conditions $\vec{E} \neq \vec{0}$ and $\vec{J} = \vec{0}$ are verified on the S_{01} sub-domain. The dual condition $\vec{E} = \vec{0}$ and $\vec{J} \neq \vec{0}$ is established on the complementary domain S_{02}. The first condition can be represented by a virtual field source while the second condition corresponds to a virtual current source as depicted respectively in Figs. 1(a) and 1(b).

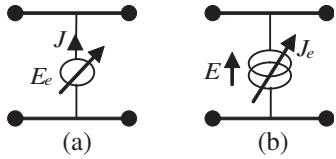


Figure 1. Symbolic notation of virtual sources: (a) field source; (b) current source.

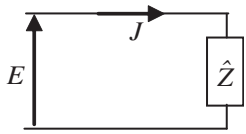


Figure 2. Representation of the impedance operator.

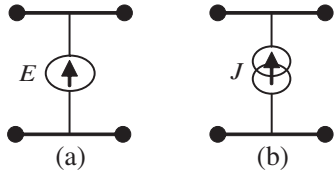


Figure 3. Symbolic notation of excitation sources: (a) field source, (b) current source.

2.2. THE ADMITTANCE OPERATOR

The admittance operator is used to compute the current $\vec{J}$ on an oriented surface S when the tangential field $\vec{E}$ is known. The impedance operator shown in Fig. 2 is used to compute the tangential field $\vec{E}$ when the current distribution $\vec{J}$ on the considered surface is known. The relation between $\vec{E}$ and $\vec{J}$ classically takes the form of the ohm's law: $\vec{E} = \hat{Z}\,\vec{J}$ or $\vec{J} = \hat{Y}\,\vec{E}$. The impedance and admittance operators are presented on a modal basis. Their detailed expressions will be provided in Section 4.2. The unique definition of these operators rises from the unicity of the $(\vec{E}, \vec{H})$ or $(\vec{E}, \vec{J})$ solution on the surface S.

2.3. THE EXCITATION SOURCES

The excitation sources are the fundamental modes of the guides leading to the discontinuity surface. The symbolic notation of the modal excitation is given either by a field modal source, or by a current modal source as shown respectively in Figs. 3(a) and 3(b). These excitation sources are called real since they deliver power into the guide.

3. DESCRIPTION OF THE MULTI-SCALE APPROACH

The multi-scale approach is based on decomposing the initial complex problem into elementary sub-problems: the total structure is split into sub-structures having almost the same dimensions; these sub-structures are partitioned again to smaller ones until the smallest dimension (called the generator pattern for pre-fractal structures) is reached. At each step, a scale level S_i is defined (Fig. 4). Lets attribute scale level $S = 1$ to the generator pattern and scale level $S = S_{\max}$ to the total structure. Once partitioned, the problem resolution starts by computing the surface impedance matrix of the generator pattern. For that, the considered level needs to be enclosed along its contour with artificial boundary conditions. Therefore, the local modal basis of the considered scale level is known and can be decomposed into two types of modes: active modes and passive modes.

The second step is to artificially excite the studied scale level with N active modes in order to determine its surface impedance matrix. Next, this surface impedance matrix is converted to a surface impedance operator which will ensure the transition to the next scale level. To determine the surface impedance matrix of the subsequent level, we replace the domain of the previous level by its impedance operator and we follow the same steps as before. The same processing will be repeated till the highest level.

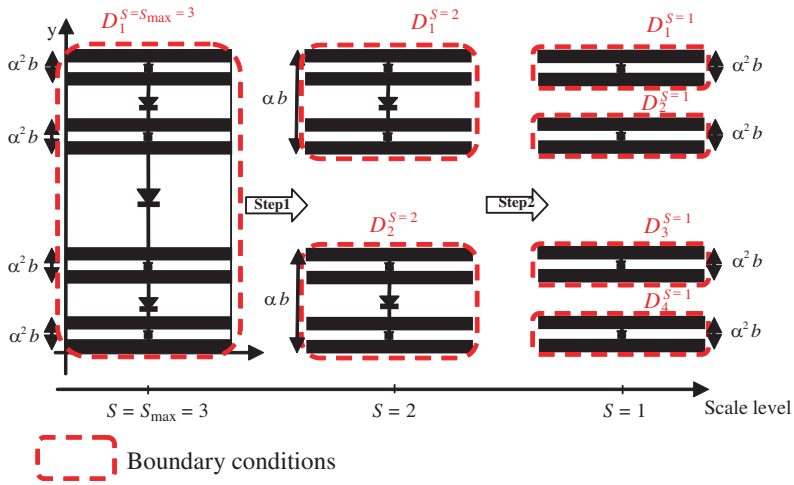


Figure 4. Partitioning of the pre-fractal structure at the 3rd stage of growth.

3.1. Choice of Boundary Conditions

The boundary conditions are defined on the contour of each sub-structure. The conventional ones are: a) Periodic boundaries, b) Perfect Electric boundaries (PE), c) Perfect Magnetic boundaries (PM), or d) Combination of PE and PM boundaries. Any one of these modal basis can be used since they are equivalent. However, a better one can be chosen based on some criteria such as accuracy, rapidity and numerical convergence. The more the modal basis respects the electromagnetic state of the real structure, the more it is adequate.

3.2. DEFINITION OF ACTIVE AND PASSIVE MODES

A modal basis is composed of two sets of modes: lower-order modes known as active modes, and higher-order modes called passive modes. Passive modes are spatially localized and then useful to express abrupt variations near and within discontinuities. On the other hand, lower-order modes are used to describe the electromagnetic coupling between scale levels. For that, a sufficient number of active modes are required for a better computation of the coupling and to guarantee a transition between levels with minimum error.

4. THE MS-GEC METHOD APPLIED TO PRE-FRACTAL STRUCTURES WITH INCORPORATED PIN DIODES

In this paper, the MS-GEC approach is used to compute the input impedance of the pre-fractal structures depicted Fig. 5. They consist of Nb perfect metallic strips with negligible thickness printed on a lossless dielectric and related by PIN diodes. These structures are located in the cross section of a parallel plates EMEM waveguide: two perfect electric boundary conditions to the top and the bottom, lateral conditions are magnetic.

The steps needed to compute the input impedance of the structure depicted Fig. 5(b) using the MS-GEC method are detailed in Fig. 6. The impedance operator $\hat{Z}_{si}$ is a linear representation of the surface impedance matrix of scale level S_i. Its detailed expression will be provided in Sections 4.2 to 4.4.

Before starting the computation for the various scales, we need to model the PIN diodes in order to include them in the GEC models.

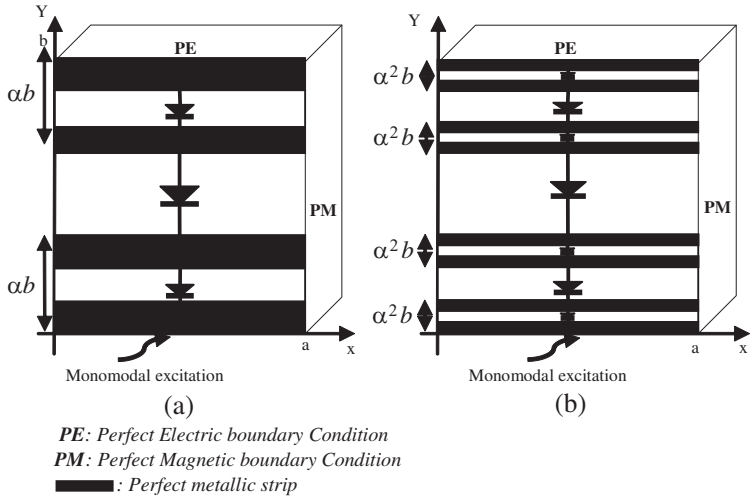
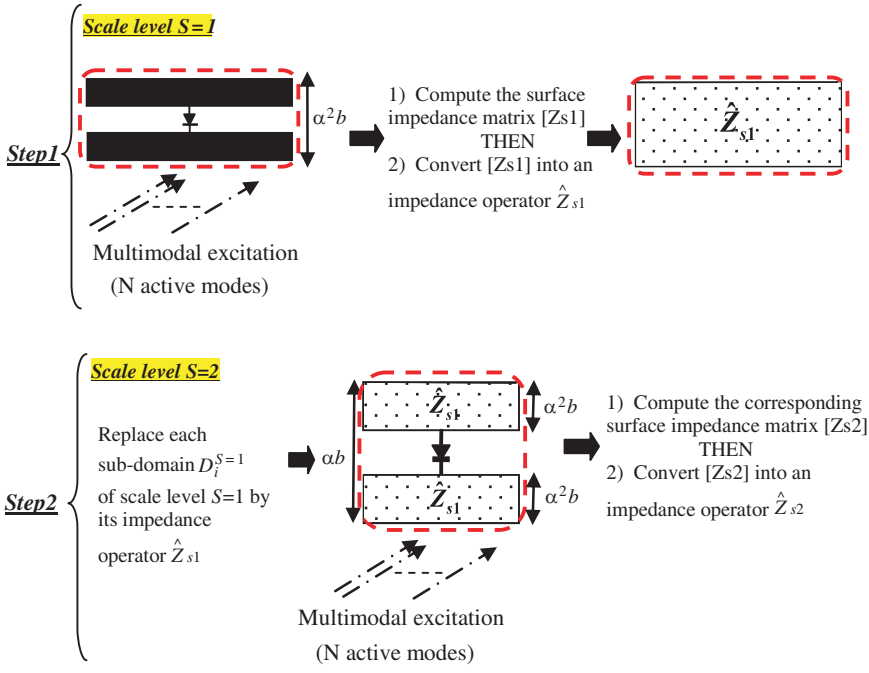


Figure 5. Pre-fractal structures at: (a) the 2nd, (b) the 3rd stages of growth.



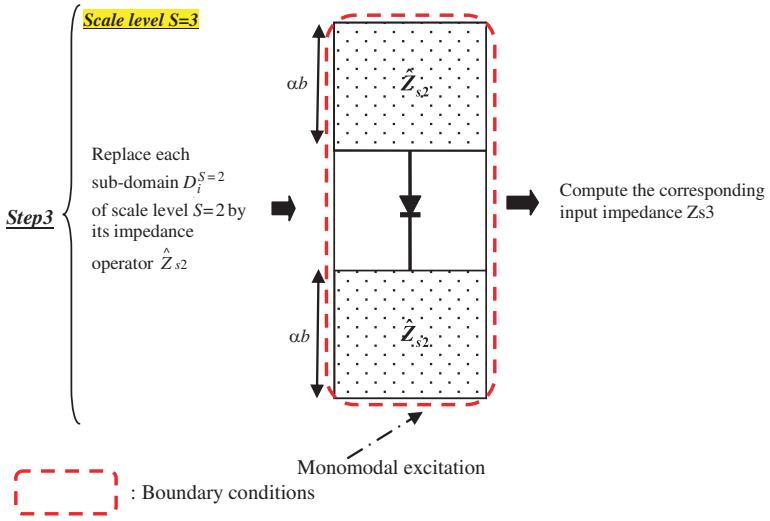


Figure 6. Steps of the MS-GEC approach: case of a pre-fractal structure at the 3rd stage of growth with incorporated PIN diodes.

4.1. PIN DIODE MODELLING

The PIN diodes integrated in the studied structures are modeled using the equivalent circuit models [8] presented Fig. 7. The forward and the reverse bias equivalent circuits are shown in Figs. 7(a) and 7(b).

Figure 7(c) presents a reverse bias equivalent circuit converted to a series RLC circuit. In this paper, the values used for forward bias are $R = 5\,\Omega$ and $L = 0.4\,\text{nH}$. For reverse bias, a capacitance $C = 0.27\,\text{pF}$ is added.

According to its ON/OFF state, each PIN diode can be replaced by a surface impedance ZD of width w and height d expressed using its intrinsic (R, L, C) characteristics. In fact, ZD is an equivalent representation of the diode impedance Z when considering the relation between E and J derived from the relation between V and I for the TEM mode.

$$\begin{cases} E = \frac{V}{d} \\ J = \frac{I}{w} \\ E = ZD\ J \\ V = Z\ I \\ Z = \begin{cases} (R + jL\omega) : \text{forward bias} \\ \left(R + jL\omega - \frac{j}{C\omega}\right) : \text{ reverse bias} \end{cases} \end{cases}$$

$$\Rightarrow ZD = \begin{cases} \frac{w}{d}(R + jL\omega) : \text{forward bias} \\ \frac{w}{d}\left(R + jL\omega - \frac{j}{C\omega}\right) : \text{ reverse bias} \end{cases} \quad (1)$$

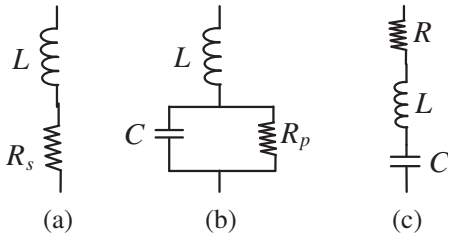


Figure 7. The PIN Diode (a) forward bias equivalent circuit, (b) reverse bias equivalent circuit, (c) reverse bias equivalent RLC circuit [8].

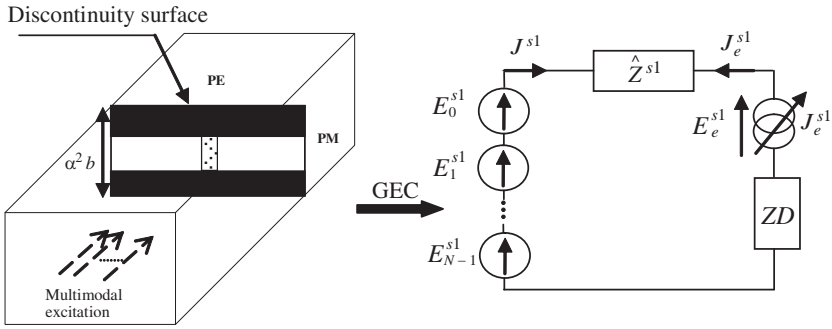


Figure 8. The generator pattern and its equivalent circuit.

4.2. SURFACE IMPEDANCE MATRIX OF THE FIRST SCALE LEVEL

Lets consider the sub-structure of scale level 1 depicted Fig. 6. Based on the equivalent circuit models of Fig. 7, each PIN diode has been replaced by its equivalent surface impedance ZD expressed as given by (1).

We choose to enclose the considered sub-structure by EMEM boundary conditions: two perfect electric boundaries to the top and the bottom, lateral boundaries are perfect magnetic. Due to the structure symmetry with regard to the discontinuity surface, only the half of the generalized equivalent circuit is needed [20]. The simplified GEC is depicted in Fig. 8.

Lets $\left(f_{mn}^{s1}\right)$ be the local modal basis of the EMEM waveguide enclosing the generator pattern. $E_i^{s1} = V_i^{s1} f_i^{s1}$ are the excitation modal sources where $f_i^{s1}, i \in [0 \ldots N-1]$ represent the active modes

of level $S = 1$. The impedance operator $\hat{Z}^{s1}$ is expressed as a function of the higher-order modes $\langle f^{s1}_{m,n}|$ and their modes' impedances $z^{s1}_{m,n}$ [20].

$$\hat{Z}^{s1} = \sum_{\substack{m,\,n \\ (m,n) \neq \text{actifs}}} |f^{s1}_{m,n}\rangle \; z^{s1}_{m,n} \, \langle f^{s1}_{m,n}| \tag{2}$$

ZD stands for the diode surface impedance localized in the diode domain. The problem's unknown J^{s1}_e is expressed as a series of known test functions g^{s1}_p weighted by unknown coefficients x^{s1}_p. J^{s1}_e exists on the metallic and the diode domains and is zero on the lossless dielectric domain. When applied to the circuit depicted in Fig. 8, the generalized Kirchhoff and ohm laws lead to the equations system (3).

$$\begin{cases} J^{s1} = -J^{s1}_e & \text{(3a)} \\ E^{s1}_e = E^{s1}_0 + E^{s1}_1 + \ldots + E^{s1}_{N-1} + \left(\hat{Z}^{s1} + ZD\right) J^{s1}_e & \text{(3b)} \end{cases}$$

The Equation (3a) can be interpreted as the continuity relation of the current on the discontinuity surface. The Equation (3b) expresses the continuity relation of the field at the discontinuity surface.

A formal relation between sources (real and virtual) and their duals is then deduced.

$$\begin{pmatrix} J^{s1} \\ E^{s1}_e \end{pmatrix} = \begin{bmatrix} 0 & -1 \\ 1 & \left(\hat{Z}^{s1} + ZD\right) \end{bmatrix} \begin{pmatrix} E^{s1} \\ Je^{s1} \end{pmatrix} \tag{4}$$

Next, we apply the Galerkin method to the system (4), the surface impedance matrix $[Z_{S1}]$ of scale level 1 is expressed by (5).

$$[Z_{S1}] = \frac{1}{2}\left([A] \;\; [Z]^{-1} \;\; [A]^T\right)^{-1}$$

where

$$A\,(i,p) = \left\langle f^{s1}_i \;\middle|\; g^{s1}_p \right\rangle, \quad Z\,(p,q) = \left[\left\langle g^{s1}_p \;\middle|\; \left(\hat{Z}^{s1} + ZD\right) g^{s1}_q \right\rangle\right] \tag{5}$$

Once computed, the surface impedance matrix $[Z_{S1}]$ is converted to a surface impedance operator $\hat{Z}_{S1}$. In fact, the matrix representation $[Z_{S1}]$ can be written in a linear form as an operator since the modal basis is orthogonal.

The conversion of the surface impedance matrix $[Z_{S1}]$ into an impedance operator is performed as expressed in (6).

$$\hat{Z}_{S1} = \sum_{i=1}^{N} \sum_{j=1}^{N} |f^{s1}_{i-1}\rangle \, Z_{S1}\,(i,j) \, \langle f^{s1}_{j-1}| \tag{6}$$

$\left(f^{s1}_i\right)_{i\in[0,N-1]}$ are the N active modes used as artificial excitation modal sources at scale level $s = 1$.

4.3. SURFACE IMPEDANCE MATRIX OF THE SECOND SCALE LEVEL

Lets consider now the second step of the MS-GEC method illustrated Fig. 6. As done before, the PIN diode was replaced by its equivalent surface impedance ZD. The structure to be studied and its corresponding GEC are presented in Fig. 9. Note that the used GEC is simplified since we have taken into account the structure symmetry with regard to the discontinuity surface.

$\hat{Z}^{s2}$ is the impedance operator of scale level 2 relating to its higher-order modes. However, $\hat{Z}_{S1}$ is the surface impedance operator deduced from the surface impedance matrix of the previous scale level ($S = 1$).

The surface impedance matrix $[Z_{S2}]$ of scale level 2 is obtained by a similar development as done for scale level $S = 1$.

$$[Z_{S2}] = \frac{1}{2}\left([A]\ [Z]^{-1}\ [A]^T\right)^{-1}$$

where

$$A(i,p) = \left\langle f_i^{s2} \middle| g_p^{s2} \right\rangle, \quad Z(p,q) = \left[\left\langle g_p^{s2} \middle| \left(\hat{Z}^{s2} + \hat{Z}_{S1} + ZD\right) g_q^{s2} \right\rangle\right] \quad (7)$$

4.4. INPUT IMPEDANCE OF THE THIRD SCALE LEVEL ($S = S_{max}$)

The third scale level corresponds to the highest level since the considered structure is at the third stage of growth. To compute its input impedance, only one excitation source is used. The equivalent

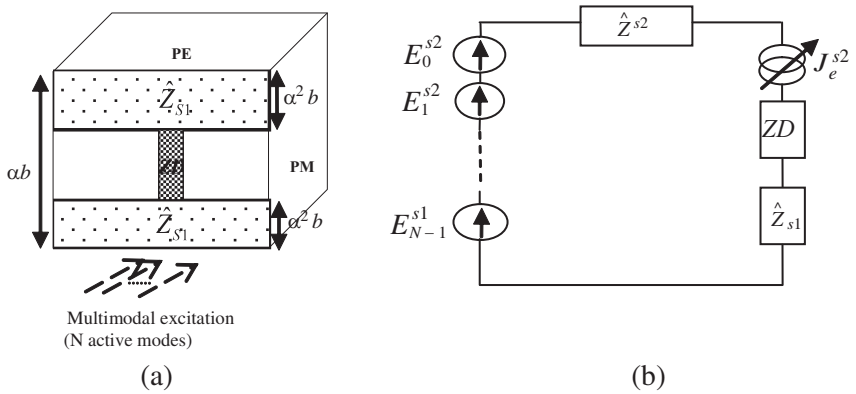


Figure 9. (a) The equivalent structure at scale level 2, (b) its simplified GEC.

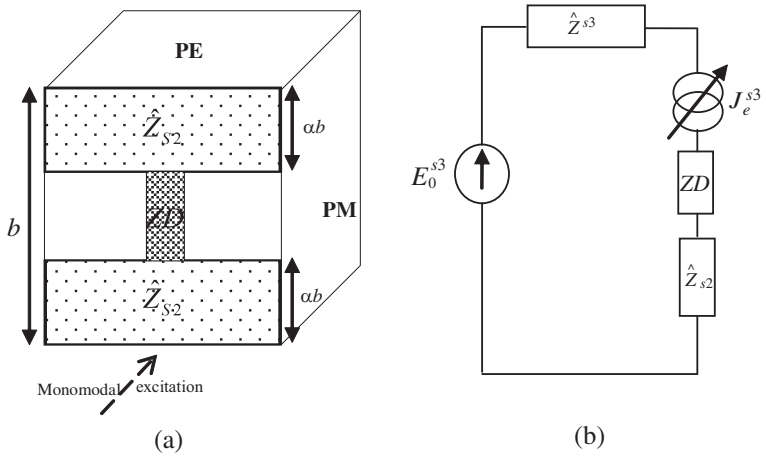


Figure 10. The third scale level: (a) structure with surface impedance operator, (b) simplified GEC.

structure is obtained by replacing the previous scale level 2 by its surface impedance operator $\hat{Z}_{S2}$. The simplified GEC is as depicted in Fig. 10.

The input impedance of the total structure using the multi-scale approach is given by (8).

$$Z_{IN\_MS} = Z_{S3} = \frac{1}{2} \quad \frac{1}{[A]\ [Z]^{-1}\ [A]^T}$$

where

$$A(1,p) = \left\langle f_0^{s3} \middle| g_p^{s3} \right\rangle, \quad Z(p,q) = \left[\left\langle g_p^{s3} \middle| \left(\hat{Z}^{s3} + \hat{Z}_{S2} + ZD \right) g_q^{s3} \right\rangle \right] \quad (8)$$

For validation purposes, the results obtained by the multi-scale approach were compared to those of the moment method.

5. VALIDATION OF NUMERICAL RESULTS

The results validation will be performed for the two structures depicted in Fig. 5. Firstly, the input impedance has been computed using the MoM and the MS-GEC methods at 2.45 GHz. Next, a study of the mismatch between the two methods is performed for frequencies ranging between 1 GHz and 6.8 GHz. Lets $\xi = 100 \times \frac{Z_{IN\_MoM} - Z_{IN\_MS}}{Z_{IN\_MoM}}$ (%) be the relative error between the input impedance Z_{IN_MoM} given by the moment method and Z_{IN_MS} computed by the MS-GEC method.

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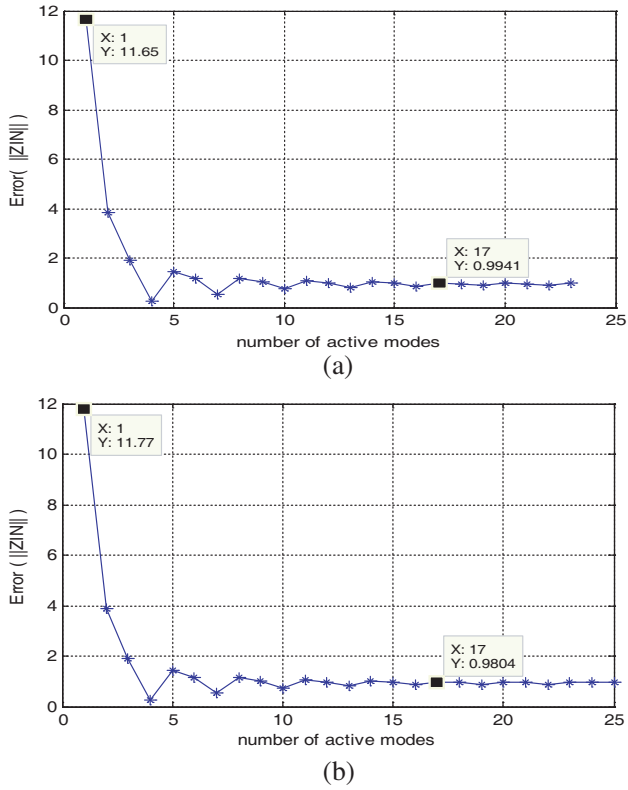

Figure 11. Variation of the relative error (%) with the number of active modes: the structure is at the 2nd stage of growth (Fig. 5(a)); (a) the PIN diode state is ON; (b) the PIN diode state is OFF; $f = 2.45\,\text{GHz}$, $a = 10.2\,\text{mm}$, $b = 22.9\,\text{mm}$, $\alpha = 1/3$, $w = 0.5\,\text{mm}$.

Figure 11 presents the variation of the relative error with the number of active modes at lower scale levels for the structure Fig. 5(a). Using one active mode at lower scale levels, we notice that the relative error is important. For example, if we consider the pre-fractal structure at the 2nd stage of growth shown in Fig. 5(a), the error on the input impedance is about 12%.

This important mismatch between the MoM and the MS method is due to the inability of one active mode to fully describe the coupling between subsequent scale levels. By adding more active modes at lower scale levels, the error decreases. With more than 17 active modes, the relative error is less than 1% whether the diode state is ON or OFF.

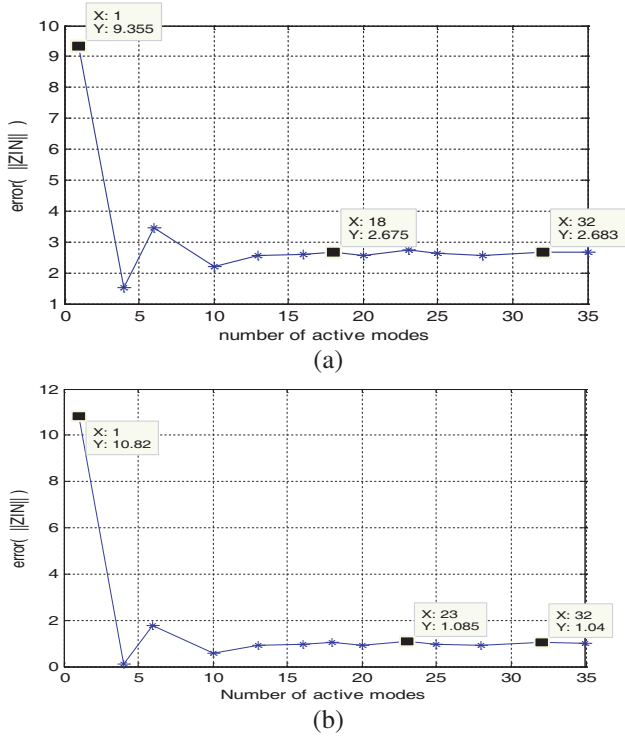

Figure 12. Variation of the relative error (%) with the number of active modes: the structure is at the 3^{rd} stage of growth (Fig. 5(b)); (a) the PIN diode state is ON; (b) the PIN diode state is OFF; $f = 2.45\,\text{GHz}$, $a = 10.2\,\text{mm}$, $b = 22.9\,\text{mm}$, $\alpha = 1/3$, $w = 0.5\,\text{mm}$.

Figure 12 shows the error variation relating to the input impedance of the pre-fractal structure at the third stage of growth depicted Fig. 5(b). At 2.45 GHz, the relative error convergence is studied by increasing the number of active modes at lower scale levels. When the number of excitation sources is sufficient, the relative error is less than 2.7% when the PIN diodes are ON and is less than 1.1% when PIN diodes are OFF.

The error convergence is reached with more than 25 active modes. Consequently, a better transition from a scale toward another can be performed if the coupling is accurately computed.

We notice that the error between the MS and MoM methods has increased when the structure contains more levels. In fact, for the first structure, only one transition between scale levels has been performed while the second structure requires two transitions. The

error estimation of the surface impedance operator at each level will be accumulated leading then to a little increase of the mismatch between MS and MoM approaches. However, for the two studied structures, the error remains less than 2.7%.

For further validation, the input impedance was computed for frequencies ranging between 1 GHz and 6.8 GHz. Based on the relative error variation with the number of active modes done in the previous section, we choose to artificially excite all the lower scale levels with 28 active modes.

Figures 13 and 14 show that the values of the input impedances found using the multi-scale method coincide with those given by the MoM method. The agreement between the two methods is obvious.

The moment method was applied to the structures depicted in Fig. 5. The distribution of the normalized diffracted field is as shown in Fig. 15. We verify that the boundary conditions are respected. In fact, the field is null on the Perfect metallic strips and on the diodes domains. It is not null elsewhere. Consequently, since the boundary conditions are verified, we proved the exactitude of the moment method that we have implemented.

We notice also the existence of the Gibbs effect due to the important value of the field localized at the interface between each diode domain and the neighbouring metallic strips. In fact, these interfaces are characterized by an abrupt and important variation of the field leading then to a more remarkable Gibbs effect. Indeed, it reflects the difficulty in approximating a discontinuous function by a finite series of continuous waves.

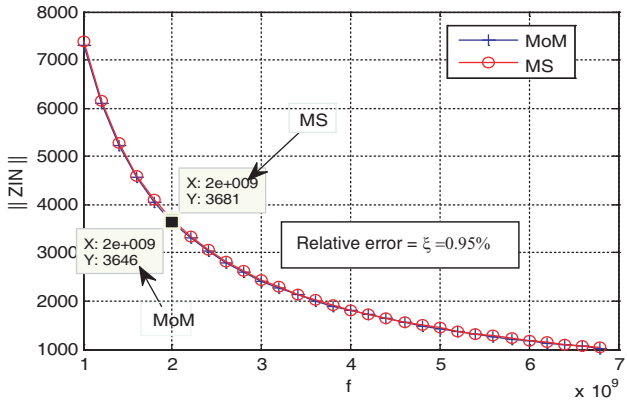

Figure 13. Variation of the input impedance with the frequency, the structure is at the 2nd stage of growth; The PIN diodes state is ON. $a = 10.2\,\text{mm}$, $b = 22.9\,\text{mm}$, $\alpha = 1/3$, $w = 0.5\,\text{mm}$.

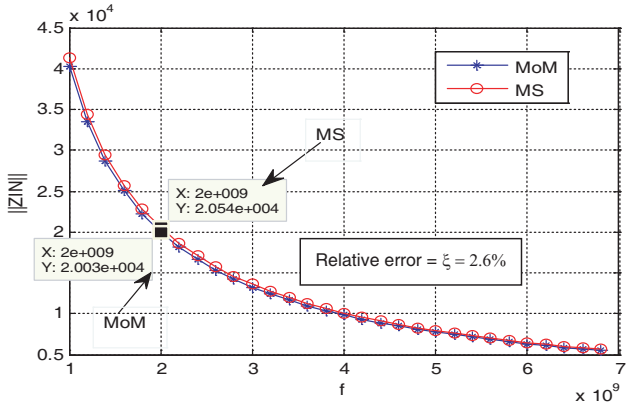

Figure 14. Variation of the input impedance with the frequency, the structure is at the 3rd stage of growth; The PIN diodes state is ON. $a = 10.2\,\text{mm}$, $b = 22.9\,\text{mm}$, $\alpha = 1/3$, $w = 0.5\,\text{mm}$.

6. EXECUTION TIME AND MEMORY RESOURCES NEEDED BY MOM AND MS-GEC METHODS

The MS-GEC method is very interesting when applied to fractal-shaped structures since it guarantees an appreciable gain in term of CPU time and memory resources. To prove that, lets define the needed time to compute the input impedance using the MoM method and the MS-GEC method. The parameters used are the following:

- T_S: Mean time to compute the scalar product $\langle g_p, f_n \rangle$.
- T_c: Mean time needed for an elementary operation of multiplication/addition.
- $T_i(q)$: Mean time needed to invert a $(q \times q)$ matrix.
- N_f: Number of auto-similar elements in the generator pattern: in our case, the generator pattern contains 2 auto-similar perfect metallic strips and so $N_f = 2$.
- p: Number of trial functions per element in the generator pattern. (We suppose that this number is the same for diodes and strips).
- N: Number of modes in the modal basis.
- Na: Number of active modes used at lower scale levels.

In the case of fractal structures with PIN diodes at scale level k, the number of total auto-similar elements is N_f^k. The number of PIN diodes is $(N_f^k - 1)$. Consequently, the total number of trial functions is: $p(2N_f^k - 1)$.

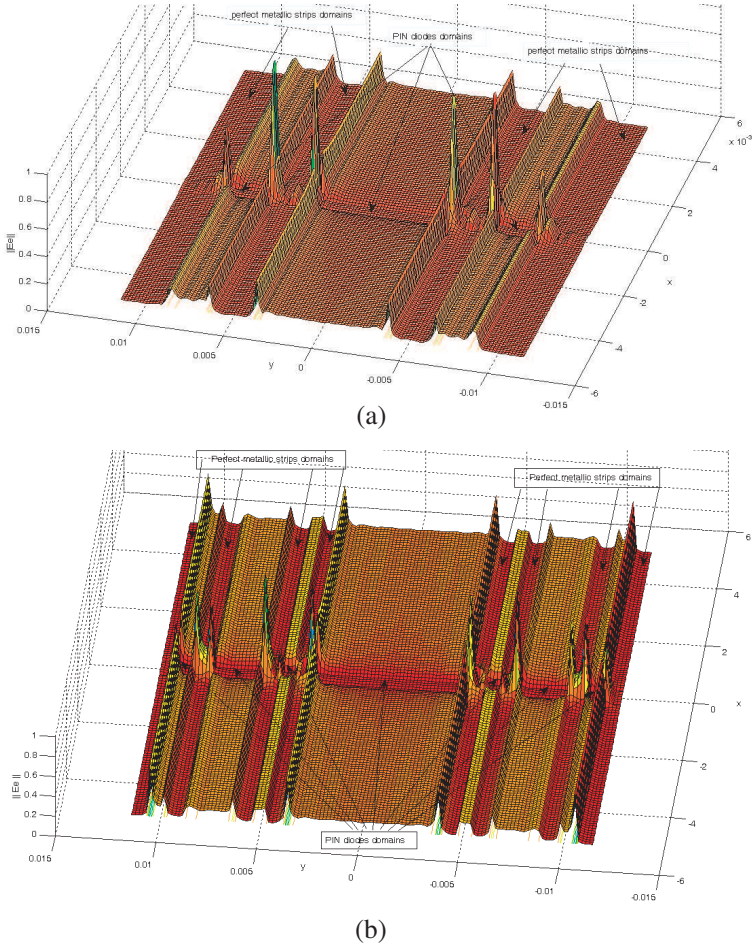

Figure 15. Distribution of the vertical component of the normalized diffracted field, PIN Diode state ON, (a) structure at the 2nd stage of growth, (b) structure at the 3rd stage of growth, $a = 10.2\,\text{mm}$, $b = 22.9\,\text{mm}$, $\alpha = 1/3$, $w = 0.5\,\text{mm}$.

Lets T^k_{MoM} be the total time needed by the MoM method to compute the input impedance of the pre-fractal structure with PIN diodes at scale level k.

$$T^k_{MoM} = \left[N\left(p\left(2N^k_f - 1\right)\right) + p^2\left(N^k_f - 1\right)\right] \times T_S + \left[(N+1)\left(p\left(2N^k_f - 1\right)\right)^2 + p\left(2N^k_f - 1\right)\right] \times T_c + T_i\left(p\left(2N^k_f - 1\right)\right) + \delta(9)$$

δ is a term which expresses the neglected residue including for example the time for filling matrices.

When the scale k increases, the processing time will increase exponentially making of the MoM method very time consuming. In addition, the manipulated matrices are $\left[p\left(2N_f^k-1\right)\times p\left(2N_f^k-1\right)\right]$ requiring then huge memory resources when k increases.

Lets T_{MS}^k be the total time needed by the MS method to compute the input impedance of the pre-fractal structure with PIN diodes at scale level k.

$$\begin{aligned} T_{MS}^k = &\left[N\left(p\left(2N_f-1\right)\right)+p^2\left(N_f-1\right)+Na\left(p\left(2N_f-1\right)\right)\right]\times T_S \\ &+\left[\left(N+Na+2\right)\left(p\left(2N_f-1\right)\right)^2+p\left(2N_f-1\right)\right]\times T_c \\ &+T_i\left(p\left(2N_f-1\right)\right)+T_{MS}^{k-1}+\delta \end{aligned} \tag{10}$$

At each iteration of the MS method, we deal with a structure composed of two strips (perfect conductors or surface impedance operators) and a PIN diode. Each level needs

$$\begin{aligned} &\left[N\left(p\left(2N_f-1\right)\right)+p^2\left(N_f-1\right)+Na\left(p\left(2N_f-1\right)\right)\right]\times T_S \\ &+\left[\left(N+Na+2\right)\left(p\left(2N_f-1\right)\right)^2+p\left(2N_f-1\right)\right] \\ &\times T_c+T_i\left(p\left(2N_f-1\right)\right) \quad \text{CPU time.} \end{aligned}$$

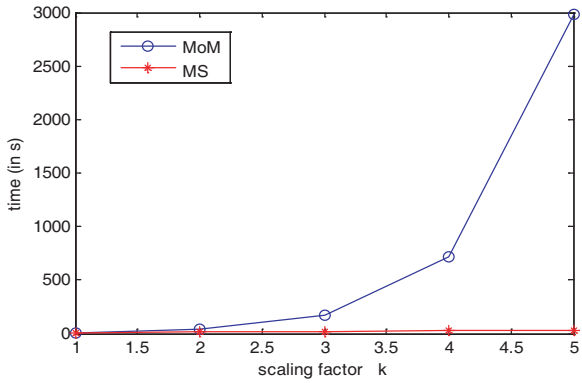

Figure 16. Variation of the processing Time with the scaling factor k.

The recursive expression (10) can be reduced as given in (11)

$$T_{MS}^{k}=k\begin{bmatrix}\left[N(p\,(2N_f-1))+p^2(N_f-1)+Na(p\,(2N_f-1))\right]\times T_S\\ +\left[(N+Na+2)\,(p\,(2N_f-1))^2+p\,(2N_f-1)\right]\times T_c\\ +T_i\,(p\,(2N_f-1))\end{bmatrix}+\delta \quad (11)$$

As expressed in (9) and (11) and shown in Fig. 16, it is obvious that the MS method uses a CPU time which varies linearly with the scaling factor k contrary to the MoM which varies exponentially with k. Moreover, the manipulated matrices are $[p\,(2N_f-1)\times p\,(2N_f-1)]$ which need reduced memory storage resources compared to the MoM.

7. CONCLUSION

In this paper, we have applied the multi-scale approach combined to the generalized equivalent circuit modeling to study some pre-fractal structures with incorporated PIN diodes. The importance of active modes to model the coupling between subsequent scale levels was investigated. In fact, we proved that a sufficient number of active modes have to be used at the lower scale levels to improve the multi-scale results accuracy compared to the moment method.

The MS method is based on the generalized equivalent circuit modeling. For that, the PIN diodes have been easily integrated in the MS approach thanks to their surface impedance model computed based on their intrinsic characteristics, their width and height.

To validate the MS approach, numerical results were compared to those of the MoM method for frequencies ranging between 1 GHz and 6.8 GHz. The developed method seems to be very interesting when applied to fractal-shaped structures since it guarantees an appreciable gain in term of CPU time and memory resources.

In further work, the PIN diode will be used as a semiconductor in order to take into consideration the physical characteristics of the PIN diode. Moreover, the MS-GEC will be extended by being combined to the renormalization approach in order to be applied to fractal structures with PIN diodes at infinite scale.

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