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WIDEBAND ON-CHIP K-BAND RF FRONT-END FOR VEHICULAR FMCW RADAR APPLICATIONS IN 0.18 μm CMOS PROCESS

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Abstract—In this paper, we present a wideband on-chip K-band RF front-end including a transmitter and receiver for vehicular FMCW radar applications using 0.18 μm CMOS process. To achieve wideband performance, an RC feedback circuit is applied to the input stage of amplifiers, as well as wideband passive circuits such as Marchand type baluns and Wilkinson type power dividers to the mixer LO port and transmitter output, respectively. The designed chip shows a 3-dB bandwidth of 6 GHz and 4.8 GHz for the receiver and transmitter, respectively. The receiver represents a gain of 18 dB and an input-referred 1 dB compression point of −9 dBm at an RF frequency of 24.15 GHz and an IF frequency of 100 kHz. The transmitter shows a power gain of 8.9 dB and an output power of 6.8 dBm at a frequency of 24.15 GHz. The total chip has a size of 1500 μm × 1270 μm while consuming 71 mA with a supply voltage of 1.8 V. Further, the designed RF front-end chip has been verified by radar performance tests such as the Doppler shift and range information. The test result for range information shows good agreement with theoretical expectations.

1. INTRODUCTION

Research on vehicular radars has been actively progressing in order to improve driver safety and convenience. This research has been further accelerated due to frequency allocation for vehicular radar applications at 24 GHz [1]. Such radars are used for short range applications, e.g., blind spot detection, near collision warning, and

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lane change support. The Federal Communications Commission (FCC) and European Telecommunications Standards Institute (ETSI) have allocated bandwidths of 200 MHz and 100/250 MHz, respectively, for narrow band applications [1–3].

Many papers have published K-band front-ends using Si CMOS technology [4–8]. Initially, a 24 GHz RF front-end was proposed in 2004 [4]. The proposal showed a receiver including a low noise amplifier (LNA) and a mixer with both high gain and low noise figure. The researchers [5] proposed a 24–27 GHz UWB phased array transmitter with a variable phase ring oscillator and phased lock loop. Subsequently, a 22–29 GHz UWB pulse-radar receiver front-end was proposed in 2007 [6]. The UWB front-end consisted of an LNA, a mixer, a variable gain amplifier, a pulse former, and a voltage controlled oscillator. In 2008 and 2009, researchers introduced 24 GHz receiver front-ends [7, 8]. The proposal [7] included a 24 GHz CMOS passive subharmonic mixer/downconverter for zero-IF applications. The researchers [8] compared receiver front-ends using active and passive mixers. Moreover, other RF front-ends have been examined such as in [9, 10]. According to literature, most researchers have designed K-band RF front-ends by means of 0.13 μm CMOS technology. Although, such technology demonstrates superior 91 and 108 GHz f_T and $f_{\max}$ [11] for K-band circuit design, process cost remains quite high. For low cost and high frequency design, only few researchers [4, 6] have employed 0.18 μm CMOS technology, utilizing f_T and $f_{\max}$ (< 60 GHz). The paper [4] showed firstly K-band design possibility using the process. And the paper [6] have improved K-band RF front-end design, which has high integrated structure and superior performance.

In this paper, we present an on-chip RF front-end for vehicular frequency modulated continuous-wave (FMCW) radar applications using 0.18 μm CMOS process. The RF front-end design is focused on achieving wideband performance. This performance can mitigate frequency shift by external interconnection with chips or equipment for assembly or testing. To verify the designed chip, on-wafer chip tests and radar experiments have been performed and analyzed.

2. RF FRONT-END ARCHITECTURE

The K-band RF front-end block diagram is shown in Figure 1. The RF front-end is designed for FMCW radars, available for short range applications. The receiver of the RF front-end consists of a low noise amplifier (LNA), a mixer and a low pass filter (LPF). The transmitter composed of a drive amplifier (DA) and a power divider (PD). In

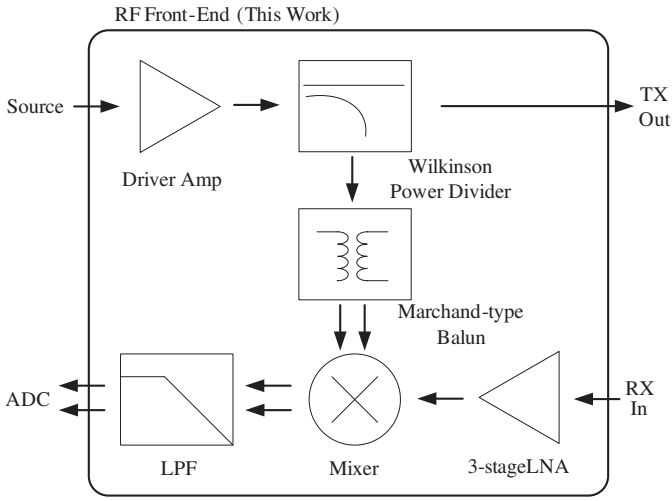


Figure 1. Block diagram of the proposed K-band RF front-end.

the RF front-end, the PD and balun with wideband performance are applied to the transmitter output and the mixer local oscillator (LO) port, respectively. Applied power into the transmitter input is divided to the transmitter output and the mixer LO port by means of the PD. The DA plays a role in mitigating VCO power and supplementing PD power loss. The first stage of the receiver consists of the LNA to minimize noise figure (NF). The Mixer and LPF are placed at the next stage of the LNA. The LPF is used for reducing noise bandwidth which affects to minimum sensitivity of the RF front-end. All RF ports of the RF front-end are matched to $50\,\Omega$ for easy inter-connection with available commercial chips and RF equipment.

3. RF FRONT-END CIRCUIT DESIGN

3.1. LNA with RC Shunt Feedback Circuit

The designed LNA schematic, shown in Figure 2, consists of a three-stage cascade structure with low NF and moderate gain. Each LNA stage has a common source configuration and the input stage is matched to $50\,\Omega$ by LC components C_p, C_{b1}, C_g, and L_g, shunt RC feedback components R_f and C_f, source degeneration inductor L_{s1}, and MOSFET M_1. The shunt RC feedback components are applied between the gate and the drain of M_1 for wideband matching. The input small-signal equivalent circuit including the feedback resistor is

shown in Figure 3, in which ac coupling capacitors C_{b1} and C_f and small pad parasitic capacitor C_p are neglected for simplification. The approximate Q-factor of the circuit shown in Figure 3 is as follows [12]

$$Q \approx \frac{1}{\left(R'_S + \omega_T L_{s1} + \frac{\left(\omega_0 L_g - \left(\frac{1}{\omega_0 C'_g} \right) \right)^2}{R_{fM}} \right) \omega_0 C_{gs1}} \tag{1}$$

where R'_s is $R_s/(1+\omega_0^2 C_{gs1}^2 R_s^2)$, ω_T is the cutoff frequency of M_1, L_{s1} is the source inductor of M_1, ω_0 is the resonant frequency, L_g is the gate inductor of M_1, C'_g is $(1+\omega_0^2 C_{gs1}^2 R_s^2)/\omega_0^2 C_{gs1} R_s^2$, R_{fM} is the Miller equivalent resistance of R_f, and C_{gs1} is the gate-source capacitance of M_1. In general, the Q-factor of RLC resonant circuits is inversely proportional to fractional bandwidth. From (1), proper feedback resistor values result in a low Q-factor. Thus, wideband input matching can be implemented by feedback resistor configuration.

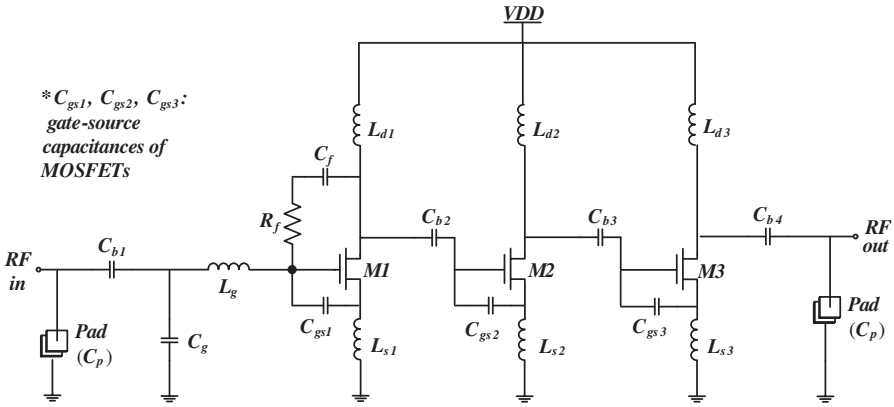


Figure 2. Three-stage K-band LNA schematic.

The input shunt capacitor C_g of the LNA provides flexibility for further improved input matching by the cost of added noise factor. However, the added noise factor can be mitigated by increasing current consumption. The parasitic capacitance C_p of the input pad is considered as an impedance matching component for accurate simulation. The measured value is about 20 fF with a pad size of 50 µm × 50 µm. The source degeneration inductor L_{s1} of M_1 is used for linearity improvement and simultaneous power and noise matching [13]. For inter-stage matching, high pass filter combinations $L_{d1} - C_{b2}$ and $L_{d2} - C_{b3}$ are applied with source inductors L_{s2} and L_{s3}

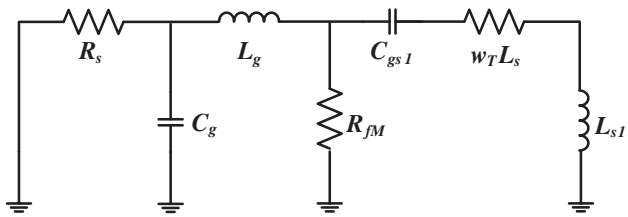


Figure 3. Small-signal equivalent models of input matching network of the proposed LNA.

between the drain outputs and the gate inputs of MOSFETs. The 2nd stage of the LNA is optimized to obtain high gain by a gate voltage of 0.7 V and an M_2 size of 40 µm × 4. For high linearity, the power matching is applied to the last stage of the LNA, which can improve the sensitivity of radar systems. All passive devices used in the LNA were verified by simulations and measurements to guarantee millimeter-wave band operation, i.e., up to 40 GHz. All component values used in the LNA are presented in Table 1. The simulated and measured S-parameter and NF results of the designed LNA are shown in Figure 4. The frequency shift between simulation and measurement results can be caused by the mismatch of inductor models and parasitic effects in the layout. The maximum gain shows 12.7 dB at 24 GHz, and the NF presents 5.3 dB at the same frequency.

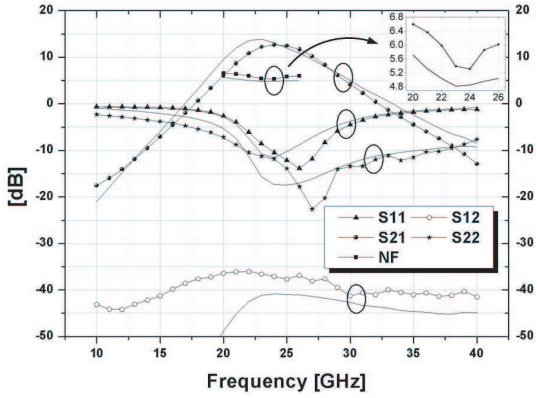


Figure 4. Simulated (line) and measured (symbol) results for S-parameter and NF of the designed LNA.

Table 1. Device values used for LNA design.

Parameters	Value
C_{b1}	740 fF
C_g	210 fF
L_g	200 pH
L_{s1}, L_{s2}, L_{s3}	50 pH
R_f	11 Ω
C_f	20 fF
C_{b2}, C_{b3}	950 fF
C_{b4}	610 fF
L_{d1}, L_{d2}	100 pH
L_{d3}	160 pH
M_1, M_2	40 μm × 4
M_3	32.5 μm × 5

3.2. Marchand Type Balun

The Marchand type balun is applied to the mixer LO port not only for single-ended to differential port conversion, but obtainment of wide bandwidth, as well. Ensuring low insertion loss, as well as low phase and amplitude imbalance, Marchand type baluns are generally smaller than Lange couplers and rat-race baluns [14]. The designed balun layout is shown in Figure 5, which is symmetrical with respect to the longitudinal direction. The S_{21} and S_{31} expression in Marchand type baluns is as follows [15]

$$S_{21} = -S_{31} = -C \times T + \frac{T^3 \times C}{1 + C^2} \tag{2}$$

where C and T are the coupled and transmitted scattering parameters, respectively, of the coupled line. Equation (2) shows a phase difference of 180° and the same amplitude loss, even though Si CMOS process has lossy substrate. The designed balun is composed of a pair of coupled spiral inductors and slot pattern ground as shown in Figure 5. For wideband operation, a ground was applied at the balun to reduce the Q-factor of the inductors. However, the ground also lowers the self-resonance frequency of the inductors [13]. This effect limits the maximum operation frequency of the balun. To solve this problem, we applied the slot pattern ground at the balun. The balun provides a

bandwidth of 54.5% (18.4–32.2 GHz) for amplitude imbalance less than 1 dB and phase imbalance less than 5° while satisfying 10 dB return loss and 5 dB insertion loss [16].

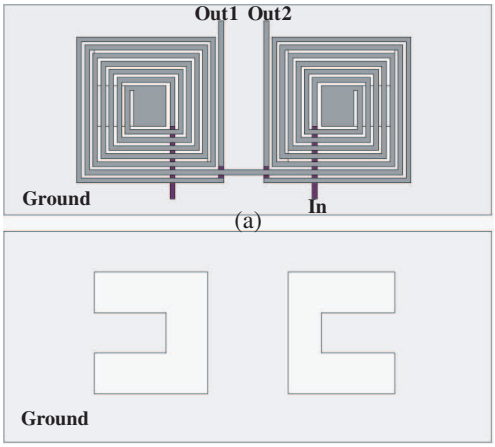


Figure 5. Structure of the proposed Marchand type balun. (a) Full structure of the balun. (b) Detailed slot pattern ground structure.

3.3. Single Balanced Mixer with Marchand Type Balun

The designed mixer has the active single balanced topology as shown in Figure 6. Such topology can reduce a required LO power than a passive topology [8]. The RF trans-conductance stage is designed by LC ladder matching network using RLC combinations, e.g., C_{b1}, L_g, R_g, C_g, C_{gs}, and L_s to obtain a wide bandwidth of 50 Ω. The equivalent circuit of the RF trans-conductance stage is similar to the LNA input circuit in Figure 3. Therefore, the RF trans-conductance stage can achieve wideband performance via proper device values as presented in Table 2. The designed balun is applied to the LO port as an impedance matching network. The impedance of the LO port is as follows

$$Z_{LO} = Z_{in,balun} + \frac{2(C_{b2} + C_p)}{sC_{b2}C_p} \tag{3}$$

where $Z_{in,balun}$ is the input impedance of the balun, C_{b2} and C_{b3} are the ac coupling capacitors of the LO stage, and C_p is the gate-source capacitance of M_2 and M_3. From (3), the real-term is determined by the resistance value of the balun and the imaginary-term is determined by the reactance value of the balun and capacitance values C_p and C_{b2}

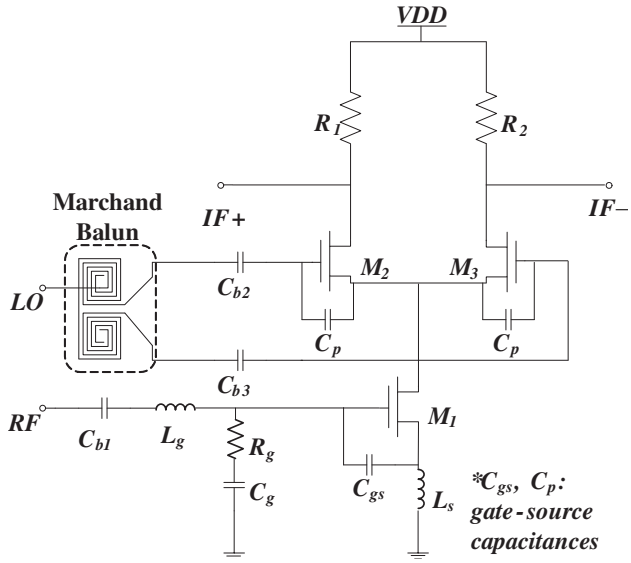


Figure 6. K-band single balanced mixer with balun.

Table 2. Device values used for mixer design.

Parameters	Value
C_{b1}	950 fF
L_g	530 pH
R_g	156 Ω
C_g	50 fF
L_s	1.5 nH
C_{b2}, C_{b3}	950 fF
R_1, R_2	480 Ω
M_1	122.5 μm
M_2, M_3	100 μm

of the mixer. If the imaginary-term is removed by being designated as zero by proper capacitance values, the LO port will show 50 Ω matching for wideband. Even though only capacitance values have limitation for good matching, they achieve reasonable return loss of less than −8 dB at a wide bandwidth of 20–30 GHz.

3.4. Wilkinson Type Power Divider

As a wideband power divider for power division to the transmitter output and balun input, Wilkinson topology is applied to the DA output. In general Wilkinson power dividers with symmetrical structures have wideband performance [17] and can be designed by the micro-strip lines or the coplanar waveguides (CPW) [18, 19]. However, the CPW structures have low flexibility for various small configurations such as curved or meandered lines.

The proposed power divider consists of slow-wave structures such as meandered micro-strip line, slot pattern ground, and metal bridges, which the detailed geometry of the proposed PD is shown in Figure 7. Such slow-wave structures are applied to the power divider for small size. A $\lambda/4$ transformer line of $70.7\,\Omega$ between the input and output port and an isolation resistor of $100\,\Omega$ between the output ports are selected for $50\,\Omega$ matching, good isolation, and equal power division. However, the $\lambda/4$ transformer in CMOS technology is considered as several millimeters long due to a low dielectric constant of SiO_2 ($\varepsilon_r = 3.9$) layer. Hence, the meandered line structure is selected as transmission lines. Moreover, the slot pattern ground with periodic rectangular patterns is applied under the line. The slow-wave effects

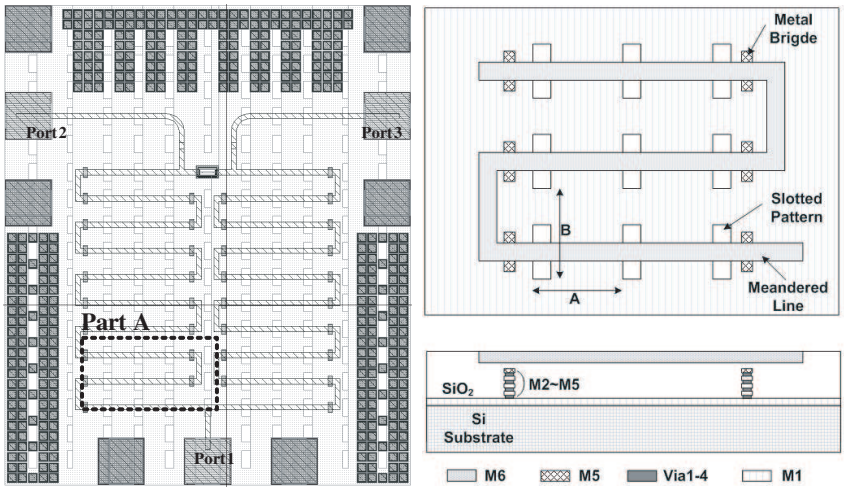


Figure 7. The proposed K-band power divider with slow-wave structure. (a) Proposed Wilkinson power divider layout. (b) Enlarged geometry of part A.

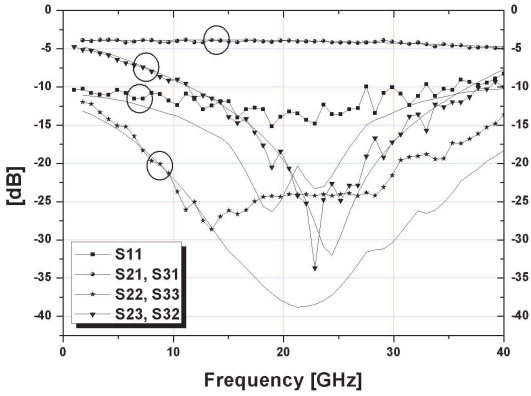


Figure 8. Simulated (line) and measured (symbol) S-parameter results of the designed power divider.

by the slot pattern ground can reduce the size of the power divider. However, this structure is limited in reducing the size of the power divider via design rules such as minimum line space and width. To mitigate the problem, the metal bridges are applied between the line and slot pattern ground. The metal bridges increase the capacitance of the line, and this capacitance, together with the inductance of the line causes the slow-wave effect by a periodic structure. As a result, the metal bridges reduce the size of the power divider even more. The designed PD, compared to one with an identical size and a meandered line design without a slot pattern ground and metal bridges, shows an improved slow-wave factor (SWF) of 8.2%. The SWF equation is as follows

$$SWF = \beta/\kappa_0 \tag{4}$$

where β and κ_0 are the phase constant and wave-number, respectively. The designed PD achieves an insertion loss of 1.3 dB and an isolation of 15 dB at frequencies ranging from 17 to 31 GHz. The simulated and measured S-parameter results of the PD are shown in Figure 8. Although, the measured results present degraded performance than the simulation results, similar trends between the results are achieved.

3.5. Driver Amplifier and Active RC Low Pass Filter

The driver amplifier at the RF front-end is placed in front of the PD as shown in Figure 1. The DA requires a maximum output power of 7 dBm to satisfy transmitter output and mixer LO pumping power. Because this power is not high, the designed LNA is used for the DA.

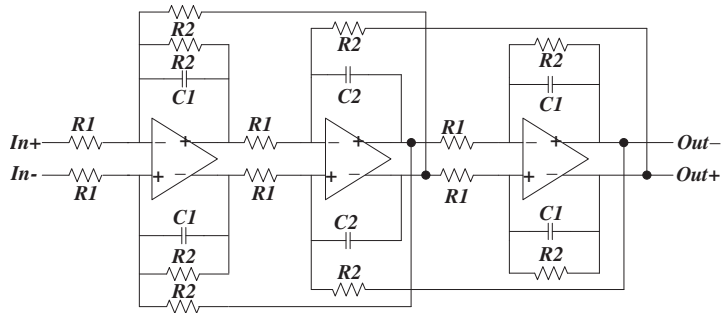


Figure 9. Active low pass filter topology.

The LPF is designed using the active RC topology as shown in Figure 9, which has a simple structure and low power consumption. The 3-stage LPF has a 3-dB cutoff frequency of 2 MHz and a slope of −60 dB/decade, which the characteristic can process IF frequencies up to 2 MHz. However, for long range radar applications, narrowband low-pass filters are required to improve signal to noise ratio (SNR).

4. MEASUREMENT RESULTS

4.1. On-wafer Chip Tests

The chip micrograph of the designed RF front-end is shown in Figure 10 and total chip size is 1500 µm × 1270 µm. The transmitter and receiver circuits are placed on the top and bottom, respectively, of the chip micrograph. The RF signal pads were designed for GSG (ground signal ground) probe types with a pitch of 100 µm. The IF and DC pads were designed for wire bonding. To prevent noise injection into RF circuits, grounds with dummy metals which consist of a poly and six metal layers, were filled in spare space in the chip layout. The designed chip was assembled on an RF substrate in a metal package with silver paste. All measurements of the chip were performed by on-wafer probing. Figure 11(a) shows the simulated and measured transmitter and receiver gain, as well as receiver NF. The measured transmitter power gain shows 8.9 dB at a frequency of 24.15 GHz and a 3-dB bandwidth of 4.8 GHz (21.7–26.5 GHz). The receiver gain was measured at a fixed IF frequency of 100 kHz and RF frequency at 20–30 GHz with a transmitter input power of −7 dBm. The measurement result shows a gain of 18 dB at an RF frequency of 24.15 GHz, and the 3-dB bandwidth presents 6 GHz at 20.7–26.7 GHz. The receiver NF was measured using "Gain Method" due to a low IF frequency of

100 kHz. A minimum NF of 8 dB is achieved at 24 GHz as shown in Figure 11(a). The isolation performance from the transmitter output to the receiver input presents less than −30 dB at 20–30 GHz as shown in Figure 11(b). The simulated isolation performance achieves less than −60 dB, which is not shown in Figure 11(b). Two poles at 22 and 26 GHz are caused by the isolation performance of the PD and the

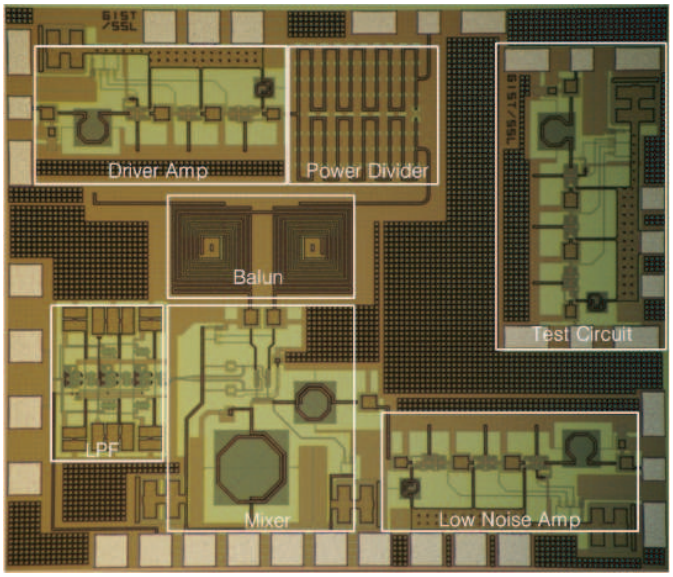


Figure 10. Photograph of the RF front-end chip.

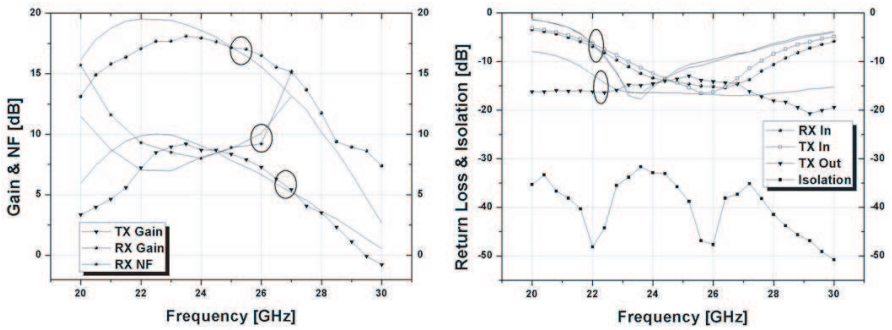


Figure 11. Simulated (line) and measured (symbol) gain, NF, return loss, and isolation of the RF front-end. (a) Gain and NF. (b) Return loss and isolation.

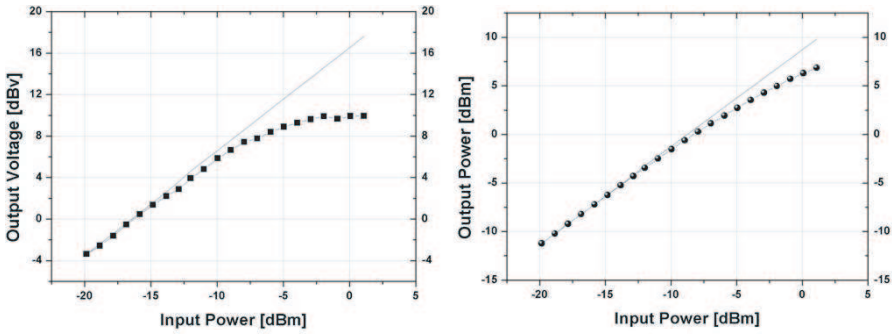


Figure 12. Measured 1-dB compression point of the RF front-end. (a) Receiver 1-dB compression point. (b) Transmitter 1-dB compression point.

Table 3. Comparison of 24 GHz CMOS RF front-end chip.

Parameter	[4] 0.18 µm CMOS	[7] 0.13 µm CMOS	[8] (Acitve) 0.13 µm CMOS	This work 0.18 µm CMOS
Integration	LNA + Mixer	LNA + Mixer + Buffer	LNA + Mixer	LNA + Mixer + LPF + DA + PD + Balun
Frequency (GHz)	21.8	23.1	24	24.15
3 dB BW (GHz)	–	–	–	RX: 6 (20.7–26.7) TX: 4.8 (21.7–26.5)
RX/TX Gain (dB)	RX: 27.5	RX: 3.2	RX: 16	RX: 18 TX: 8.9
RX IP1 dB (dBm)	−23	−12.7	−24.6	−9
DSB NF (dB)	7.7	10	5	8
Current (mA)	43	8.5	14.8	71
Area (mm^2)	0.2	0.58	0.5	1.9

mixer (LO to RF). Figure 11(b) also shows the measured return loss performance of the RF front-end. All RF ports of the RF front-end are well matched with 50 Ω at 23–28.2 GHz. The frequency shifts between

simulated and measured results in Figure 11 are mainly caused by the performance of the amplifiers. The input-referred 1 dB compression point of the receiver shows −9 dBm at a frequency of 24.15 GHz as shown in Figure 12(a). The output power of the transmitter presents 6.8 dBm at a frequency of 24.15 GHz as shown in Figure 12(b). The RF front-end consumes 71 mA (LNA: 31 mA, mixer: 6 mA, LPF: 3 mA, and DA: 31 mA) at a supply voltage of 1.8 V. The performance of the RF front-end is compared to other works in Table 3. Table 4 shows the measured performance summary of the RF front-end components, excluding the mixer, which is presented by simulation.

4.2. Radar Performance Tests

In addition, the designed chip was tested for the verification of radar performance. The Doppler shift and range information tests were performed. Accordingly, Agilent 83630A was used as a signal source and a corner reflector with a RCS of 30 dBsm was adopted as a radar target. Also micro-strip patch antennas (TX antenna gain: 18 dB, RX antenna gain: 20 dB) which have micro-strip line feeds were applied to the RF front-end using on-wafer probing and coaxial cables. The test environment is shown in Figure 13. For the Doppler shift test, a single tone signal of 24 GHz with −5 dBm was applied to the transmitter input of the RF front-end. With the moving reflector by hand, the measured Doppler shift is shown in Figure 14(a). For the range information test, a FMCW ramp waveform was used as the radar source. The FMCW waveform has a center frequency of 24.1 GHz, a sweep bandwidth B of 200 MHz and a sweep time T of 1 s. The specifications were determined by source performance for target detection. The range information test was performed for a target distance of 2.1 m, including the antenna connection cable. According

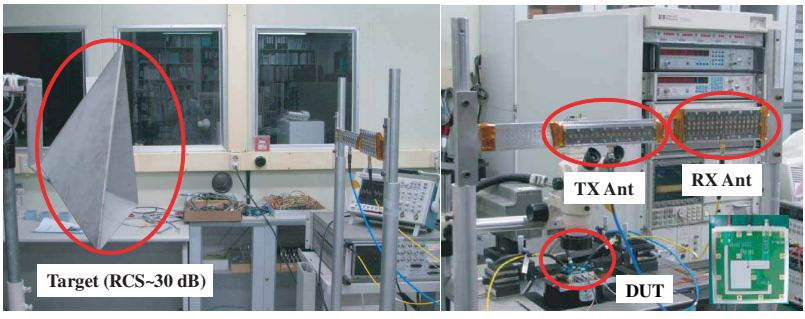
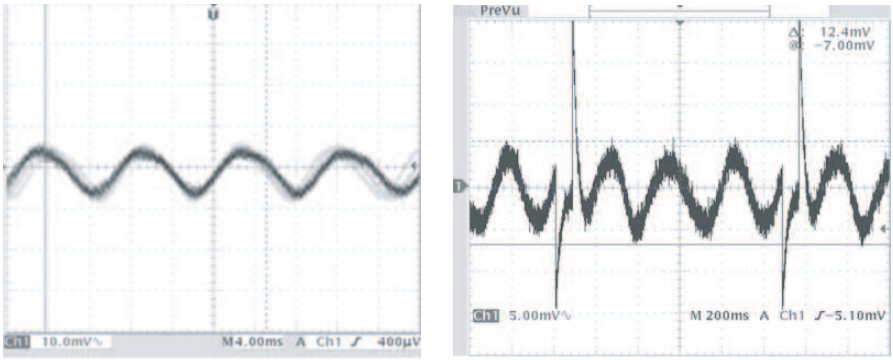


Figure 13. Radar experiment environment.

Table 4. Performance summary of components in RF front-end.

LNA and DA	
Maximum gain (dB)	12.7
3-dB bandwidth (GHz)	5.7 (21.6–27.3 GHz)
In/out return loss (dB)	In: −10 (23.6–27.3 GHz) Out: −10 (21.8–36.1 GHz)
Input 1 dB compression point (dBm)	−5.5
Minimum noise figure (dB)	5.3
Current consumption (mA)	31
Mixer (simulation)	
Maximum gain (dB)	5.8
RF/LO return loss (dB)	In: −10 (16.8–24.8 GHz) Out: −10 (20.8–27.8 GHz)
Input 1 dB compression point (dBm)	4
Current consumption (mA)	5.5
LPF	
Inband gain (dB)	1.9
3-dB cutoff frequency (MHz)	2
Current consumption (mA)	3
Balun	
Insertion loss (dB)	5 (18.4–40 GHz)
In return loss (dB)	10 (18.4–40 GHz)
Amplitude imbalance (dB)	1 (17.8–35.8 GHz)
Phase imbalance (°)	5 (13.6–32.2 GHz)
PD	
Insertion loss (dB)	< 1.3 (< 30 GHz)
In/out return loss (dB)	In: −10 (< 32.9 GHz) Out: −10 (< 40 GHz)
Isolation (dB)	15 (17–31 GHz)

to target distances, amplitude and frequency variations were observed from an oscilloscope. Figure 14(b) shows the measured results from the target distance of 2.1 m. The frequency of the measured results is compared to hand calculation using a range frequency equation as



(a) (b)

Figure 14. Measured radar test results. (a) Doppler shift caused by moving target by hand. (b) Range frequency of stationary target at a distance of 2.1 m.

follows [20]

$$f_R = \frac{2B}{cT}R \tag{5}$$

where R is the range between the front-end chip and target and c is the light velocity of 3×10^8 m/s. The measured result at the target distance of 2.1 m is 3.3 Hz and the calculated result presents 2.8 Hz, which explains a range error of 0.375 m. The range error is caused by arrangement mismatch between the target and the antennas and the limited resolution of the FMCW waveform. The arrangement mismatch also causes signal loss. The measured signal amplitude shows approximately 5 mVpp. In Figure 14(b), the peak signals come from the clock signals for controlling the sweep time.

5. CONCLUSION

This paper has presented a wideband on-chip K-band RF front-end using 0.18 µm CMOS technology for vehicular short-range radar applications. The front-end consists of a receiver (LNA + mixer + LPF) and a transmitter (DA + PD). Moreover, design methods for wide bandwidth have been presented. In particular, the receiver and transmitter achieve 3-dB bandwidth of 6 GHz and 4.8 GHz, respectively. The front-end consumes 71 mA at a supply voltage of 1.8 V. Radar performance tests using the designed chip have also been demonstrated. Measured radar performance for range information shows good agreement with theoretical expectations. Accordingly,

the designed wideband front-end can be used for not only radar applications, but other communication systems, as well.

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