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WIDE-BAND HIGH ISOLATION SUBHARMONICALLY PUMPED RESISTIVE MIXER WITH ACTIVE QUASI-CIRCULATOR

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Abstract—A novel subharmonically pumped resistive mixer (SHPRM) with a core chip dimension of $0.64 \times 0.65\,\mathrm{mm}^2$ is fabricated through a standard 0.18 µm CMOS process. An impedance-transforming active quasi-circulator is monolithically integrated with an nMOS field-effect transistor (FET) to perform up-converter mixing while simultaneously enhancing all port isolation through a broadband operation. The design analysis of impedance-transforming active quasi-circulator is also presented for matching between circulator and resistive transistor. As shown in the measured results, the mixer exhibits a 9–14.5 dB conversion loss. All port-to-port isolations better than 16.5 dB over a radio frequency (RF) of 10–20 GHz can be achieved.

1. INTRODUCTION

With the substantial interest in the emerging millimeter-wave CMOS communication systems, more and more attention is being given to complete systems-on-a-chip. There is a significant potential to integrate whole devices into a portable system for global positioning system, wireless local area network, and wireless personal area network applications. Consequently, the essential issue for millimeter-wave designers is to investigate the compact, low-cost, low-power, broadband, and high-performance CMOS transceivers in the modern millimeter-wave realm.

In general, the mixing mechanism of most mixers employs the fundamental local oscillation (LO) signal to perform frequency

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conversion. Although realizing a voltage-controlled oscillator (VCO) directly at the desired high frequency band in CMOS technology is possible, the resulting VCO would suffer from the increase of phase noise and degradation of the output power due to the degradation of the resonator quality used for the oscillator. Compared with the fundamental mixer, the subharmonic mixer (SHM) requires only a fraction of the LO frequency. This outcome makes the local oscillator sources more reliable and less expensive. Moreover, the doubler chain with amplifier buffer can be eliminated completely to economize the use of chip area and reduce power consumption further.

Previously, several SHMs constructed from open/short stubs in the III-V process have been demonstrated in the literature [1–3]. Owing mainly to the structure of the open/short stubs, the operational bandwidth is narrow. Moreover, the required LO frequency is only one half of the RF frequency, causing the quarter-wavelength open/short stubs at the LO frequency to occupy a large chip size. To extend the operational bandwidth efficiently, two new configurations of the SHMs have been proposed [4, 5]. Otherwise, the quarter-wavelength microstrip structures [1–5] are difficult to implement at a low frequency for compact requirement. Accordingly, the compactness of SHMs is highly prioritized in MMIC design. A miniature quadruple SHM with lumped frequency diplexer can be found in [6]. However, the operation with overlapping frequency bands of RF and LO signals is constrained by the frequency diplexer.

Consequently, a design concept of the subharmonically pumped resistive mixer (SHPRM) composed of an active quasi-circulator fabricated in a 0.18 μm CMOS process is proposed to fulfill the requirements of broadband operation, compactness, superior port-to-port isolation, and low-cost. Furthermore, analyses of the impedance-transforming active quasi-circulator are presented for matching between quasi-circulator and resistive transistor.

2. CIRCUIT DESIGN AND IMPLEMENTATION

The schematic diagram of the proposed CMOS SHPRM, consisting of an active quasi-circulator and a resistive transistor for subharmonic mixing, is illustrated in Fig. 1(a). Among various SHMs, the single-end SHMs with an anti-parallel diode pair (APDP) or pumped resistive transistor topologies are the most common prototype because the single-end architecture often employs the frequency diplexers constructed from high- and low-pass filters or quarterwave resonators to separate simply the RF and LO/IF signals. However, due to the intrinsic restriction of the frequency diplexer, the single-end SHM

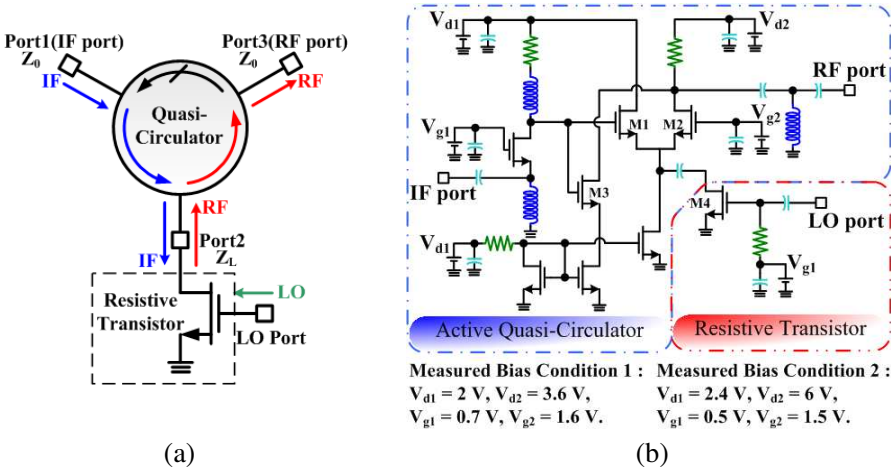

Figure 1. (a) Schematic diagram and (b) detailed circuitconfiguration of the proposed CMOS SHPRM.

cannot allow the operation with overlapping RF and LO/IF frequency bands subsequent to the limited expansion of the operating bandwidth. In our case, the frequency diplexer is replaced by the three-port non-reciprocal active quasi-circulator to improve the SHM performance appropriately.

A number of active quasi-circulator configurations have been introduced [7–9]. The major difference between the circulator and the quasi-circulator in practice is that there is no power transfer from port 3 to port 1 in the case of the quasi-circulator. The detailed structure of the proposed active quasi-circulator, as shown in Fig. 1(b), can be referred to [7], and the scattering matrix of full port matching is given by

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ \frac{2g_{m1}}{Y_0+g_{m1}} & \frac{g_{m1}+g_{m2}-Y_0}{g_{m1}+g_{m2}+Y_0} & 0 \\ \frac{-2Y}{Y_0} & \frac{2g_{m2}}{Y_0+g_{m2}} & 1 \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix} \quad (1)$$

where g_{m1} and g_{m2} are the transconductance of common-drain transistor M1 and common-gate transistor M2, respectively. $Y_0 = 1/Z_0$ denotes the characteristic admittance and is usually set to $1/50\,\Omega$ typically. The scattering parameter of S_{31} dominates the isolation performance between port 3 and port 1; hence, $Y = g_{m3} - [g_{m1}g_{m2}/(g_{m1} + g_{m2} + Y_0)]$ should be set to zero to satisfy the operation of active quasi-circulator, which can be computed from the

Condition of $Y = 0$ as follows:

$$g_{m3} = [g_{m1}g_{m2}/(g_{m1} + g_{m2} + Y_0)] \tag{2}$$

where g_{m3} is transconductance of common-source transistor M3. However, port 2 of the active quasi-circulator is connected to the drain of resistive transistor, as shown in Fig. 1(a), to feed IF signal from port 1, simultaneously extracting RF signal from port 3. Subsequently, the impedance matching issue between port 2 and the drain of resistive transistor cannot be ignored in SHPRM design. The characteristic impedance of port 2 is denoted as Z_L. After some algebraic manipulations, the impedance-transforming scattering matrix can be easily determined as follows:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ \frac{2\sqrt{Z_L Y_0}\, g_{m1}(Y_0+g_{m1}+g_{m2})}{(Y_0+g_{m1})\left(Y_0^2 Z_L+g_{m1}+g_{m2}\right)} & \frac{2(g_{m1}+g_{m2})}{Y_0^2 Z_L+g_{m1}+g_{m2}} - 1 & 0 \\ \frac{-2Y}{Y_0} - \frac{2g_{m1}g_{m2}(Y_0+g_{m1}+g_{m2})(1-Y_0 Z_L)}{(Y_0+g_{m1})(Y_0+g_{m2})\left(Y_0^2 Z_L+g_{m1}+g_{m2}\right)} & \frac{2\sqrt{Z_L Y_0}\, g_{m2}(Y_0+g_{m1}+g_{m2})}{(Y_0+g_{m2})\left(Y_0^2 Z_L+g_{m1}+g_{m2}\right)} & 1 \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \\ a_3 \end{bmatrix} \tag{3}$$

The scattering parameters of S_{21} and S_{32} are typically characterized in terms of g_{m1}, g_{m2} and Z_L. Clearly, the transmissions of IF and RF signals are primarily affected by the different impedances Z_L. From Equation (3), $S_{12} = S_{13} = S_{23} = 0$ which denotes inherent LO-to-IF, RF-to-IF, and RF-to-LO isolations, respectively, can be achieved. To improve IF-to-RF isolation, the Condition of $S_{31} = 0$ occurs when

$$g_{m3} = \frac{g_{m1}g_{m2}}{(Y_0 + g_{m1} + g_{m2})} - \frac{Y_0 g_{m1}g_{m2}\,(Y_0 + g_{m1} + g_{m2})\,(1 - Y_0 Z_L)}{(Y_0 + g_{m1})\,(Y_0 + g_{m2})\left(Y_0^2 Z_L + g_{m1} + g_{m2}\right)} \tag{4}$$

With appropriate selection of the sizes of M1, M2, and M3, the superior IF-to-RF isolation can be accomplished readily. Equation (3) shows that the IF and RF signals can operate over the same frequency band to extend operational bandwidth more efficiently. The common-gate transistor M5 is used for IF port matching. Consequently, this proposed design concept of SHPRM is adequate for the severe demand for wide-band, high-isolation, and compactness in modern SHM design.

In this case, 8 nMOSFETs [10] with f_T and $f_{\max}$ better than 60 and 55 GHz, respectively, are used to realize the proposed SHPRM. To

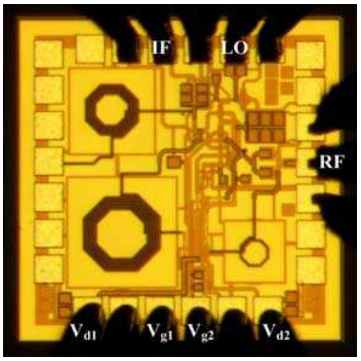

Figure 2. Microphotograph of the fabricated CMOS SHPRM. The overallchip dimension with and without the contact pads are 0.8 mm × 0.81 mm and 0.64 mm × 0.65 mm, respectively.

achieve good impedance matching between the quasi-circulator and the resistive transistor, the 48-finger resistive nMOSFET with a 96 μm gate width is optimized to ensure minimum conversion loss. The high frequency parasitic effect of metal trace is evaluated by iterative EM simulation to ensure the circuit feasibility. A microphotograph of the fabricated CMOS SHPRM is presented in Fig. 2. The chip dimension is reduced to $0.8 \times 0.81\,\text{mm}^2$. The core chip dimension, excluding the contact GSG testing pads, is only $0.64 \times 0.65\,\text{mm}^2$.

3. EXPERIMENTAL RESULTS

Figure 3 presents the measured and simulated conversion losses of the CMOS SHPRM as a function of RF frequency for the up-converter mode biased at different voltage settings. The SHPRM is driven by an LO power of 11 and 6 dBm under bias conditions 1 and 2, respectively, as depicted in Fig. 1(b). The choice of LO power level is based on the significant mixing effect observed under the bias conditions. Condition 1 is for simulation, whereas Condition 2 is for measurement. The measurements were performed with an IF power level of −16 dBm and a fixed IF frequency of 3.1 GHz. Based on the result of bias Condition 1, the conversion loss of 16.1–19.3 dB at an RF frequency of 15–27 GHz shows a large variation compared with the simulated results of 7–11.5 dB.

Figure 4 shows the measured conversion loss as a function of IF bandwidth. The measured conversion loss is 13.9–16.9 dB within an IF bandwidth from 2.25–4.75 GHz. Clearly, the measured conversion

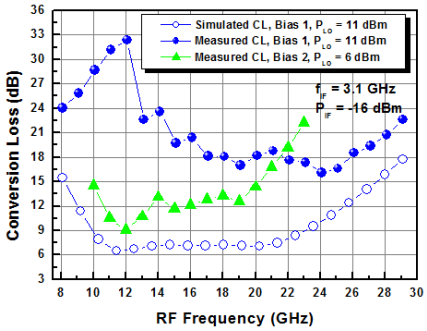

Figure 3. Measured and simulated conversion loss of the CMOS SHPRM as a function of RF frequency under bias Conditions 1 and 2 with a fixed LO power level of 11 and 6 dBm, respectively.

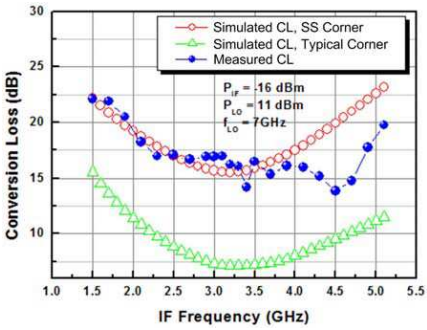

Figure 4. Measured conversion loss as a function of IF frequency of the CMOS SHPRM under bias Condition 1. Simulation for the process variations under typical and SS corners are given for comparison.

loss fairly agrees with the simulated result of the process variations of slow nMOSFET and slow pMOSFET (SS) corner. The main reason may be partly attributed to the CMOS process variation, which allows the shift of the matching point. The other reason may be due to the accuracy of the transistor nonlinear large signal model that results in a large deviation in the higher order mixing, especially the third-order mixing in this work.

The circulator provides good LO-to-IF, LO-to-RF, and IF-to-RF isolations exceeding 32, 22.5, and 1.6 dB over the 15–27 GHz RF frequency range, whereas the 2LO-to-IF and 2LO-to-RF isolations are larger than 42 dB and 32 dB, respectively. All isolations larger than 21.6 dB indicate that the use of the quasi-circulator can be a good approach to enhance the isolation. From the conversion loss versus IF input power, an input of 1 dB compression with a power of −6.6 dBm can be achieved.

As mentioned previously, the conversion loss is highly sensitive to the process variation and can be adjusted by bias conditions to achieve better performance. For Condition 2, $V_{d1} = 2.4$ V, $V_{d2} = 6$ V, $V_{g1} = 0.5$ V, and $V_{g2} = 1.5$ V. The measured conversion loss exhibits 9–14.5 dB within an RF bandwidth from 10–20 GHz as shown in Fig. 3. The observed minimum conversion loss is 9 dB when the RF frequency is 12 GHz. This reveals that the measured data can be improved substantially by adjusting the bias condition.

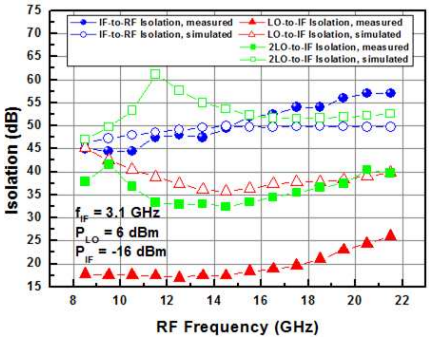

Figure 5. Measured and simulated IF-to-RF, LO-to-IF, and 2LO-to-IF isolations as a function of the RF frequency under bias Condition 2.

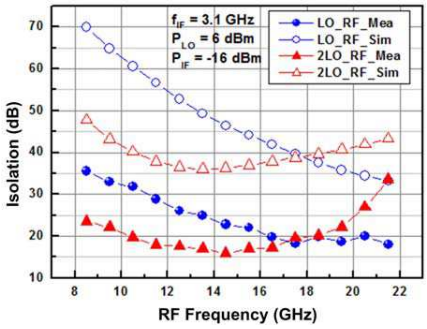

Figure 6. Measured and simulated LO-to-RF and 2LO-to-RF isolations as a function of the RF frequency under bias Condition 2.

The measured port-to-port isolations of CMOS SHPRM under the measured Condition 2 for the up-converter mode are plotted in Figs. 5 and 6. The IF-to-RF isolation is higher than 44 dB from 8–22 GHz. This indicates again that the proposed active quasi-circulator can provide superior isolation between the IF port and the RF port. The LO-to-IF isolation is higher than 16.5 dB from 8–22 GHz, and the 2LO-to-IF isolations also exceed 32 dB over the same RF frequency range. This outcome signifies that the quasi-circulator provides excellent isolation in the reverse direction. The LO-to-RF and 2LO-to-RF isolations exceed 18 and 16.5 dB, respectively. A high-pass filter is employed to enhance the LO-to-RF isolation further in this design. Due to shift matching point of quasi-circulator; however, large deviation between simulation and measurement in the LO-to-RF and 2LO-to-RF isolation can be seen (Fig. 6). Another improved approach is to reconstruct the SHPRM by a single balanced LO pumped structure while maintaining all the other circuits, resulting in broadband and inherence LO-to-RF isolation without any additional filters.

The performance comparisons of the proposed CMOS SHPRM with other reported SHMs are summarized in Table 1. Note that this work presents some significant advantages such as operating bandwidth of 66.7%, inherent port-to-port isolations, and compactness in the chip area.

Table 1. Performance comparison of the reported SHMs.

Ref.	[3]	[4]	[5]	[6]	This Work	
					Cond. 1	Cond. 2
Technology	GaAs	0.18 µm CMOS	0.15 µm GaAs	0.15 µm GaAs	0.18 µm CMOS	
RF freq. (GHz)	58.5–60.5	10–40	54–66	16–31	15–27	10–20
BW (%)	3.4	120	20	63.8	57.1	66.7
LO harm.	×4	×2	×2	×4	×2	×2
CL (dB)	11.3–13.3	15.6–17.6	15.2–18.3	12.5–16.5	16.3–19.3	9–14.5
LO-to-RF Iso. (dB)	30	> 12	> 23.5	> 14	> 22.5	> 18
LO Power (dBm)	7	8	12	12–14	11	6
Die Size (mm^2)	7	0.74	1.5	0.35	0.42	0.42

4. CONCLUSION

A 10–20 GHz monolithic SHPRM with a core chip dimension of $0.64 \times 0.65\,mm^2$ has been implemented using the 0.18 µm CMOS technology. Given the active quasi-circulator, the proposed SHPRM not only achieves a wide-band performance but also obtains inherent isolations. Moreover, the entire active design is valuable at a lower frequency band where passive component is considerably large. Accordingly, the proposed design concept is relatively suitable for building SHM with wider bandwidth, superior isolations, and high level of integration.

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