LINEARITY IMPROVEMENT OF CASCODE CMOS LNA USING A DIODE CONNECTED NMOS TRANSISTOR WITH A PARALLEL RC CIRCUIT

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Abstract—A fully integrated 5.5 GHz high-linearity low noise amplifier (LNA) using post-linearization technique, implemented in a 0.18 μm RF CMOS technology, is demonstrated. The proposed technique adopts an additional folded diode with a parallel RC circuit as an intermodulation distortion (IMD) sinker. The proposed LNA not only achieves high linearity, but also minimizes the degradation of gain, noise figure (NF) and power consumption. The LNA achieves an input third-order intercept point (IIP3) of +8.33 dBm, a power gain of 10.02 dB, and a NF of 3.05 dB at 5.5 GHz biased at 6 mA from a 1.8 V power supply.

1. INTRODUCTION

Recently, telecommunication systems require high performance, low noise, low power, and highly linear RF integrated circuits [1]. Since the digital modulation scheme requires highly linear RF front-end circuits, the linearity requirement of the LNA becomes more stringent. Owing to possible large interference signal tones at the receiver end along with the carrier, the LNA is expected to provide high linearity, thus preventing the intermodulation tones created by the interference signal from corrupting the carrier signal. Moreover, the high linearity should

be achieved in combination with a high gain, low NF and low current consumption. In a common source (CS) circuit, the cascode topology is often employed to provide high gain, low NF and high reverse isolation. However, its poor linearity limits its usage to high-jammer applications.

To improve the linearity of the cascode LNA, several linearization methods have been proposed [2–4], which are usually evaluated with the IIP3. To suppress the nonlinearity of the amplifier, the third-order derivative coefficient has to be close to zero. The multiple gated transistors (MGTR) technique [2], which falls under the category of feed forward, uses two transistors connected in parallel and biased in weak and strong inversion region, respectively. The auxiliary transistor generates a positive third-order derivative of the dc transfer characteristic (gm3) to cancel the negative third-order derivative of the gm3 generated by the main transistor. However, the penalty of using this method is that the weak inversion transistor connected to the input of the LNA inducing the input impedance mismatch and the NF degradation. To eliminate this drawback, the folded cascode PMOS topology has been proposed [3]. Moreover, this topology has the advantages of low transconductance and low current consumption. Another linearization method, post-linearization technique, is introduced in [4]. This linearization technique uses a diode connected NMOS transistor to apply to a cascode common gate (CG) LNA, and the linearity performance looks good. However, by applying this technique to a cascode CS LNA, the linearity improvement is needed at the penalty of degrading the gain, NF and current consumption. This is apparent in the simulated results presented later. In this paper, we present a post-linearization technique for the cascode CS LNA with the concept of IMD sinking. In the proposed method, the IMD3 can be partially canceled by the additional folded diode with a parallel RC circuit. In addition, it will be not at the expense of gain, NF and current consumption, which is suitable for the high-frequency and high-linearity cascode CS LNAs.

2. DESIGN OF CMOS LNA

The schematic diagram of the proposed LNA is shown in Fig. 1. The inductive source degeneration structure provides simultaneous input matching and low NF. For this LNA, the input impedance can be simplified to Equation (1), where g_{m1} and C_{gs1} are the transconductance and gate-to-source capacitance of M1.

$$Z_{in} \approx j\omega(Lg + Ls) + \frac{1}{j\omega C_{gs1}} + \frac{g_{m1}Ls}{C_{gs1}} \qquad (1)$$
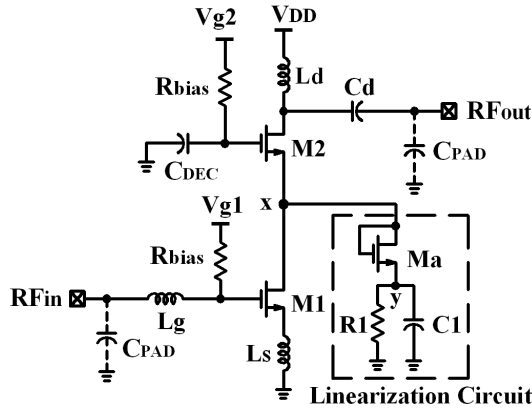
Figure 1. Schematic diagram of the proposed LNA.

The real part of the input impedance is adjusted using the source inductor Ls, while the imaginary part is removed at the resonant frequency using the inductor Lg. C_{DEC} and C_{PAD} are the bypass capacitance and parasitic capacitance of the pads, respectively. The output matching network has been designed to match $50\,\Omega$ by Ld and Cd.

The concept of the proposed linearization technique is illustrated in Fig. 2. The voltage (v_y) can be expanded as a function of v_x:

$$v_y(v_x) \approx g_{1a}v_x + g_{2a}v_x^2 + g_{3a}v_x^3 \tag{2}$$

where g_i is the ith-order expanded coefficient. The voltage and currents of M1 and Ma can be expressed as follows up to third order:

$$i_a = \frac{v_y}{z_{R1}} \approx g'_{1a}v_x + g'_{2a}v_x^2 + g'_{3a}v_x^3 \tag{3}$$

$$i_{d1}(v_{gs}) \approx g_m v_{gs} + g_{m2}v_{gs}^2 + g_{m3}v_{gs}^3 \tag{4}$$

$$v_x \approx b_1 v_{gs} + b_2 v_{gs}^2 + b_3 v_{gs}^3 \tag{5}$$

where b_i is the ith-order expanded coefficient. Since the currents at the drain node (v_x) of M1 have to satisfy the KCL equations, yielding the output current i_x:

$$
\begin{aligned}
i_x = i_{d1} + i_a &\approx \left(g_m + b_1 g'_{1a}\right) v_{gs} + \left(g_{m2} + b_2 g'_{1a} + b_1^2 g'_{2a}\right) v_{gs}^2 \\
&+ \left(g_{m3} + b_3 g'_{1a} + 2b_1 b_2 g'_{2a} + b_1^3 g'_{3a}\right) v_{gs}^3
\end{aligned} \tag{6}
$$

The proposed linearization technique can introduce the degree of freedom g'_{1a}, g'_{2a}, and g'_{3a} for linearity optimization, which partially cancels the second-order and third-order distortion terms. It is
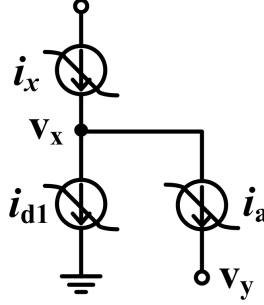
Figure 2. Conceptual view of the proposed linearization technique.

apparent from the above equation that the linearity can be improved. However, at higher frequencies, the device capacitances, such as gate-to-source, gate-to-drain, drain-to-substrate and source-to-substrate capacitances, significantly affected the current-voltage relationship. Besides, the dc nonlinearity coefficients cannot capture memory effects in the transistors. To address these issues, the newly extracted Volterra coefficients are introduced [5]. The output current i_x can be re-expressed as follows:

$$i_{x,\text{HB}} \approx g_{1,\text{HB}}(s) \circ v_{gs} + g_{2,\text{HB}}(s_1, s_2) \circ v_{gs}^2 + g_{3,\text{HB}}(s_1, s_2, s_3) \circ v_{gs}^3 \quad (7)$$

where the extracted Volterra coefficients of $g_{1,\text{HB}}$, $g_{2,\text{HB}}$, and $g_{3,\text{HB}}$ are defined as the ratio of the ac current to the ac gate-to-source voltage at each output frequency. The subscripts HB indicate the coefficients are derived using Harmonic Balance (HB) simulation.

The mechanism of distortion cancellation can be demonstrated in Fig. 3, where the extended Volterra coefficients are extracted for the transistors. It is observed that the proposed linearization technique can introduce the degree of freedom $g_{2,\text{Ma,HB}}$ and $g_{3,\text{Ma,HB}}$, which partially cancels the second-order and third-order distortion terms. Besides, the second-order nonlinearity also contributes to third-order intermodulation (IM3) product [5, 6]. Thus, the proposed technique uses the diode (Ma) and resistor ($R1$) to decide the magnitude and phase of second- and third-order nonlinearity contribution to IM3 product. The composite 2nd-order coefficient has the opposite phase with respect to the composite 3th-order coefficient. It can partially cancel the contribution from 2nd-order nonlinearity to IM3 product, resulting in a small IM3 product at the output. Thus, the linearity can be effectively improved. Since g'_{1a} is smaller than the transconductance of M2, the input impedance seen from RF_{in} of LNA is the same with and without the linearization circuit (L.C.) [4]. Besides, the degradation in gain, NF and current consumption is not severe because

the transconductance and bias current of the linearization circuit are much smaller than those of the cascode stage. These will be confirmed in the simulated and measured results.

In this work, the goal focuses on designing a novel LNA to achieve high linearity without sacrificing any of its specifications of gain, noise figure and power consumption. We utilize the diode (Ma) and resistor ($R1$) as shown in Fig. 1 to generate the i_a, and choose the appropriate size of the diode and resistor for linearity optimization. It should be noted that the IIP3 is independent of varying capacitance ($C1$), because the $C1$ is for ac ground [6]. To further investigate the influence of the proposed linearization circuit on the gain, NF, I_{DC}, and IIP3 performances of the LNA, the simulated values for the different diode and resistor size are demonstrated in Fig. 4, which provides the design guidelines of the LNAs. The frequency and $C1$ are fixed at 5.5 GHz and 4.3 pF, respectively. It is observed that proper choice of the diode and resistor size can increase the linearity of LNA. Based on the analysis results (see Fig. 4), the optimal dimensions of the linearization circuit are Ma with gate width of 25 µm, $R1$ of 9 kΩ and $C1$ of 4.3 pF. Moreover, the corresponding vector diagram is shown in Fig. 3. It should be noted that the resistor ($R1$) provides the voltage drop required to control the voltage across the diode. As can be seen from the analyzed results shown in Fig. 5, the size of $R1$ affects the magnitude and phase of the composite second- and third-order nonlinearity contribution. In order to have the opposite phase of composite 2nd-order nonlinearity contribution with respect to the composite 3th-order nonlinearity contribution, the optimal dimension of $R1$ is chosen to be 9 kΩ.
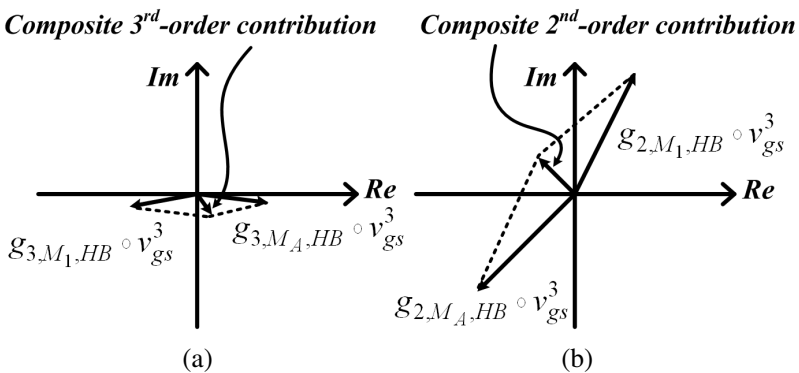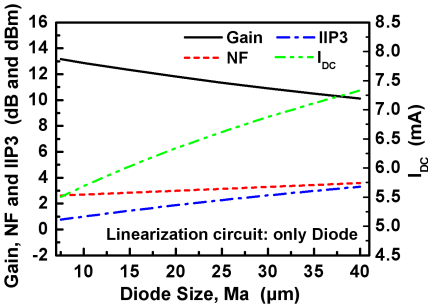

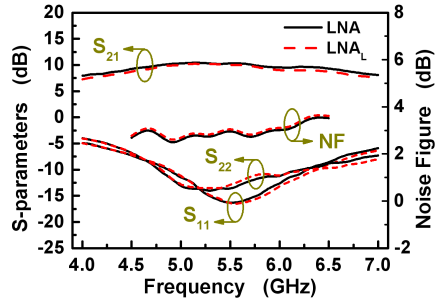**Figure 3.** Vector diagram of the proposed method for the IM3 products.
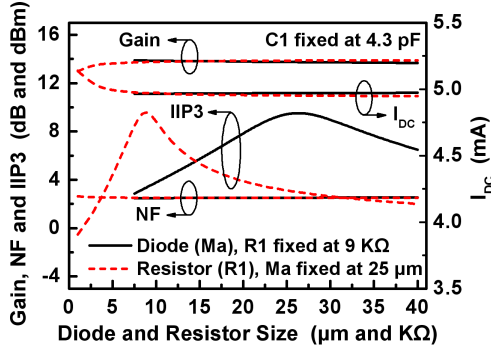
Figure 4. Simulated gain, NF, I_{DC}, and IIP3 performances of LNA sweeping the size of the linearization circuit.
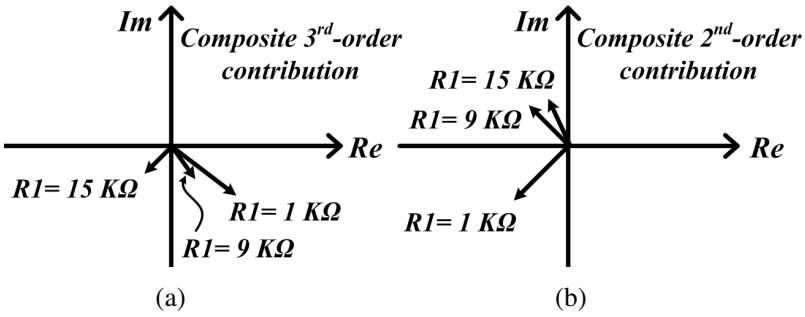
Figure 5. Vector diagram for the IM3 product.

Figure 6. Simulated gain, NF, I_{DC}, and IIP3 performances of LNA without $R1$-$C1$ circuit for the different diode size.

Figure 7. S-parameter and noise figure performances of the LNAs.

It is worth to note that $R1$ and $C1$ play an important role for the optimization of LNA performance. To further investigate the influence of the parallel $R1$-$C1$ circuit, the simulated gain, NF, I_{DC} and IIP3 performances of LNA without $R1$-$C1$ circuit are illustrated in Fig. 6. With the increase of diode size, the IIP3 of LNA can be improved. However, it will appreciably degrade the gain, NF and current consumption of LNA. Thus, the diode with a parallel $R1$-$C1$ circuit can improve the linearity performance, minimizing the degradation of gain, NF and current consumption.

3. EXPERIMENTAL RESULTS AND DISCUSSION

The LNA under this study was fabricated with a standard $0.18\,\mu$m mixed-signal/RF CMOS technology on a p-type substrate, provided by the TSMC. The proposed LNAs consume only 10.8 mW DC power with a supply voltage of 1.8 V. For comparison, the LNAs with and without linearization circuit are realized. The LNA without linearization circuit is denoted as a LNA, and the one with linearization circuit is denoted as LNA_L. The measured power gain, input/output return losses, and NF of the LNAs are plotted in Fig. 7. With the on-chip matching network, both reflection coefficients are better than -12.9 dB and the power gain are approximately 10.32 dB and 10.02 dB, respectively, at 5.5 GHz. The noise figures of the LNAs are approximately 2.96 dB and 3.05 dB, respectively, at 5.5 GHz.

The measured gain performance of the LNAs is plotted in Fig. 8. The measured input $P1$ dB with and without linearization circuit is -6.83 dBm and -6.91 dBm, respectively. The two-tone test at 5.5 GHz
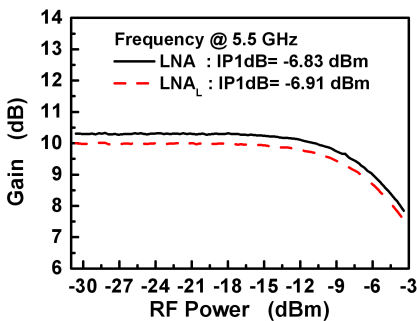
Figure 8. Measured gain performance of the LNAs as a function of RF power.
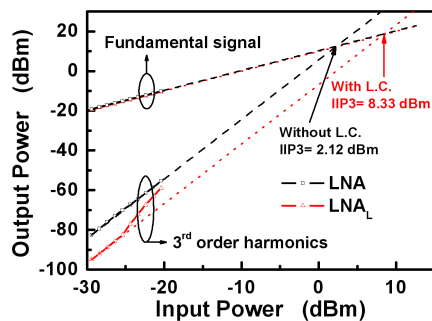
Figure 9. Two-tone harmonic performance of the LNAs.

and 5.501 GHz was performed to measure the IIP3 performance as shown in Fig. 9. The IMD3 reduction is about 12.42 dB, which improves IIP3 performance from +2.12 dBm to +8.33 dBm. The slope of intermodulation product increases for higher input power levels, which suggests a higher odd-order contribution to the nonlinearity [7]. For all inputs lower than −25 dBm, the proposed LNA maintains a lower distortion level, which makes it attractive for most high performance communication systems.

To evaluate the performance of high-linearity CMOS LNAs, different figures of merit (FOMs) are commonly used in the literature. A first figure of merit (FOM$_A$) of the LNA is defined as follows:

$$\text{FOM}_A = 10 \log \left(100 * \left[\frac{Gain\,[\text{abs}]}{(F-1) \times P_{dc}\,[\text{mW}]} \right] \left[\frac{OIP3\,[\text{mW}]}{P_{dc}\,[\text{mW}]} \right] \right) \quad (8)$$

Further, it can be extended to include the operating frequency (f_o) as follows [8]:

$$\text{FOM}_B = 10 \log \left(100 * \left[\frac{Gain\,[\text{abs}] \times f_o^2}{(F-1) \times P_{dc}\,[\text{mW}]} \right] \left[\frac{OIP3\,[\text{mW}]}{P_{dc}\,[\text{mW}]} \right] \right) \quad (9)$$

Table 1. Performance comparisons with the recently published LNAs

Ref.	This Work		[2]*		[3]*		[9]**		[10]
Tech. (μm)	0.18		0.35		0.18		0.25		0.18
fc (GHz)	5.5		0.9		2		2.4		0.8
L.C. (-)	w/o	w/i	w/o	w/i	w/o	w/i	w/o	w/i	w/i
Pdc (mW)	10.7	10.8	20.1	21.1	13.14	14.4	20	23.5	15.8
Gain (dB)	10.3	10	10	10	14.4	12.8	15.6	14.5	14
NF (dB)	2.96	3.05	2.25	2.85	1.2	1.4	3.1	3.1	3
IIP3 (dBm)	2.12	8.33	5.5	15.6	5.3	13.3	1.8	13.9	3.5
FOM$_A$ (-)	17.1	22.6	16.1	24.4	29.5	33.5	19	28.1	20.5
FOM$_B$ (-)	31.9	37.4	15.2	23.5	35.5	39.6	26.6	35.7	18.6

*Input Off-Chip Matching   **Differential Structure

Here, [abs] denotes the absolute value of the parameters. The comparisons of the circuit performance with the recently published LNAs are summarized in Table 1. Only a higher FOM_B value was reported by Kim et al. [3]. The remarkably low noise figure of 1.4 dB was reached by employing the off-chip matching components. It should be noted that the proposed LNAs are fully integrated without off-chip components. The proposed technique indeed improves the linearity performance without obvious effects, and usable at higher frequency range.

4. CONCLUSION

Based on the proposed linearization technique, a fully integrated 5.5 GHz CMOS LNA for high linearity applications has been demonstrated. The proposed linearization technique adopts an additional folded diode with a resistor and capacitor in parallel as an IMD sinker. The measured results of LNA with linearization circuit shows that it can improve linearity performance with small gain loss, noise figure and current consumption penalty. It can be easily integrated as part of a complete high-linearity transceiver because this design does not use any off-chip components. Hence, the proposed LNA could be potentially used in high-frequency and high-linearity applications.

ACKNOWLEDGMENT

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