Progress In Electromagnetics Research Letters, Vol. 17, 105–114, 2010

A 9–21 GHz MINIATURE MONOLITHIC IMAGE REJECT MIXER IN 0.18-μM CMOS TECHNOLOGY

W.-C. Chien, C.-M. Lin, Y.-H. Chang, and Y.-H. Wang

Department of Electrical Engineering
Institute of Microelectronics
National Cheng-Kung University
No. 1 University Road, Tainan City 701, Taiwan, R.O.C.

Abstract—A compact 9–21 GHz monolithic image reject mixer (IRM) with a chip dimension of $0.9 \times 0.74\,\mathrm{mm}^2$ has been designed and fabricated using a standard 0.18 μm CMOS technology. The compact configuration is composed of a 90° coupler for local oscillator (LO) and two doubly balanced ring mixers for mixing core. Particularly, a radio frequency (RF) dual balun with advanced intermediate frequency (IF) extraction technique can not only eliminate the use of power divider in IRM design, and simultaneously provide balanced signals for ring mixing, but also obtain high side band suppression without any additional IF low-pass filter. Moreover, the entire passive circuits are constructed by utilizing broad side coupling structure to achieve high-level integration further. From the measured results, the IRM exhibits a 19.4–22.4 dB conversion loss, a maximum image rejection ratio (IRR) of 34 dB, all port-to-port isolations better than 28 dB over RF frequency range of 9 to 21 GHz, and an input 1 dB compression power of 14 dBm.

1. INTRODUCTION

Recently, rapid advances in various silicon- and III-V-based semiconductor technologies have made the performance of monolithic microwave/millimeter-wave integrated circuits (MMICs) significantly improved. Whereas the demands for high-volume and low-cost cannot be ignored in practice, the MMIC chipset should achieve as high an integration level as possible. Meanwhile, a wireless high data rate transmission requires inevitably wider RF and IF operating bandwidths.

Received 26 July 2010, Accepted 6 September 2010, Scheduled 14 September 2010
Corresponding author: Y.-H. Wang (yhw@eembox.ncku.edu.tw).

Consequently, broadband, compact, low-cost and high-performance are the key issues in modern millimeter-wave territory.

A receiver system benefits by an image reject mixer (IRM) to avoid noise interference from image frequency. Previously, many methods are developed to filter the image signal. A highly integrated 1.9 GHz receiver front-end with a tunable image reject filter has been reported in [1]. The active image reject filter is designed to reduce chip size and provide image frequency tuning function. However, additional DC consumption is indispensable. Besides, passive notch filters are extensively applied to image reject low-noise amplifier [2] and IRM [3] design, respectively. Nevertheless, these prototypes typically suffer from a narrow operation bandwidth, mainly due to the characteristic of high channel selectivity. In order to permit of image rejection with broadband performance, Hartley architecture [4] provides a more convenient solution for IRM design. Accordingly, a number of Hartley-type IRMs are proposed to suppress image signal [5–9]. Although the operating bandwidth of IRM is extended substantially, the larger chip dimension cannot be neglected yet. Furthermore, Hartley architecture is rather sensitive to I/Q mismatches subsequent on the degradation of IRR.

Based on the above mention, it is essential to design a broadband, compact and high-performance IRM without DC consumption. In this work, a new RF dual balun included broadband IF extraction is proposed to simplify Hartley-type IRM and improve RF-to-IF isolation further without any IF filter. In addition, an IF phase calibration is used to compensate I/Q mismatches. Subsequently, a reasonable IRR can also be accomplished.

2. CIRCUIT DESIGN AND IMPLEMENTATION

The architecture of the proposed CMOS IRM, consisting of a LO 90° coupler, two identical LO spiral baluns, a meandering RF dual balun with broadband IF extraction, is illustrated in Fig. 1. It can be found that the overall passive circuits are constructed by utilizing broad side coupling structure to achieve high-level integration further. As compared to the conventional Hartley-type IRMs using doubly balanced ring mixing mechanism [10, 11], two identical baluns and an in-phase power divider for RF signal excitation are replaced by the new RF dual balun to decrease chip size usage appropriately. Furthermore, the IF extraction is still a key issue for ring mixer design. Thus, the proposed RF dual balun is designed to provide balanced signals for ring mixing as well as combine IF extraction circuit satisfied broadband operation requirement. Owing to the compact rearrangement of IRM,

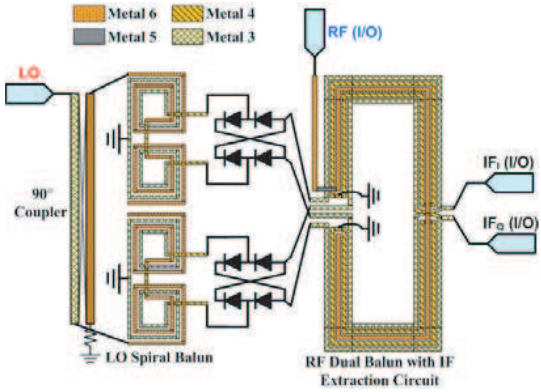

Figure 1. The proposed compact configuration of the CMOS IRM.

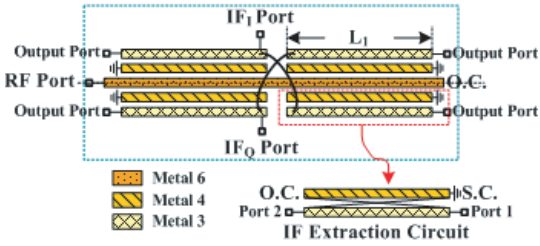

Figure 2. The structure of the proposed RF dual balun.

it will greatly benefit the reduction of layout complexity and chip dimension.

The structure of the proposed RF dual balun, as shown in Fig. 2, can be viewed the overall structure is symmetric, and the terminals of four outside strip-lines were connected respectively to form two IF I/Q ports. A major consideration in the design of the dual balun is the enhancement of the isolation between RF and IF port, which avoids the leak of RF signal from IF port, and vice versa. Due to the outside coupled-line structure of the dual balun, as shown in Fig. 2, this intrinsic feature brings a low-pass effect with wider 3-dB cut-off bandwidth. The scattering matrix for ideal coupled-line is given by

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \begin{bmatrix} 0 & T & C & 0 \\ T & 0 & 0 & C \\ C & 0 & 0 & T \\ 0 & C & T & 0 \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{bmatrix} \tag{1}$$

where the scattering parameters of C and T for the coupled and

transmitted ports, respectively, are

$$C = \frac{j\left(\frac{Z_{0e}}{Z_0} - \frac{Z_{0o}}{Z_0}\right)\sin(\beta\ell)}{2\cos(\beta\ell) + j\left(\frac{Z_{0e}}{Z_0} + \frac{Z_{0o}}{Z_0}\right)\sin(\beta\ell)} \tag{2}$$

$$T = \frac{2}{2\cos(\beta\ell) + j\left(\frac{Z_{0e}}{Z_0} + \frac{Z_{0o}}{Z_0}\right)\sin(\beta\ell)} \tag{3}$$

Z_{0e} and Z_{0o} are even- and odd-mode characteristic impedance, respectively, β defines as odd-mode and even-mode propagation constants, and ℓ is coupled-line length [12]. The scattering matrix of IF extraction circuit can be computed from the conditions $a_3 = -b_3$ and $a_4 = b_4$ as follows:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} \frac{-C^2}{1+T^2} & T\left(1 - \frac{C^2}{1+T^2}\right) \\ T\left(1 - \frac{C^2}{1+T^2}\right) & \frac{C^2}{1+T^2} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{4}$$

Furthermore, port 2 is defined as the IF port, while port 1 is the output port of the RF dual balun. The maximal amount of transmission between ports 1 and 2 occurs when

$$\beta\ell = n\pi \quad \text{rads} \quad n = 0, 1, 2, \ldots$$

Therefore, we obtain $C = 0$ and $T = (-1)^n$. The scattering matrix of IF extraction circuit can be easily determined as follows:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} 0 & (-1)^n \\ (-1)^n & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{5}$$

This results mean that the low frequency IF signal directly transmits between port 1 and port 2 without any loss. However, the coupling coefficient of coupled-line section mainly dominates the IF bandwidth. Thus the smaller coupling exhibits the larger IF bandwidth. Additionally, the minimum value of transmission is found when

$$\beta\ell = \frac{n\pi}{2} \quad \text{rads} \quad n = 1, 3, 5, \ldots$$

Further, from (2) and (3)

$$C = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}} \tag{6}$$

$$T = \frac{(-1)^{\frac{n+1}{2}} j2Z_0}{Z_{0e} + Z_{0o}} \tag{7}$$

The two-port scattering matrix of IF extraction circuit is found by substituting (6) and (7) in (4), which gives

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{8}$$

As the results show, the IF port shows an open circuit state over the RF frequency band to protect against the RF signal influence. Based on the above analysis, the proposed approach is employed to open the RF/LO signals with a broad bandwidth and to lead out the IF signals within pass-band simultaneously. This outcome implies that the RF dual balun maintains the original performance, and so the RF/LO-to-IF isolation can be improved with broadband operating.

In order to utilize the chip area more efficient, a broad side coupling structure is proposed to shrink the size of conventional planar edge-coupling structure while maintain similar performance. The entire passive circuits, as depicted in Fig. 1, are realized on metal 6, 5, 4 and 3 respectively. In this structure, the different metal layers need to be interconnected through via holes via65 and via34, respectively. In this case, the gate-drain connected nMOSFET with a f_T and $f_{\max}$ of better than 60 and 55 GHz, respectively, is used as the diode. In order to achieve good impedance matching, the 10-finger diode with total 30 μm gate width is optimized to ensure minimum conversion loss. A microphotograph of the fabricated CMOS IRM is shown in Fig. 3. The chip dimension is reduced to $1 \times 1\,\text{mm}^2$ even across X-band. Moreover, the core chip dimension, excluding the contact GSG testing pads, is only $0.9 \times 0.74\,\text{mm}^2$.

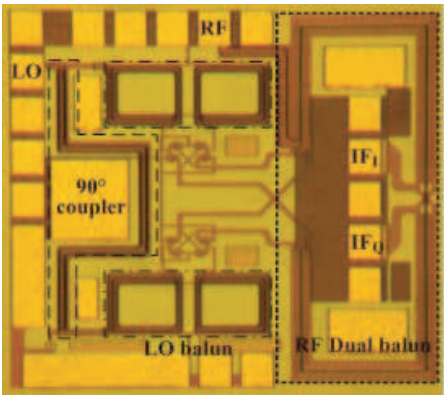

Figure 3. Microphotograph of the fabricated CMOS IRM. The overall chip dimension including the contact pads is 1 mm × 1 mm.

3. EXPERIMENTAL RESULTS

Figure 4 demonstrates the measured and simulated conversion loss of the CMOS IRM as a function of RF frequency for down-converter modes. The measured RF bandwidth were performed with an LO power level of 13 dBm and 1 GHz IF frequency. The obtained conversion loss is 19.4 to 22.4 dB within an RF bandwidth from 9 to 21 GHz. Due to the lossy substrate of silicon-based process and the inaccuracy of EM estimation, the overall conversion loss increases 4 dB as compared to the design goal. However, the trend of measured curve agrees with the simulation. Moreover, the conversion loss varies with IF frequency is also shown in Fig. 4. The measured results were obtained with a fixed LO frequency of 9 GHz. Based on the proposed IF extraction circuit, the 3-dB IF bandwidth of the mixer was found to be around 10 GHz.

The measured and simulated port-to-port isolations of the CMOS IRM for the down-converter mode are plotted in Fig. 5. Under the measured conditions shown in Fig. 5, it can be seen that the RF-to-IF isolation exceeds 16 dB with RF bandwidth ranging from 5 to 30 GHz. After connecting IF I/Q ports to IF quadrature hybrid, the RF-to-IF isolation can be enhanced up to 28 dB within operating bandwidth. Otherwise, the LO-to-IF isolation is between 26 and 47.8 dB over the same RF frequency range. Due to the employment of the advanced IF extraction technique, both LO/RF-to-IF isolations have been enhanced

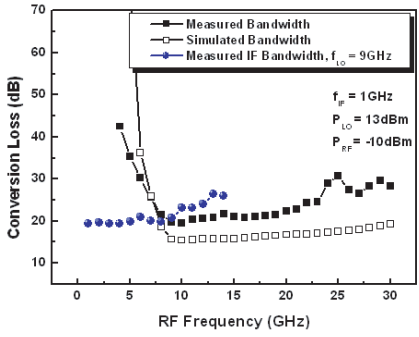

Figure 4. Measured and simulated conversion loss of the CMOS IRM as a function of frequency at a fixed LO power of 13 dBm. Also shown is the conversion loss varies with IF frequency.

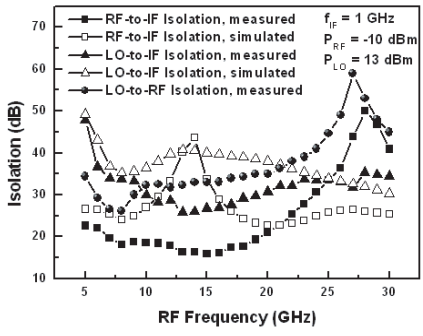

Figure 5. Measured and simulated LO-to-RF, LO-to-IF, and RF-to-IF isolations as a function of the RF frequency.

without any additional IF filters. Furthermore, the doubly balanced ring mixing is a great benefit to the LO-to-RF isolation, which is larger than 30 dB from 9 to 21 GHz.

As we know, excellent suppression of image requires accurate phase and amplitude balance in the overall IRM. Equation (9) describes IRR in terms of phase $\theta_{LO/RF}$, amplitude $\alpha_{LO/RF}$ errors and conversion efficient CE_{DBM} of ring mixer [6]. It is a good method to calibrate the phase and amplitude errors by using high-speed ADCs, but additional DC consumption is needed. In our case, a passive phase delay transmission line is more suitable to compensate the phase error produced from overall passive circuits. From the phase calibration measurement, a 40° phase compensation provides the highest suppression of image signal. Fig. 6 indicates the measured and simulated IRRs with and without phase calibration, respectively, as a function of RF frequency. Due to the low amplitude imbalance of IRM, the good IRR has been achieved without amplitude calibration. The improvement of 20 dB can be accomplished at the high end of the band ranging from 15 to 24 GHz. The maximum IRR observed was 34 dB at 21 GHz RF frequency. Moreover, it should be noted that the IRR still depends on the conversion loss of ring mixer cells. From Equation (9), the lower conversion loss CE_{DBM} inherits the higher IRR.

In addition, the measured input 1 dB compression point is 14 dBm with the RF fixed at 16 GHz. Furthermore, the two-tone intermodulation characteristic of the CMOS IRM was also measured. A two tone RF signal was applied at 16 GHz and 16.01 GHz to measure IIP3 and OIP3. As shown in Fig. 7, the IIP3 and OIP3 were determined

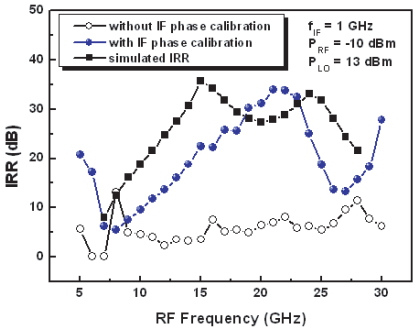

Figure 6. Measured and simulated IRRs of CMOS IRM as a function of the RF frequency.

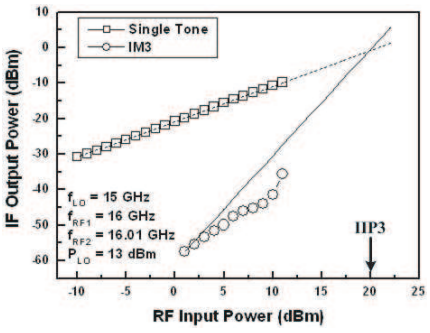

Figure 7. Intermodulation characteristics of the CMOS IRM.

to be approximately +20 and −0.4 dBm, respectively. Comparisons of the proposed structure with other published works are summarized in Table 1. This work presents some significant advantages, such as an operating bandwidth of 12 GHz across X-band, 34 dB IRR, high dynamic range and compact chip size as compared to previously reported works. Furthermore, it is worth to mention that this paper demonstrates the Hartley-type IRM implemented by the standard CMOS process for the first time.

$$IRR = 10\log\left(\frac{\begin{array}{l}\left(\sqrt{CE_{DBM}}\right)^2+\left(\sqrt{CE_{DBM}}+\alpha_{LO/RF}\right)^2\\ +2\sqrt{CE_{DBM}}\left(\sqrt{CE_{DBM}}+\alpha_{LO/RF}\right)\cos(\theta_{LO/RF})\end{array}}{\begin{array}{l}\left(\sqrt{CE_{DBM}}\right)^2+\left(\sqrt{CE_{DBM}}+\alpha_{LO/RF}\right)^2\\ -2\sqrt{CE_{DBM}}\left(\sqrt{CE_{DBM}}+\alpha_{LO/RF}\right)\cos(\theta_{LO/RF})\end{array}}\right) \quad (9)$$

Table 1. Comparison of reported IRMs.

Ref.	[6]	[7]	[8]	[9]	This Work
Technology	0.15 µm GaAs	0.15 µm GaAs	0.15 µm GaAs	0.15 µm GaAs	0.18 µm CMOS
RF freq. (GHz)	55–65	40–57	70–90	6–30	9–21
Bandwidth (%)	16.7	35.1	25	133	80
LO harm.	×1	×2	×1	×1	×1
CL (dB)	10.2	8.6	9	10	19.4
IRR (dB)	30	22	25	> 15	34
P1dB (dBm)	3	2.5	1	> 6	14
LO Power (dBm)	1	15.5	4	10	13
Die Size (mm^2)	9.24	0.84	3	1.82	0.67

4. CONCLUSION

A miniature 9–21 GHz monolithic IRM with a chip dimension of $0.9 \times 0.74\,\text{mm}^2$ is realized using the 0.18 μm CMOS technology. The new RF dual balun is utilized to provide the balanced RF signals, while simultaneously simplify IF extraction to enhance RF/LO-to-IF isolations without additional IF filters. Moreover, our fabricated IRM prototype eliminates the use of two identical RF baluns and RF in-phase power divider in the conventional Hartley-type IRM. Based on the measured results, the proposed architecture has some significant advantages, such as wider RF/IF bandwidth, superior isolations, and the improved IRR of 34 dB, which are relatively suitable for millimeter-wave applications.

ACKNOWLEDGMENT

This work was supported in part by the National Science Council of Taiwan under Contracts NSC 98-2221-E-006-213-MY3 and 982C12.

REFERENCES

1. Macedo, J. A. and M. A. Copeland, "A 1.9-GHz silicon receiver with monolithic image filtering," *IEEE J. Solid-State Circuits*, Vol. 33, 378–386, Mar. 1998.
2. Reynolds, S. K., B. A. Floyd, U. R. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyuer, "A silicon 60-GHz receiver and transmitter chipset for broadband communications," *IEEE J. Solid-State Circuits*, Vol. 41, No. 12, 2820–2831, Dec. 2006.
3. Phan, A. T., C. W. Kim, C. Y. Cha, M. S. Kang, S. G. Lee, C. D. Su, and H. T. Kim, "A low noise image rejection down CMOS mixer," *MWSCAS*, Vol. 3, 327–330, Jul. 2004.
4. Razavi, B., *RF Microelectronics*, Prentice-Hall, Upper Saddle River, NJ, 1998.
5. Singhal, P. K., S. Basu, and Y.-H. Wang, "Integrated compact broad Ka-band sub-harmonic single sideband up-converter MMIC," *Progress In Electromagnetics Research C*, Vol. 8, 179–194, 2009.
6. Gunnarsson, S. E., D. Kuylenstierna, and H. Zirath, "Analysis and design of millimeter-wave FET-based image reject mixers," *IEEE Trans. Microw. Theory Tech.*, Vol. 55, No. 10, 2065–2074, Oct. 2007.

7. Chiou, H.-K., W.-R. Lian, and T.-Y. Yang, "A miniature Q-band balanced sub-harmonically pumped image rejection mixer," *IEEE Microw. Wireless Compon. Lett.*, Vol. 17, No. 6, 463–465, Jun. 2007.
8. Gavell, M., M. Ferndahl, S. E. Gunnarsson, M. Abbasi, and H. Zirath, "An image reject mixer for high-speed E-band (71–76, 81–86 GHz) wireless communication," *Proc. IEEE CSIC Symp. Dig.*, 1–4, Oct. 2009.
9. Fujii, K. and H. Morkner, "A 6–30 GHz image-rejection distributed resistive MMIC mixer in a low cost surface mount package," *IEEE MTT-S Int. Microw. Symp. Dig.*, 37–40, Jun. 2005.
10. Passiopoulos, G. and K. Lamacraft, "A compact L-band LTCC mixer with high image rejection," *IEEE MTT-S Int. Microw. Symp. Dig.*, 249–252, Seattle, WA, 2002.
11. Mourant, J. M. and S. Jurgiel, "A broadband planar image reject mixer," *IEEE MTT-S Int. Microw. Symp. Dig.*, Vol. 3, 1637–1640, May 1994.
12. Mongia, R., I. Bahl, and P. Bhartia, *RF and Microwave Coupled-Line Circuits*, 136–137, Artech House, Norwood, MA, 1999.