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ELECTROMAGNETIC SIMULATION AND CHARACTERIZATION OF A METAL CERAMIC PACKAGE FOR PACKAGING OF HIGH ISOLATION SWITCHES

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Abstract—Packaging of planar MMICs poses a unique challenge at microwave frequencies as the dimensions of the encapsulating cavity are comparable to wavelength at the operational frequencies. In addition, the effect of ground loops (caused by bond wires exposed to ground over extended length due to gaps between interconnects) deteriorates the situation even further in circuits like MMIC switches requiring high isolation between ports. The ground loops cause reflections thereby deteriorating the insertion loss figure of merit. This paper presents optimization of design of a metal ceramic package used for packaging an SPDT MMIC switch working in the frequency range of 5–6 GHz. The microwave performance of the package was simulated using EM simulation with parameters including cavity dimensions, port placement, gaps between interconnect lines, package feed-thrus and MMIC chip pads. Detailed characterization of the bare package and packaged SPDT MMIC done later shows a good match between the simulated and measured performance. The SPDT MMIC performance degradation was arrested by improvement in the package structure and it showed insertion loss of -1.6 dB and input/output (I/O) return losses of ~ 16 dB in the new package as compared to the values of -2.1 dB insertion loss and -12 dB I/O return losses in the original package. The port-to-port isolation remained unchanged (~ 40 dB in both cases) as it is governed by the MMIC assembly inside the package rather than the conditions at the I/O interfaces in this kind of large sized packages.

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1. INTRODUCTION

Performance of any packaged Monolithic Microwave Integrated Circuit (MMIC) greatly differs from its on-wafer performance. Many researchers have investigated these effects in Plastic Quad Flatpack No lead (PQFN) packages. Effects of the molding compound on the performance of Single Pole Double Throw (SPDT) switches have been studied using Electromagnetic (EM) simulation by Uda et al. [1, 2] and Xiao et al. [3] and method to minimize the performance degradation by parasitic effect modeling has been suggested. Jessie and Larson [4] have discussed the development of a plastic Small Outline (SO) package with remarkable performance in X-band by EM optimization of the package structure and package leads. Ishitsuka and Sato [5] have described development of a metal ceramic package for Multi-Chip Module (MCM) applications. They have investigated the effect of the cavity structure, multilayer ceramic structure and frame wall metallization on the performance of the MMICs being packaged and optimized the package for application in the 30–32 GHz frequency band. Decker et al. [6] also have described development of a metal ceramic package for MCM application upto 35 GHz. In particular, optimization of the RF feedthrus to minimize insertion loss and VSWR for enhancing the performance of the package has been emphasized. Liang et al. [7] have discussed the method to deduce the package effects associated with the package lead capacitance, the self and mutual inductances of the bond wires, and the coupling between the input and output of metal ceramic packages for packaging of power transistors by using a combination of full wave EM simulation and equivalent circuit extraction. In case of metal ceramic packages, the primary causes for the influence on MMIC performance could be either the cavity resonance [8] or isolation between ports of the package [9]. The inductive connections between the chip and the package pads/feedthrus also seriously affect the performance of the packaged device due to formation of ground loops in the interface area exposed to ground due to any gap between the chip and the interconnect or between two interconnects. For instance, deterioration of performance of a packaged SPDT switch MMIC was traced to such inductive connections by Ndagijimana et al. [10]. But, their work limited the frequency of operation to about 2 GHz, and the case studied was of a low isolation requirement ($\sim$ 22 dB at 2 GHz). The effect of ground loops formed by these inductive connections becomes more serious with higher frequencies of operation and with more stringent isolation between the ports (35–40 dB at 5.5 GHz).

In our work, we have investigated the performance degradation

problems in a commercial rectangular metal ceramic package for packaging an SPDT MMIC working in 5–6 GHz frequency range. Electromagnetic simulations and experiments were carried out to study the effect of gaps between the feedthru edge and package edge. In addition, the effects of placement of ports on the cavity resonance and isolation between ports were also studied in an attempt to minimize insertion loss, maximize isolation between ports and to achieve an optimum VSWR (Voltage Standing Wave Ratio) on all ports. Effects of ground loops due to long inductive connections (bond wires) and gaps between different parts of the MMIC assembly on isolation, insertion loss and VSWR have been investigated. A new package structure was designed and fabricated to achieve the aforementioned objectives. It has been shown that by minimizing the ground loops by avoiding gaps between the elements in the assembly, performance deterioration due to packaging can be minimized. Very high isolation of the order of 35–40 dB has been achieved in the SPDT switch MMIC packaged in the new package without any degradation of insertion loss.

2. EXPERIMENTAL

A High Frequency wafer probe station, Cascade SUMMIT 10600 [11] and Vector Network Analyzer 8510C were used for the on wafer RF measurements on the empty package and MMIC chips in wafer form. A 4-port network analyzer Agilent E5071B was used to perform connectorized measurements of the packaged SPDT switches. CST Microwave Studio 5.0 [12] was used for electromagnetic simulations of the packages under study. The packages were fabricated at Kyocera America. The SPDT MMICs were designed and fabricated using the standard G7S MMIC process at GAETEC, Hyderabad, India.

3. SIMULATION

Figure 1 shows the fabricated SPDT MMIC and Fig. 2 shows the metal ceramic package (A0051, from Kyocera Inc.) under study along with the close-up view of the feedthru edge showing the large gap between the feedthru and package edge. The insertion loss, return losses, and isolation of the SPDT measured on-wafer were -1.2 dB, <-20 dB, and <-40 dB, respectively. But after packaging, the insertion loss increased to about -1.8–2.0 dB, return losses deteriorated to worse than -12 dB and isolation reduced to less than -35 dB.

To understand the cause of performance degradation, Eigen mode simulation of the package structure was carried out to check if there are any resonances in the frequency range of interest. It was found that

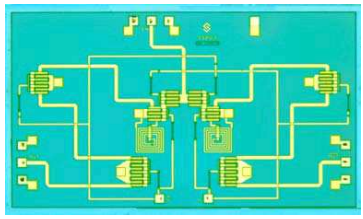


Figure 1. The SPDT MMIC chip (GS33203).

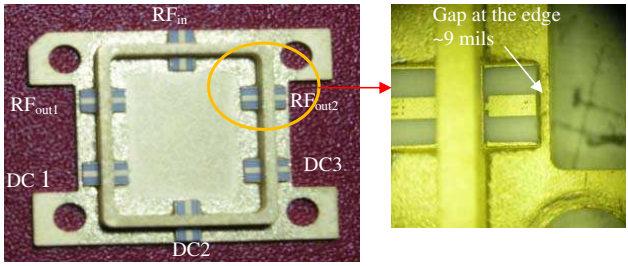


Figure 2. Picture of original package (A0051, Kyocera Inc) along with close up view of the gap between the feedthru and package edges.

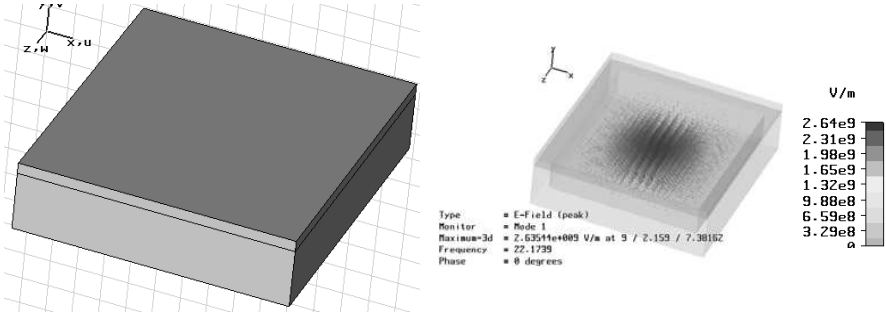


Figure 3. Eigen mode simulation of the internal cavity of the package.

the internal cavity structure was free of any resonances up to 22 GHz, with the lowest mode occurring at 22.17 GHz (Fig. 3).

The presence of dielectric material (such as feedthru, chip, and other interconnect lines), known to be detrimental for resonance situations, was also simulated by incorporating the ceramic feedthrus into the cavity, as shown in Fig. 3. Simulation showed an early onset of resonance with addition of each dielectric structure (Fig. 4, Table 1).

As evident from the Table 1, in the worst-case condition also, the frequency of fundamental resonance is 21.84 GHz, which is well

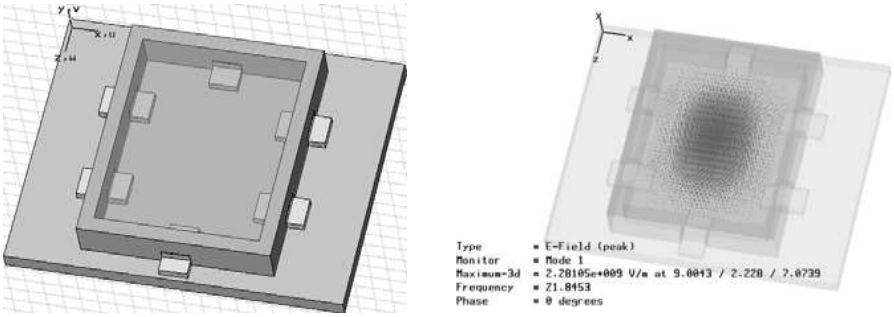


Figure 4. Eigen mode analysis in presence of feedthrus.

Table 1. Cavity resonance analysis of original package.

Structure detail	**Fundamental resonance Frequency (GHz)**
Empty cavity	22.2
RF_{in} feedthru added	22.1
RF_{out1} feedthru added	22.05
RF_{out2} feedthru added	22.00
DC1 feedthru added	21.95
DC3 feedthru added	21.91
DC2 feedthru added	21.84

beyond the frequency range of interest (5–6 GHz). These results show that the problem was not related to the basic cavity of the package. Hence, transient analysis of the package structure was performed next to simulate the isolation between the ports in open condition (OPEN case) as well as the insertion loss with a thru-line connected between a pair of ports (THRU case). This was to understand the quality of transitions and the effect of discontinuities due to these transitions. This simulation revealed that in ideal case, where all the transition lines are well-matched in terms of substrate heights and least gaps between the transitions, the insertion loss of the thru line in the package (Fig. 5(a)) was very low up to a frequency of 20 GHz. The return losses at all the ports were better than −20 dB. But, as an intentional mismatch was introduced by increasing the gap between the interconnects, necessitating the increase of length of bond wires connecting the transitions and increasing the reflection due to ground loops, the insertion loss increased and the return losses became poor.

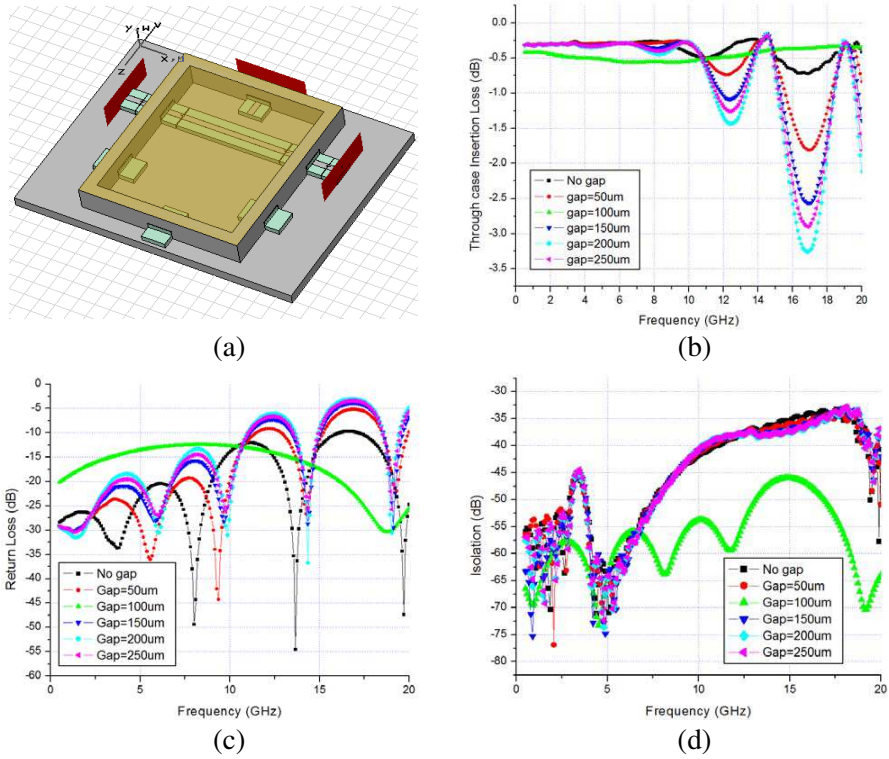


Figure 5. Transient simulation of the old package — effect of gaps between feedthru lines and package edges (causing ground loops). (a) Structure for thru-case simulation. (b) Thru case insertion loss for various gaps between feedthru and package edge. (c) Thru case return losses for various gaps between feedthru and package edge. (d) Isolation between un-connected ports of the package for various gaps between feedthru and package edge.

On careful physical examination of the package under an optical microscope, it was found that the feedthrus were not extending to the edge of the base resulting in gaps (see close-up view in Fig. 2) between the package feedthru and the test-fixture interconnect line. These gaps were measured to be about 9 mils (225 μm) on all the feedthrus. These gaps demanded longer wire bonds leading to increase in the ground loops causing reflection and deteriorating the VSWR of the device being packaged. This situation was simulated by connecting a microstrip line between ports RF_{out1} and RF_{out2} making a through connection and additional microstrip lines outside the package.

External lines were connected to the package feedthru through wire bonds. The gaps were varied from 50–250 micron, causing the increase in bond length and height. The simulation showed that the length of bond and the gap at the package edge have an appreciable deteriorating effect on the VSWR, and for a gap of 250 microns, the worst-case return losses have degraded to a value of <-10 dB at 12.6 GHz (Figs. 5(b)–(d)).

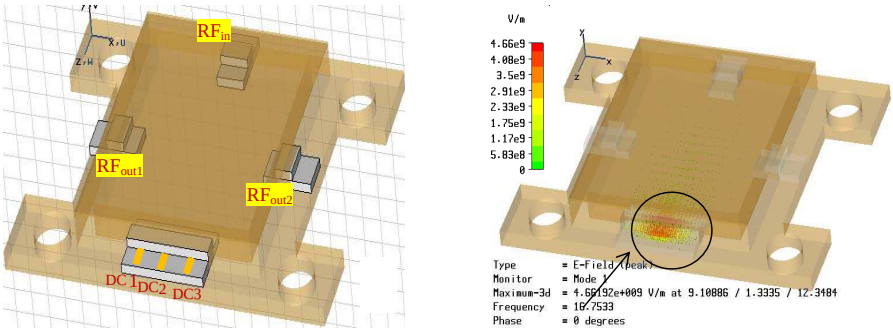
These problems were investigated and the following modifications were made to the package structure as shown in Fig. 6(a):

(i) All the DC feedthrus were moved to the side opposite to RF_{in} feedthru,

(ii) The RF_{out} feedthrus were moved to the centers of the respective sides, and

(iii) The gap at the package edges were reduced to 2 mils (50 µm), within the tolerance and manufacturing limits.

The first two modifications were done from the point of view of easing the assembly, testing and use of the package, while the third modification was done to alleviate the problem of deterioration of VSWR. The modified structure was simulated for cavity resonance to make sure that the new structure was also resonance-free, at least up to 15 GHz (Fig. 6(b)). It is evident from Table 2, that even in the worst-case condition, the frequency of fundamental resonance is well beyond the frequency range of interest (6 GHz). The field intensity in the final case ($f_r = 16.75$ GHz) is concentrated near the DC feedthru where no active RF circuitry would be present in the actual application. The frequency of the next resonant mode (with intensity concentration in



(a) (b)

Figure 6. Eigen mode analysis of the modified package structure.

Table 2. Cavity resonance analysis of modified package.

Structure detail	Fundamental resonance Frequency (GHz)
Empty cavity	22.17
RF_{out1} feedthru added	22.07
RF_{out2} feedthru added	21.95
RF in feedthru added	21.86
DC feedthru added	16.75

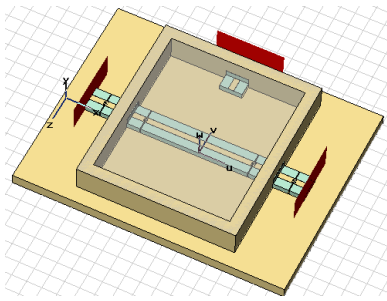


Figure 7. Modified package structure with minimum realizable gaps during assembly and production.

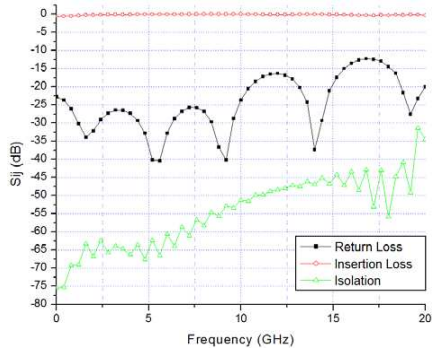


Figure 8. Transient simulation of the modified package structure.

the area of RF circuitry) is 22.20 GHz, and hence the package could be used up to 22 GHz.

Transient analysis of the modified structure was also done by connecting a 50-ohm thru line between two ports as shown in Fig. 7 to study the effect of gap reduction at the package base edge. Simulation showed a definite improvement in VSWR as shown in Fig. 8, compared to the earlier case. Additionally, the isolation between the ports in "open case" improved by about 10 dB between 5–10 GHz because of the increased distance of these ports with respect to RF_{in} port, gained by moving the RF_{out1} and RF_{out2} ports to the centers of the respective sides.

Simulation of increasing the gap between the interconnects in closed lid condition was also performed as in the case of old package configuration. It was observed that as the gap between interconnects

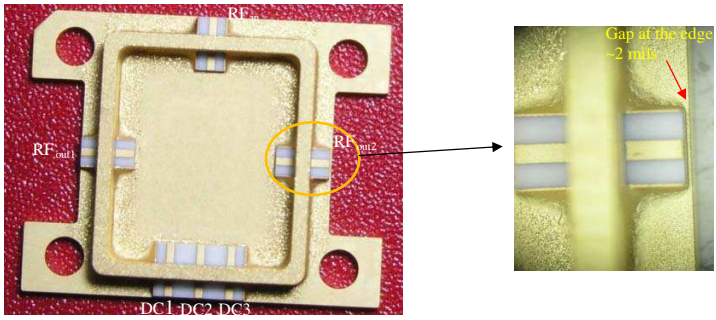
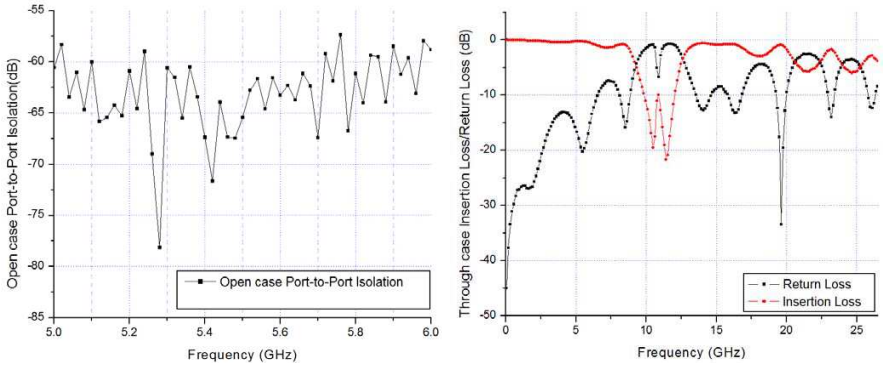


Figure 9. (a) Picture of the modified package. (b) Close up view of the feedthru showing the reduced gap at the edge.

increased, VSWR and isolation between the ports deteriorated due to increase in bond length and hence the increased ground loop. It was observed that for a typical gap of 50 microns between the interconnects, 2–3 wire-bonds with a wire diameter of 25 microns and loop height not more than 100 microns are required to achieve a VSWR of at least 1.6 : 1 (return loss better than −13 dB) on all the ports up to a frequency of 11 GHz. This modified structure was fabricated at Kyocera Inc. USA. Fig. 9 shows the picture of the modified package. The close-up view of the feedthru clearly shows the reduction of the gap between the feedthru and the package edge as compared to the original package shown in Fig. 2. The three DC feedthrus shown in the picture at the bottom were not included in the simulation, as they do not have any relevance in the RF performance of the package.

4. CHARACTERIZATION

A detailed characterization of the original package was done to confirm the results of EM simulation, prior to actual modification of the package. First, the measurement of the empty package was done by wire bonding the package I/O ports onto Co-Planar Waveguide (CPW) structures and measuring the performance using CPW wafer probes (Air Coplanar Probes from Cascade Microwave Inc). The measurements were done in two conditions, viz., Open condition, and Thru condition (a 50 ohm line connected between two ports). Fig. 10 shows these measurements. These measurements show rapid degradation in the insertion loss and return losses beyond 8 GHz due to length of bonds necessitated by large gaps between the interconnects etc., as was illustrated in the simulation. The SPDT switch was measured in bare die form prior to packaging and showed



Open case Through case

Figure 10. CPW measurements of the original package.

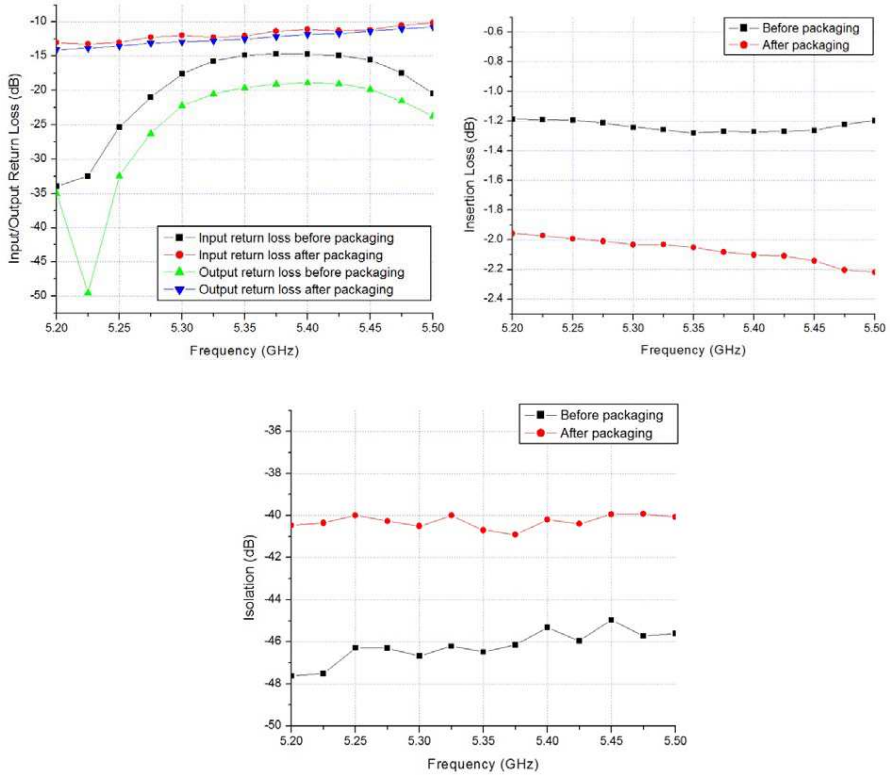


Figure 11. Measured results of SPDT in old package prior to optimization of assembly parameters.

an insertion loss of −1.3 dB, input return loss of −15 dB, output return loss of −20 dB and port-to-port isolation of −46 dB during on-wafer measurements. The switch was then packaged in the original package and measurements of insertion loss, isolation and return losses were done again by wire-bonding the package I/O interconnects to CPW structures, and measuring the performance using CPW probes (Fig. 11). The insertion loss of the packaged switch degraded to −2.1 dB, input and output return losses degraded to −12 dB and isolation degraded to −40 dB.

These measurements confirm the deterioration of performance as predicted by simulation and it was expected that if the modifications indicated by simulation were incorporated, it should result in improvement in the packaged device performance. Accordingly, the gap between interconnects, the numbers and lengths of bond wires, and the test fixture for testing of these packaged devices were

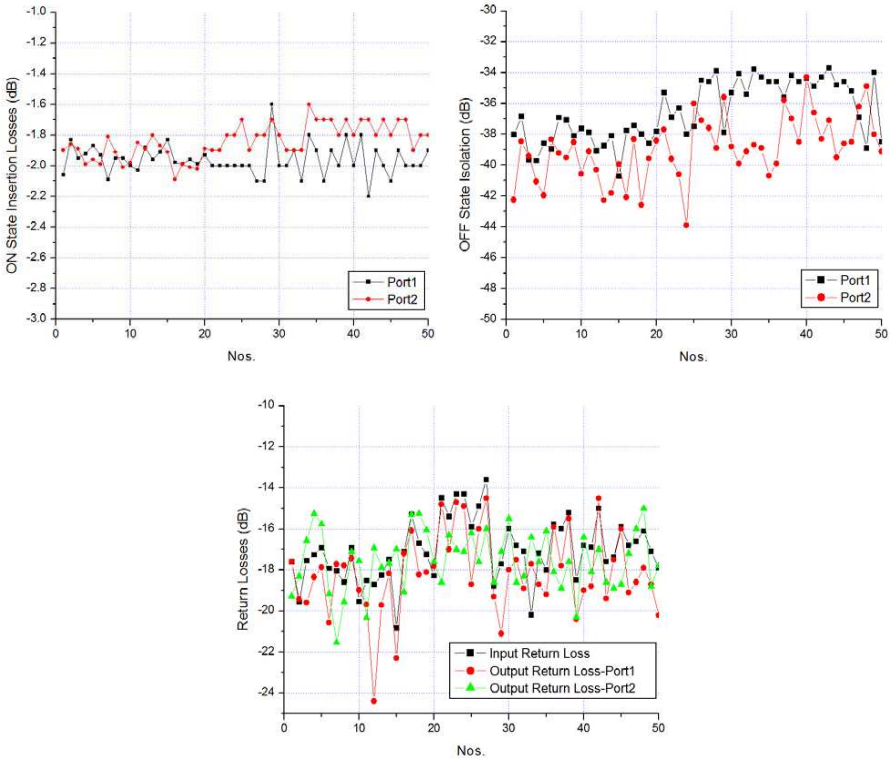


Figure 12. Measured data of 50 SPDT switches after optimization of assembly parameters.

optimized [13]. The actual performance was measured on more than 50 SPDT MMICs with this optimized assembly procedure. Fig. 12 shows these results and it is clear that reduction of gaps leading to ground loops helped in improving the performance as indicated by simulation.

In the measurements shown in Fig. 12, the original package was used. Improvement in the return losses was achieved by bonding multiple wires between the microstrip lines of the package and interconnect line of the test fixture. This approach, however, is not viable for large volume production as it incurs damage to the microstrip line of the feedthru when this operation is performed many times during the screening process of the packaged MMIC for high reliability applications. Taking a cue from the simulation and the package characterization as described above and considering the ease of production, the package was modified and manufactured at Kyocera USA, as shown in Fig. 9.

The gaps at the package edges were reduced to 50 microns, as mentioned earlier. The samples of the new package were characterized again to verify the improvement. It was observed that the insertion loss characteristics (thru-case), which was degrading rapidly after 8 GHz in the old package, was less than 1 dB, and the return losses were better than −15 dB up to 15 GHz (Fig. 13).

The SPDT MMIC was packaged in the new modified package. Fig. 14 shows the measured results of the SPDT in new package. In this case, the insertion loss was −1.6 dB (degradation was arrested to less than 0.4 dB compared to on wafer performance), isolation was −40 dB (degradation of only about 5 dB) and return losses were better than 16 dB. This validates the predictions made by simulation.

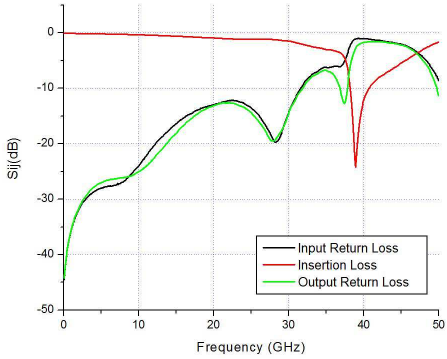


Figure 13. Measured data of feed thru for modified A0051 package (Courtesy: Kyocera Asia Pacific, Malaysia).

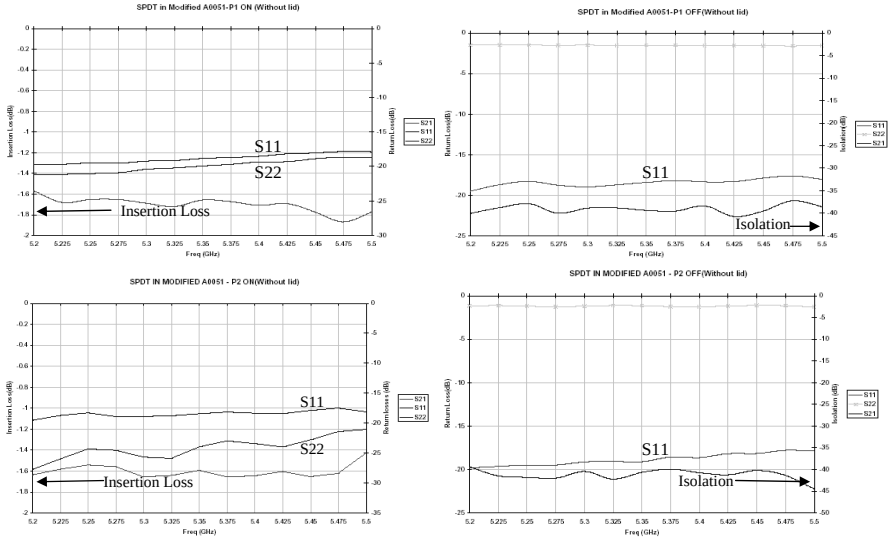


Figure 14. Measured data of the SPDT MMICs in modified A0051 package.

5. CONCLUSION

Effect of ground loops arising due to gaps between interconnects in the metal ceramic packages for SPDT switch was studied. A commercial metal ceramic package, manufactured by Kyocera Inc. USA, was considered as a sample case for packaging of a 5–6 GHz SPDT MMIC switch. The package cavity was analyzed for cavity resonance and the port-to-port isolation as a function of port placement. It was seen that in the bare package, the isolation improves with increasing port-to-port distance. The effect of gap between the feedthru edge and package base edge was also simulated for gap values of 50 to 250 microns. This parameter was found most critical in the performance of the package feedthrus. The simulation showed that this gap was detrimental for insertion loss and return loss of the feedthru. This is attributed to ground loop formation due to longer wire bonds needed to connect the feedthru to the test fixture interconnect lines. The simulated results have been validated by supporting measurements on the empty package as well as with SPDT switch packaged in it. The insertion loss and return losses of the SPDT switch were found to be degrading after packaging in the original package with large gaps at the edges. A modified package was designed after simulation and fabricated. The insertion loss improved by 1 dB and return losses improved by 12 dB at

10 GHz for the THRU case. The SPDT switch insertion loss improved to −1.6 dB as compared to −2.1 dB, and the return losses improved to −16 dB as compared to −12 dB with old package. More than 700 SPDT MMICs were packaged in this improved package and these showed repeatable improved performance in terms of reduced insertion loss and better return losses, compared to the switches in original package.

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