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THE MINIATURE FREQUENCY DOUBLER USING COMPENSATED CAPACITIVE LINE IN BALUN

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Abstract—A compact balanced frequency MMIC doubler using compensated capacitive line in Marchand balun is proposed. With multi-coupled lines technology, the balun is applied to a balanced doubler successfully. Compared with the conventional Marchand balun, more than 55% reduction in the length of coupled line can be achieved. Implemented by a PHEMT process, the compact monolithic balanced frequency doubler with better performance can be obtained. An operation bandwidth from 20 to 44 GHz with the best conversion loss of 8.4 dB at 25 GHz can be achieved. In addition, the fundamental frequency suppression is better than 28.9 dB, and the chip dimension is as small as $0.41 \times 0.68\,\mathrm{mm}^2$.

1. INTRODUCTION

In the communication systems, the signal sources can be obtained either by high frequency local oscillators or by doublers from a lower frequency source. The doublers is used more widely than a local oscillator as it allows a stable and high-quality oscillator working at a lower frequency and at the same time provides high performance for communication systems.

The balanced topology is especially attractive to doubler, due to its high conversion efficiency and effective suppression of fundamental frequencies [1]. In addition, the baluns are integral parts of the balanced doubler. Balun performance needs to provide outputs in terms of equal amplitude, 180-degree phase difference, and most

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important, compact size [2]. Many new topologies for the balanced doubler design have been developed to reduce the balun size with better area efficiency and balanced outputs over a wide frequency range [3–7]. Previously, good performance balanced doublers have been demonstrated, but the Marchand baluns with $\lambda/4$ multi-coupled line is too large in dimension to design flexibility [3, 4]. Moreover, the balanced doublers have been reported that rely on 3D MMIC or CPW technology to achieve its small chip size [5–7], but the complicated processes were difficult to design. Therefore, a compact and flexible balun still needs further investigation, especially in terms of improving flexibility and producing effective circuits.

In this letter, a compact 20–44 GHz frequency doubler, based on multi-coupled lines topology, is presented. Employing the extra coupled line to increase capacitors can reduce the coupled line length in the Marchand balun. Compared with the conventional Marchand baluns, more than 55% length reduction can be obtained. According to this concept, a frequency doubler using the compensated capacitive line was implemented. This doubler offers low conversion loss of 8.4–14.5 dB and good fundamental signal rejection over a wide output frequency range from 20–44 GHz. This doubler with a chip size of $0.28\,\text{mm}^2$ can be achieved.

2. DESIGN OF THE PROPOSED MINIATURE DOUBLER

2.1. Novel Balun Design

The conventional Marchand balun usually using two $\lambda/4$ coupled line sections [8], which occupies most of the chip area, is shown in Fig. 1(a). To overcome the problem, the 180° hybrid based on interdigitally coupled asymmetrical artificial transmission lines or periodic shunt capacitive stubs has been demonstrated. The compensated capacitors supplies each coupled line with different phase velocities. It can

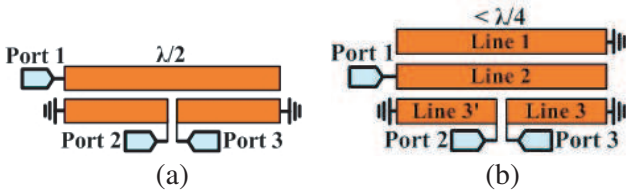

Figure 1. (a) The conventional Marchand balun. (b) The proposed balun with the compensated capacitive line.

reduce the length of the coupled line section, and maintain the good performance for hybrid [9, 10]. However, these methods may still cause a large circuit dimension and layout complications.

The proposed balun with the compensated capacitive line is shown in Fig. 1(b). This Marchand-like balun is used to produce the 180-degree phase difference, while the coupled line 1 is employed to reduce the length of $\lambda/4$ coupled line. The compensated capacitor can be easily realized by shunting coupled line-1 to the ground.

Figure 2 shows the structure and cross sectional view of the coupled lines. L is coupled line length; Z_1 and Z_2 are the characteristic impedance of line 1 and line 2, respectively. In addition, C_1 and C_2 are the capacitance per unit length of the line, and C_m stands for the mutual capacitance between coupled-lines.

In general, the symmetrical/asymmetrical coupled lines are designated as c- and π-modes. For quasi-TEM mode coupled lines, the analysis below is based on this assumption [9, 11]. The phase velocity of c- and π-modes for coupled line can be described as:

$$\nu_c = \left\{ \frac{L_1C_1 + L_2C_2 + \left[(L_1C_1 - L_2C_2)^2 + 4L_1L_2C_m^2\right]^{\frac{1}{2}}}{2} \right\}^{\frac{-1}{2}} \quad (1)$$

$$\nu_\pi = \left\{ \frac{L_1C_1 + L_2C_2 - \left[(L_1C_1 - L_2C_2)^2 + 4L_1L_2C_m^2\right]^{\frac{1}{2}}}{2} \right\}^{\frac{-1}{2}} \quad (2)$$

where L_1 and L_2 are the inductance per unit length of the line.

When line 1 and line 2 are symmetrical, the inductance $L = L_1 = L_2$ and the capacitance $C = C_1 = C_2$. While the capacitance of C is larger than C_m, it can be assumed $C_m = pC$, where $0 < p < 1$ and p is a constant. Thus the phase velocity of even- and odd-modes for symmetrical coupled line can be obtained. Equations (1) and (2) can

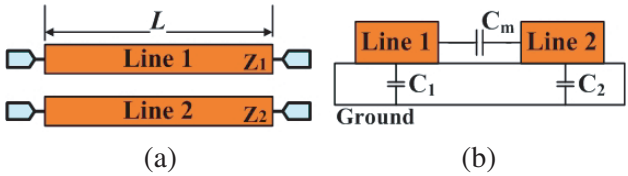

Figure 2. (a) The structure of coupled line, and (b) cross-sectional view of the coupled line structure.

be expressed as:

$$\nu_c = \nu_{even} = \frac{1}{\sqrt{LC(1+p)}} \tag{3}$$

$$\& \quad \nu_\pi = \nu_{odd} = \frac{1}{\sqrt{LC(1-p)}} \tag{4}$$

The crossover structure as shown in Fig. 3(a) for the proposed balun, line 1 was adopted to increase the effective distributed capacitance. Three-coupled lines structure can be simplified as a pair of asymmetrical two-coupled lines with an effective capacitance C_C, as illustrated in Fig. 3(b). The effective capacitor C_C is a series capacitor of C_m and C_1, where C_m is between line 1 and line 2. While the capacitance of C_C was assumed to be equal to qC, q is a constant and $q > 0$.

Similarly, the inductance/capacitance of line 2 and line 3 are the same $L = L_2 = L_3$ and $C = C_2 = C_3$ can be obtained. In addition, C_m is also assumed equally to pC, p is a constant and $< p < 1$. The phase velocity of c- and π-modes for asymmetrical coupled line can be obtained. Equations (1) and (2) can be rearranged as:

$$\nu_{c\_s} = \frac{1}{\sqrt{LC\left[1 + \frac{q+(q^2+4p^2)^{\frac{1}{2}}}{2}\right]}} \tag{5}$$

$$\& \quad \nu_{\pi\_s} = \frac{1}{\sqrt{LC\left[1 + \frac{q-(q^2+4p^2)^{\frac{1}{2}}}{2}\right]}} \tag{6}$$

According to the the Equations (3) to (6), the relations of symmetrical/asymmetrical coupled lines can be expressed as follows:

$$\nu_{c\_s} < \nu_{even} \quad \& \quad \nu_{\pi\_s} \cong \nu_{odd} \tag{7}$$

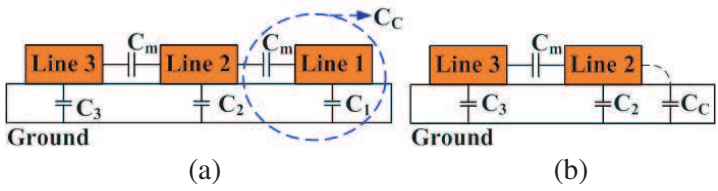

Figure 3. (a) The crossover structure of proposed balun, and (b) the simplified asymmetrical coupled line.

As indicated in Equation (7), the phase velocity of asymmetrical structure is slower than that of symmetrical structure. Since the wavelength λ and operation frequency f of the coupled line are well known as $v = \lambda \times f$. It is proved that for the coupled line with the compensated capcitive line, the effective capacitance will be increased, while the length will be reduced.

In order to impartially compare the proposed balun with the conventional Marchand balun as shown in Fig. 1(a), the simulations of the balun operated at the Ka-band using ideal coupled lines and ground were completed on the 100 µm-thick GaAs substrate. The values of the $\lambda/4$ coupled lines length, width, spacing were 850, 20, and 5 µm, respectively. In addition, the coupled line values of the proposed balun length, width, and spacing were 350, 7, and 5 µm, respectively. As Figs. 4 and 5 depict, the proposed miniaturized balun not only has wider output port bandwidth for 180° phase difference, but also provides the similar insertion loss and return loss as compared with the conventional topology. Table 1 summarizes the comparisons of the proposed hybrid with conventional Marchand balun. Although the slow phase velocity comes with narrow operation bandwidth of the proposed balun, but more than 55% reduction in the length of the proposed balun can be achieved. A proof-of-concept for a 20–44 GHz balanced doubler using PHEMT technology will be demonstrated.

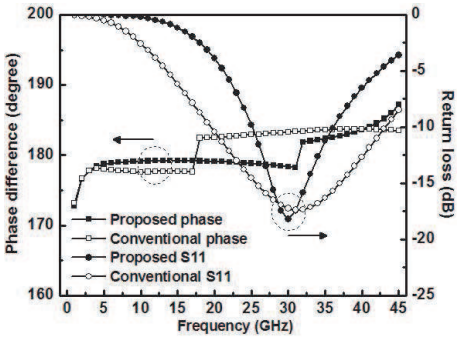

Figure 4. Comparison of the conventional Marchand balun and the proposed structure simulated phase difference S_{31}/S_{21} and return loss S_{11}.

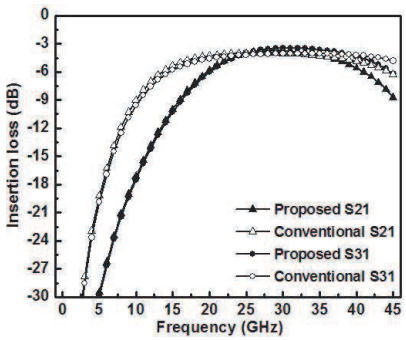

Figure 5. Comparison of the conventional Marchand balun and the proposed structure simulated insertion losses.

Table 1. Comparison with the conventional Marchand balun.

Performance	Marchand balun	The proposed balun
Frequency (GHz)	$13 \sim 45$	$19 \sim 42$
Insertion loss (dB)	$-4 \sim -6.8$	$-3.4 \sim -6.5$
Return loss (dB)	$-4.6 \sim -17.4$	$-3.1 \sim -18.2$
Phase difference (degree)	$177.7^\circ \sim 183.5^\circ$	$179.1^\circ \sim 187.2^\circ$
Coupled line length (μm)	850	350
Bandwidth (%)	110	75
Size (mm^2)	0.0765	0.0434

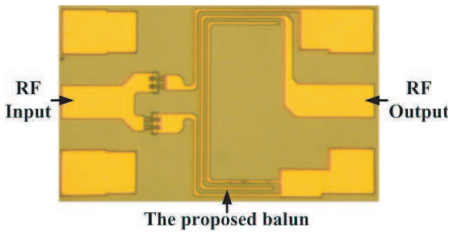

Figure 6. Photograph of the fabricated doubler. The chip dimension is 0.41 mm × 0.68 mm.

2.2. Frequency Doubler Implementation

By using the Marchand balun with a compensated capacitors line structure, the implemented balanced doubler can be simplified as shown in Fig. 6. The incoming signal was divided among balanced signals by the balun and was transferred to the gates of two diodes. To adjust the width and length of the coupled line properly, the multi-coupled lines structure can also serve as an impedance transformer from the input terminal to the diodes at the same time. Furthermore, the balun can not only provide the balanced signals easily to the diodes, but also have a compact size smaller than traditional balanced doubler.

To design this MMIC doubler, the layout was verified using the ADS and Zeland IE3D software, and the harmonic balance method was used to simulate the frequency doubler. The fabricated chip on a 100 μm-thick GaAs substrate implemented by a WIN PHEMT process as shown in Fig. 6 is as small as 0.41 mm × 0.68 mm.

3. DOUBLER RESULTS

The fabricated MMIC frequency doubler was attached on carrier plates for testing. The measurement of the input and output signals was provided by the coplanar GSG on-wafer system based on the Agilent E4446A spectrum analyzer that was calibrated by the E44198 power meter, while the losses of the probes and cables were calibrated by the PNA E8364A network analyzer.

Figure 7 shows the conversion loss and fundamental suppression as functions of output frequency. The conversion loss is better than 14.5 dB from 20 to 44 GHz with the best conversion loss of 8.4 dB at 25 GHz. The fundamental signal suppression is 28.9–57.1 dB at the input power of 15 dBm. As the Fig. 7 indicates the proposed balun provide two outputs signals with equivalent amplitudes and differential phase. It makes a good conversion loss, fundamental signal suppression and broad bandwidth.

Figure 8 shows the output power of the frequency doubler as a function of input power, ranging from 0 to 20 dBm. Consistency between the measured and simulated results can be observed. The saturated output power of the second harmonic signal is 6.6 dBm, while the corresponding fundamental signal output power is −29.6 dBm at input power 15 dBm.

The deviation between simulations and measurements can be seen. This is partly due to the use of the simple two-finger 10 μm in channel length Schottky diode's model with low-junction series resistance and junction capacitance offered by WIN Semiconductor in simulation.

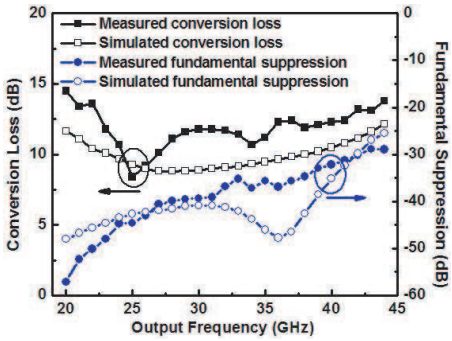

Figure 7. Conversion loss and fundamental suppression as functions of output frequency at 15 dBm input power for the proposed doubler.

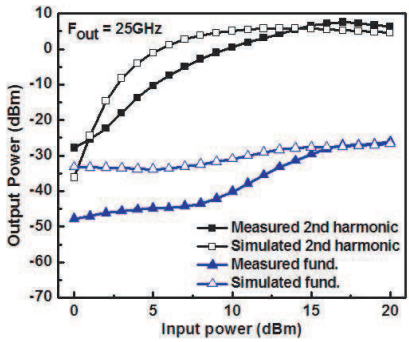

Figure 8. Output power of the fundamental and second harmonics as a function of input power at 25 GHz.

Table 2. Comparison with the reported millimeter-wave balanced doublers.

Reference	This Work	[3]	[4]	[5]	[12]
Technology	0.15 µm PHEMT	0.15 µ m PHEMT	HBT	0.15 µ m PHEMT	HBT
Output Freq. (GHz)	20 ∼ 44	22 ∼ 50	16 ∼ 40	63 ∼ 75	14 ∼ 22
Conversion Loss (dB)	8.4 ∼ 4.5	12.5	12	8 ∼ 20	4
Fundamental Rejection (dB)	28.9 ∼ 57.1	> 19	> 20	> 35	> 20
P_{DC} (mW)	0	0	0	50	75
Chip Size (mm^2)	0.28	0.561	8	1	1

More parameters, such as dielectric constant, metal loss, discontinued junction, and parasitic capacitive with the inductance of the Schottky diode's model, should be considered in design process. This will make the simulated results more accurate.

Table 2 summarizes the comparisons of the proposed doubler with the reported balanced frequency doublers [3–5, 12]. This frequency doubler adopts the proposed miniaturized balun, which also provides the compact size and satisfied performance.

4. CONCLUSION

A balanced frequency doubler incorporated with a novel miniaturized balun has been presented. By using the compensated capacitive line, the traditional Marchand balun can be easily designed with small sizes. The 20–44 GHz MMIC frequency doubler has been realized. The doubler achieves the best conversion loss of 8.4 dB at 25 GHz, and realizes more than 28.9 dB fundamental signal suppression from 20 to 44 GHz. As the measured results show, this balun not only provides a wideband performance to design a frequency doubler but also reduces the entire circuit size, which is very attractive for microwave and millimeter-wave applications.

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