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A BROADBAND DUAL-INFLECTION POINT RF PREDISTORTION LINEARIZER USING BACKWARD REFLECTION TOPOLOGY

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Abstract—This paper presents a flexible and generic broadband RF predistortion linearizer designed using backward reflection topology that can correct for the dual-inflection point type compression characteristics usually encountered in the gain profile of metal semiconductor field effect transistor (MESFET) based power amplifiers. It employs circuit configuration of two parallel Schottky diodes with one p-intrinsic-n (PIN) diode in parallel, connected at two ports of a 90° hybrid coupler. The Schottky diodes are coupled via a quarter wave transmission line segment which generates dual inflection points in the gain characteristics of the linearizer. The incorporation of a PIN diode helps in improving the achievable range in the gain and phase characteristics of the linearizer. Overall, the linearizer is capable of linearizing various types of power amplifiers owing to the flexible control on the linearizer's parameters and eventually the gain and phase characteristics of the linearizer. The proposed linearizer can be employed in the frequency range of 1.4–2.8 GHz and can simultaneously improve the third- and fifth-order intermodulation distortions. The measurements carried out on a commercial ZHL-4240 gallium arsenide field effect transistor (GaAs FET) based power amplifier demonstrates the broadband functionality of the proposed linearizer.

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1. INTRODUCTION

Highly efficient and linear power amplifiers (PAs) are in high demands with the emerging wireless standards. The transistor devices employed in PAs are operated in saturation mode to achieve high efficiency, but this introduces amplitude and phase distortions in the output. To improve the performances of PAs and to mitigate these distortions, analog and digital linearization techniques [1–18] have been adopted. Among these techniques, pre-distortion linearizers [8–14] are very popular as they possess wide bandwidth and can be easily incorporated as separate stand-alone units in the existing PAs. The pre-distortion linearizers provide equal and opposite gain and phase distortion, at the input of the PAs, to those exhibited by the PAs. The pre-distorter and PA combine together to remove the amplitude and phase distortions from the final output.

An analog linearizer that employs a series feedback amplifier with large source inductance [8] is miniature in size and extremely simple. This technique although benefits from low DC power consumption but can be applied only to PAs whose input power is beyond 20 dBm. A linearizer based on a series diode with a parallel capacitor [9] overcomes the limitations of the linearizer reported in [8]. This linearizer although miniature and simple in configuration requires additional isolation mechanism to isolate it from the PA to be linearized. Moreover, this linearizer has very limited degree of control on the achieved distortions in gain and phase characteristics and thus is very limited in applications. The diode based linearizer reported in [10] is flexible and provides a higher degree of control on achieving the gain and phase characteristics but still requires isolation mechanism between it and the PA. There are techniques to overcome this isolation issue as reported in [11, 12] by either employing isolator or by using hybrid couplers. Although all of these linearizers have certain benefits but lack the capability to linearize PAs exhibiting dual-inflection points in their gain characteristics.

Recently reported linearizer [19] is capable of linearizing PAs with dual-inflection point gain curves. The linearizer incorporates most of the advantages of the linearizers reported in [10, 11] but unfortunately not suitable for broadband operation. It is accepted norm that the advent of multiple wireless standards requires the PAs and the linearizers to optimally operate at broad range of carrier frequencies. This paper therefore builds on the foundation provided by the linearizer reported in [19]. The proposed linearizer is capable of operating optimally between 1.4–2.8 GHz and can linearize PAs with dual inflection points. This linearizer also provides simultaneous

improvements in the third- and fifth-intermodulation components.

2. DESIGN OF THE LINEARIZER

The block diagram of the proposed Linearizer is shown in Fig. 1(a). It consists of two similar circuit configurations, Fig. 1(b), at the second and third ports of a quadrature hybrid. The configuration in Fig. 1(b) comprises of two parallel Schottky diodes, D_1 and D_2, and a PIN diode, D_3. This configuration is substantially altered version of the one reported in [19].

The variable bias points, V_{d1} and V_{d2}, of the diodes D_1 and D_2 generate the desired nonlinear distortions in the gain and phase characteristics of this linearizer. The bias points of D_1 and D_2 are the superposition of the DC static biases from the supply voltages, V_{cc1} and V_{cc2}, and the rectified DC bias voltages resulting from the input RF signal. This allows the control of nonlinear characteristics of this linearizer by altering either the input RF signal or the supply voltages. The PIN diode, D_3, primarily works as a dynamic resistance, regulated by its bias voltage V_{d3}, and is used to achieve better dynamic control in the gain and phase characteristics of the linearizer. All the diodes are biased via separate feed resistances R_{b1}, R_{b2} and R_{b3} respectively. This ensures that the diodes can be biased independent of each other and at different bias levels thus providing the higher degree of freedom in achieving any phase and gain characteristic. The $\lambda/4$ transmission line provides the dual-inflection points in the gain characteristic of the linearizer.

The Fig. 1(a) can be analysed to determine the relationship

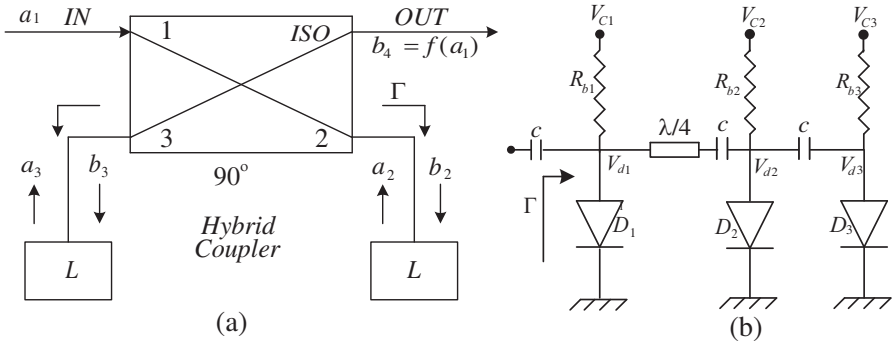

Figure 1. (a) The block diagram of the linearizer (left). (b) Schematic diagram of the circuit configuration L (right).

between the input signal, a_1, and the output signal, b_4. This dependence of b_4 on a_1 is regulated by the reflection coefficient, Γ, of the circuit configuration (L), Fig. 1(b), at the two ports of the hybrid coupler. The reflection coefficient, Γ, can be written as:

$$\Gamma = |\Gamma| \angle\varphi = s_{11} \tag{1}$$

where $|\Gamma|$ is the magnitude of the reflection coefficient, φ is the phase of the associated reflection coefficient, and the s-parameter is for the circuit configuration, Fig. 1(b), given by:

$$s_{11} = \frac{-\left[Z_0^2 \cdot (Y_1Y_2 + Y_1R_3) + Z_0 \cdot (-Y_1 + Y_2 + R_3)\right]}{Z_0^2 \cdot (Y_1Y_2 + Y_1R_3) + Z_0 \cdot (Y_1 + Y_2 + R_3) + 2} \tag{2}$$

In the above equation Y_1 and Y_2 are the admittances of the Schottky diodes, D_1 and D_2 respectively, and R_3 is the total resistance of the PIN diode, D_3. The admittances Y_1 and Y_2 and can be derived by analyzing the equivalent circuit in Fig. 2(b) as explained below:

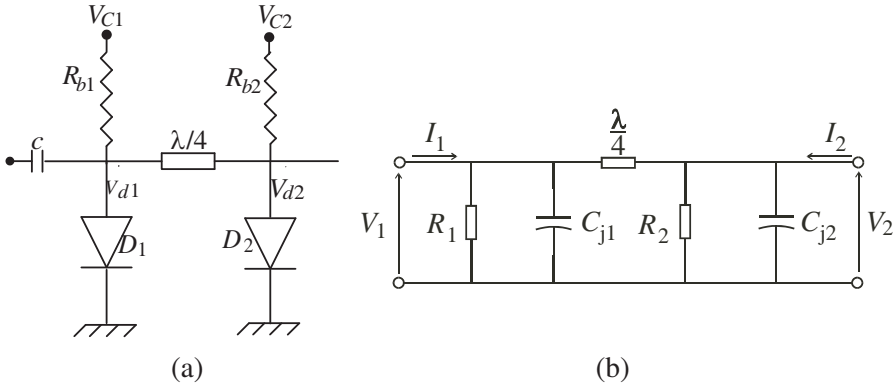

Figure 2. (a) The two Schottky diodes coupled by a quarter wave line (left). (b) The equivalent circuit of the Schottky diode configuration (right).

The total resistance for each diode is R_1 and R_2, respectively:

$$R_1 = \frac{R_{d1} \times R_{b1}}{R_{d1} + R_{b1}} \tag{3}$$

$$R_2 = \frac{R_{d2} \times R_{b2}}{R_{d2} + R_{b2}} \tag{4}$$

where, R_{d1} and R_{d2} are the dynamic resistances of the Schottky diodes

D_1 and D_2 respectively. Then the admittances Y_1 and Y_2 are given by:

$$Y_1 = \frac{1 + j\omega \cdot C_{j1} R_1}{R_1} \tag{5}$$

$$Y_2 = \frac{1 + j\omega \cdot C_{j2} R_2}{R_2} \tag{6}$$

where C_{j1} and C_{j2} are the junction capacitances of the Schottky diodes D_1 and D_2 respectively.

Similarly the total resistance R_3 of the PIN diode can be determined. In the dynamic state the PIN diode can be represented by the dynamic resistance R_{d3}. In this case the total resistance R_3 is given by:

$$R_3 = \frac{R_{d3} \times R_{b3}}{R_{d3} + R_{b3}} \tag{7}$$

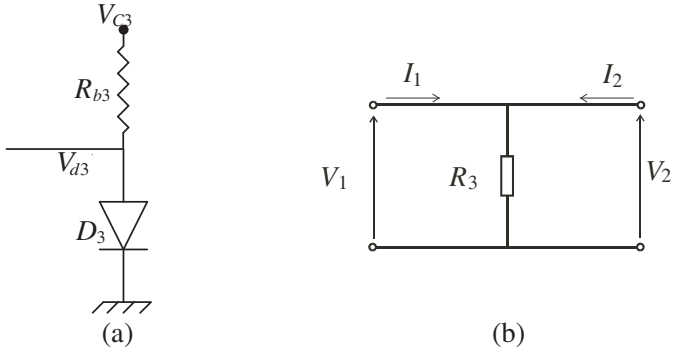

Figure 3. (a) The PIN diode (left). (b) The equivalent circuit of the PIN diode (right).

In Equation (2), the factor Z_0 represents the characteristic impedance of the $\lambda/4$ line. The decoupling capacitor, c, at the input of the circuit configuration (L) and the diode decoupling capacitors, c, have negligible impedance at the carrier frequency of the order of GHz and therefore it is not considered in the analysis. The Equation (2) provides the dependence of magnitude and phase of Γ to the bias voltages of diodes D_1, D_2 and D_3 and the impedance Z_0 of the $\lambda/4$ line. It is also evident from Equations (5)–(7) that the parameters Y_1, Y_2 and R_3 can be appropriately controlled by controlling the respective bias voltages V_{d1}, V_{d2} and V_{d3}.

Once the reflection coefficient Γ is known, the following relationship between a_1 and b_4 can be derived:

$$b_4 = f(a_1) = -j \cdot \Gamma \cdot a_1 \tag{8}$$

As $|a_1|^2 = P_{IN}$ and $|b_4|^2 = P_{OUT}$, the Equation (8) can be used to determine the relationship for the output power versus input power for the linearizer:

$$P_{OUT} = |\Gamma|^2 P_{IN} \tag{9}$$

Thus it is evident from Equation (9) that the term $|\Gamma|^2$ regulates the gain and phase characteristics of the linearizer. It is also evident from Equations (1)–(2) that the gain and phase of the reflection coefficient, Γ, can be controlled by altering the admittance Y_1 and Y_2 of the Schottky diodes, dynamic resistance R_3 of the PIN diode and the impedance Z_0 of the quarter wave transmission line coupling the Schottky diodes D_1 and D_2.

The prototype for this proposed linearizer was built on a RT/5880 duroid substrate with a dielectric constant of 2.2 and thickness of 0.508 mm. The chosen PIN and Schottky diodes were from Agilent with models HMPP-3890 and HSMS-2820 respectively, while the chosen 90° hybrid coupler is from Anaren. In the current investigation, the *1 W GaAs FET* amplifier was used for the purpose of linearization. Therefore simulations were carried out on the linearizer to determine the values of the design parameters identified in Equation (2) such that the predistorter will be customized and aligned with the amplifier

For the present case, the optimal value of the impedance of the quarter wave length transmission line section comes out to be 45 Ω. The values for the bias feed resistances R_{b1}, R_{b2} and R_{b3} comes equal to 1 kΩ. It will be demonstrated in the next section that proper control of bias voltage for D_1, D_2 and D_3 generates the desired phase and gain characteristics.

3. EVALUATION OF THE LINEARIZER

To evaluate the performance of the designed linearizer, first a *1 W GaAs FET* amplifier was selected. The normalized gain and phase characteristic of the amplifier, at carrier frequency f_0 of 1.63 GHz, is shown in Figs. 4(a) and 4(b) respectively. It is evident from 4(a) that the gain characteristic exhibits a dynamic expansion of 0.16 dB and then a compression of −1.18 dB for the input power dynamic range of 30 dB. This gives a total dynamic characteristic of 1.34 dB. It can also be deduced from Fig. 4(b) that the chosen *1W GaAs FET* amplifier exhibits phase distortion of −10° at the input 1 dB compression point of −8.5 dBm.

In principle, the linearizer should possess gain and phase characteristics which are exact replicas of the inverse of the gain and phase characteristics given in Figs. 4(a) and 4(b) respectively. For this purpose, the biasing voltage of diodes D_1, D_2 and D_3 were set at

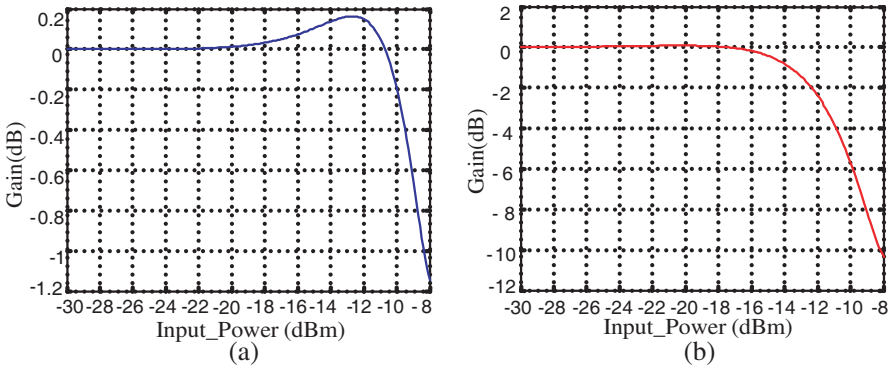

Figure 4. (a) The normalized dual-inflection gain characteristic (left) of the 1 W GaAs FET amplifier at $f_0 = 1.63$ GHz. (b) The normalized phase characteristic (right) of the 1 W GaAs FET amplifier at $f_0 = 1.63$ GHz.

0.7 V, 0.72 V and 0.75 V respectively to achieve the desired gain and phase characteristics from the linearizer. The measured gain and phase characteristics of the linearizer, at $f_0 = 1.63$ GHz, for these bias points are given in Figs. 5(a) and 5(b) respectively.

It can be deduced from Fig. 5(a) that the gain characteristic first shows a compression of -0.18 dB and then an expansion up to 1.17 dB giving a total dynamic characteristics of 1.35 dB. By comparing the Fig. 4(a) with the Fig. 5(a) it can be concluded that the linearizer is capable of linearizing the *1 W GaAs FET* based power amplifier to the extent that the distortion in the gain could be within 0.1–0.2 dB for the input power dynamic range of 30 dB. Similarly it can be comprehended from Figs. 4(b) and 5(b) that the phase distortion in the power amplifier's output performance could be significantly improved.

To demonstrate the broadband nature of the linearizer, the *1 W GaAs FET* based power amplifier was first characterized at a carrier frequency of 2.0 GHz. It was found that the power amplifier exhibits a dynamic expansion of 0.17 dB and then a compression of -1.23 dB in its gain characteristics. This gives total dynamic characteristics of 1.40 dB. The distortion in the phase at 2.0 GHz was found to be 12° at the 1-dB compression point of -8.5 dBm.

Once again, at $f_0 = 2.0$ GHz, the biasing voltages of the diodes have to be tuned in such a way that the linearizer should possess gain and phase characteristics which are exact replicas of the inverse of the gain and phase characteristics of the 1 W GaAs FET based power amplifier at $f_0 = 2.0$ GHz. For this purpose, the biasing voltage of diodes D_1, D_2 and D_3 were set at 0.55 V, 0.73 V and 0.71 V respectively

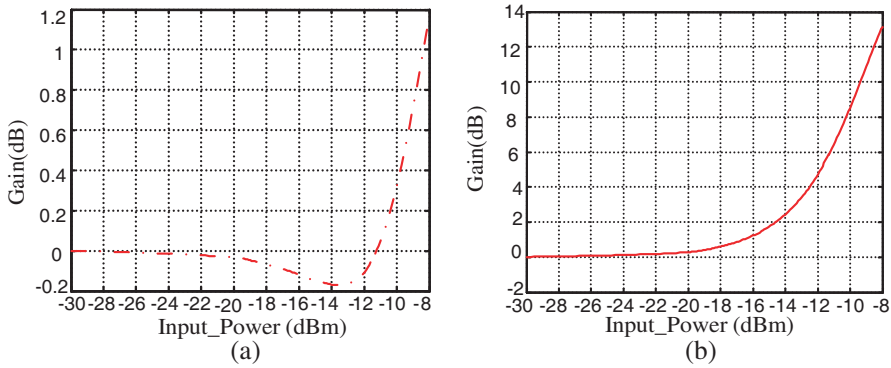

Figure 5. (a) The measured normalized gain characteristic (left) of the proposed linearizer at $f_0 = 1.63\,\text{GHz}$. (b) The measured normalized phase characteristic (right) of the linearizer at $f_0 = 1.63\,\text{GHz}$.

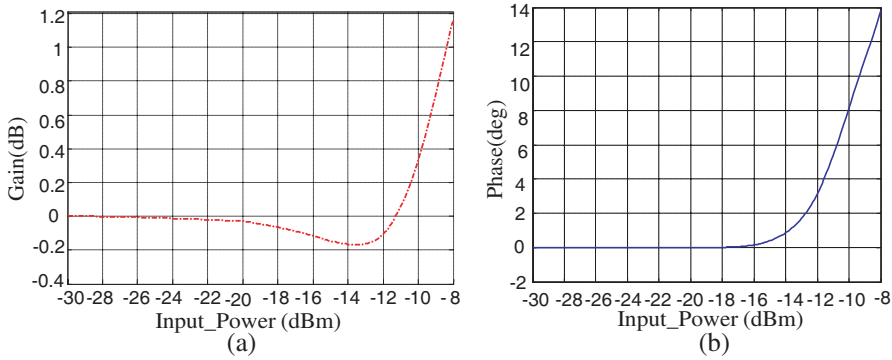

Figure 6. (a) The measured normalized gain characteristic (left) of the proposed linearizer at $f_0 = 2.0\,\text{GHz}$. (b) The measured normalized phase characteristic (right) of the linearizer at $f_0 = 2.0\,\text{GHz}$.

to achieve the desired gain and phase characteristics from the linearizer. The measured gain and phase characteristics of the linearizer, at $f_0 = 2.0\,\text{GHz}$, for these bias points are given in Figs. 6(a) and 6(b) respectively.

It can be seen in Fig. 6(a) that the gain characteristic first shows a compression of $-0.19\,\text{dB}$ and then an expansion up to $1.19\,\text{dB}$ giving a total dynamic characteristics of $1.38\,\text{dB}$. This achieved dynamic characteristic in the gain of the linearizer is very close to the inverse of the gain characteristics of the 1 W GaAs FET based PA. Thus it can be concluded that the linearizer is capable of linearizing the *1 W*

GaAs FET based power amplifier at $f_0 = 2.0$ GHz to the extent that the distortion in the gain could be around 0.1 dB for the input power dynamic range of 30 dB. It is evident from Fig. 6(b) that the linearizer gives a phase distortion of 13° at the 1-dB compression points. Therefore it can be comprehended that the phase distortion in the power amplifier's output performance can be significantly improved.

4. EXPERIMENTAL VALIDATION OF THE LINEARIZER

Although this linearizer can work for a single carrier, two carriers or any complex modulation but the current investigation involves the demonstration of the broadband operation of the linearizer and therefore simple two-tone measurement are reported. This two-tone method is simple, quick and easy to comprehend and gives ample proof of the feature and performance of the linearizer. The block diagram for performing the two-tone test is shown in Fig. 7.

The experiment was performed on a commercial ZHL-4240 from Mini-Circuits that utilizes a *1 W GaAs FET* device. The variable attenuator and pre-amplifier were used to align the predistorter with the PA that was to be linearized, such that:

$$P_{Out\_MaxG}^{PD} = P_{in\text{-}Sat}^{PA} \tag{10}$$

where $P_{Out\_MaxG}^{PD}$ represents the output power at the linearizer when it is under the condition of maximum gain expansion, and $P_{in\text{-}Sat}^{PA}$ is the input power for saturating the power amplifier. This also ensures that the input power to the power amplifier is the same as when the power amplifier is operated without the linearizer.

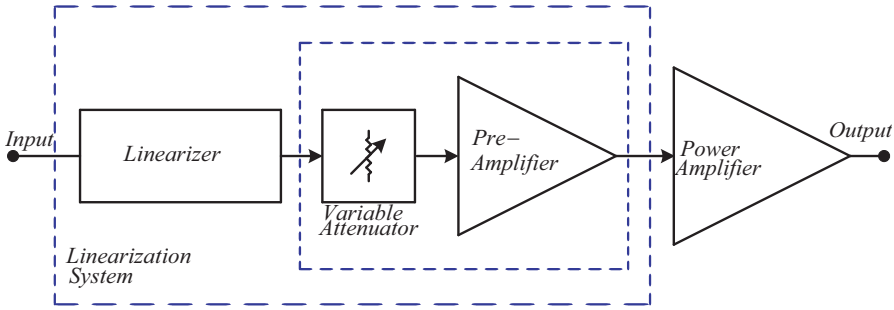

Figure 7. Block diagram of the linearization system for RF predistortion.

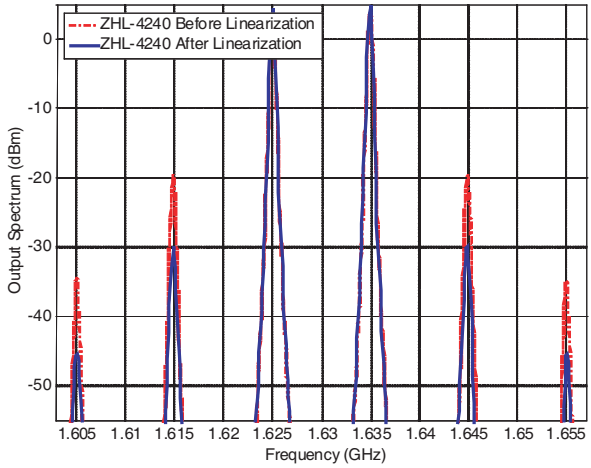

Figure 8. C/IMD with two carriers at $f_1 = 1.625\,\text{GHz}$ and $f_2 = 1.635\,\text{GHz}$ for 4.5 dB OPBO before and after linearization of the ZHL-4240 power amplifier.

To verify the broadband nature of the developed linearizer, the experiments were carried out two separate bands of frequencies around 1.63 GHz and 2.0 GHz. Single tone tests were carried out on the power amplifier ZHL-4240 at the carrier frequencies of 1.63 GHz and 2 GHz to determine the 1-dB compression point at these frequencies. This test gives the information about the behavior of the PA while backing off the input power.

The two-tone test was carried out at $f_1 = 1.625\,\text{GHz}$ and $f_2 = 1.635\,\text{GHz}$ while backing off the input power such that the Output Back-off Power (OPBO) is 4.5 dB. The OPBO of 4.5 dB was selected as the carrier to third- and fifth-intermodulation ratio is optimal at this value. The achieved power spectrum at this OPBO = 4.5 dB is shown in Fig. 8.

Then the linearizer, while keeping the bias voltages of D_1, D_2 and D_3 at 0.7 V, 0.72 V and 0.75 V respectively as identified in the previous section, was integrated at the input of ZHL-4240 and two tone tests were carried out for the same OPBO. Both the PA and linearized PA's output spectra are superimposed in Fig. 8. It is evident that the developed linearizer is able to improve the C/IMD_3 (carrier to third-intermodulation ratio) by around 11 dBc and the C/IMD_5 (carrier to fifth-intermodulation ratio) by around 13 dBc. The result achieved using the proposed linearizer is a significant improvement over the recently reported result in [19].

The carrier to third- and fifth-intermodulation ratio is optimal,

around frequency of 2 GHz, when the OPBO of 5 dB was achieved. Therefore the two-tone test at $f_1 = 1.995$ GHz and $f_2 = 2.005$ GHz was carried out while backing off the input power such that the Output Back-off Power (OPBO) is 5 dB. The achieved power spectrum, while measurement is carried out only on the ZHL-4240 alone, is shown in Fig. 8. Then the two-tone test was once again carried out while the linearizer, with the bias voltages of D_1, D_2 and D_3 were set at 0.55 V, 0.73 V and 0.71 V respectively as identified in the previous section, is placed at the input of ZHL-4240. Both the PA and linearized PA's output spectra are superimposed in Fig. 9. It is evident that the developed linearizer is able to improve the C/IMD3 (carrier to third-intermodulation ratio) by around 10 dBc and the C/IMD5 (carrier to fifth-intermodulation ratio) by around 13 dBc.

The achieved result at the frequency band around 2 GHz is also similar to the results obtained at frequency band around 1.63 GHz. Thus it can be concluded that the proposed linearizer is capable of operating properly at a wide range of frequency of interest. The limitation on frequency ranges from 1.4 GHz to 2.8 GHz is due to the components used in the design of the linearizer. This linearizer topology could be extended to work in other frequency band by changing the components.

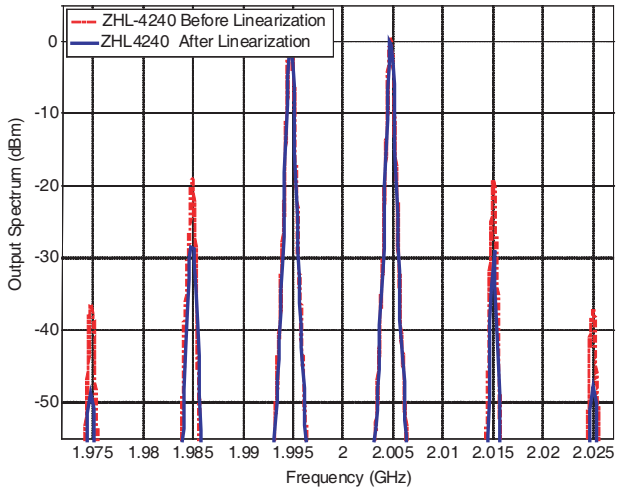

Figure 9. C/IMD with two carriers at $f_1 = 1.995$ GHz and $f_2 = 2.005$ GHz for 5 dB OPBO before and after linearization of the ZHL-4240 power amplifier.

5. CONCLUSION

A new broadband, miniature, dual-inflection point, analog, backward reflection based predistortion linearizer using parallel diode configuration, coupled with a quarter wave transmission line section, has been presented. The linearizer possesses four degrees of control to achieve the desired output characteristics through i) control of the bias voltage of the Schottky diode D_1, ii) control of the bias voltage of the Schottky diode D_2, iii) control of the bias voltage of the PIN diode D_3, and iv) control of the impedance of the quarter wave transmission line section. To verify the broadband feature of the linearizer, a *1 W GaAs FET* amplifier was taken as a case study; and, the proposed linearizer's characteristic was controlled by the diode bias voltages so as to achieve a characteristic curves which are inverse to those of the GaAs FET PA. Then the two-tone tests were carried out at frequency bands around 1.63 GHz and 2.0 GHz. The results clearly show a simultaneous reduction of third- and fifth-order distortion in both the selected frequency bands. These measurements on a commercial power amplifier, ZHL-4240 based on a *1W GaAs FET* device, demonstrated the successful broadband operation of the proposed linearizer.

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