Progress In Electromagnetics Research C, Vol. 13, 1–18, 2010

A FLEXIBLE DUAL-INFLECTION POINT RF PREDISTORTION LINEARIZER FOR MICROWAVE POWER AMPLIFIERS

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Abstract—This paper presents a very flexible and generic design of a diode-based RF predistortion linearizer that can correct for the dual-inflection point type compression characteristics found in the gain profile of metal semiconductor field effect transistor (MESFET) based and Doherty power amplifiers. It consists of a circuit configuration that has the head-tail configuration of Schottky diodes, complemented with a p-intrinsic-n (PIN) diode in parallel, at two ports of a 90° hybrid coupler for improving the performance of the linearizer. The use of a PIN diode in the linearizer provides it with an extra level of freedom in achieving the desired characteristic. Overall, the linearizer is equipped with three degrees of freedom and hence possesses the capability to achieve output characteristics that can be employed in linearizing various types of power amplifiers. The proposed linearizer has been shown to simultaneously improve the third- and fifth-order intermodulation distortions of a commercial ZHL-4240 gallium arsenide field effect transistor (GaAs FET) based power amplifier over a 10 dB power range.

1. INTRODUCTION

The advent of multiple standards and applications in wireless domains has resulted in high demand for highly efficient and linear microwave power amplifiers (PAs). The PAs should be operated in saturation mode to achieve high efficiency, but this introduces amplitude and phase distortions in the output. Various non-adaptive and adaptive linearization approaches [1–7] have been adopted to correct these

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anomalies, so that the performance of the PA does not exhibit amplitude and phase distortions in the output.

Predistortion linearizers [7–16] are widely used in linearizing the PAs due to, their wide bandwidth, ease of use and their ability to be appended to existing amplifiers as a separate stand-alone module. The predistortion linearizers, in fact, introduce equal and opposite gain and phase distortion at the input of the PA to correct for the actual encountered distortion in the gain and phase characteristics of the final output.

Predistortion linearizers employing a microcontroller for the control of various parameters were reported in [7, 8]. These types of linearizers exhibit gain and phase characteristics opposite in orientation to that of the PAs to be characterized. They are very effective, but are bulky in size and are also complex. Moreover, enhancement in the performance of these linearizers can only be achieved through increased circuit complexity and cost. These issues can be overcome by employing amplitude and phase linearizing techniques that employ a series feedback amplifier with large source inductance [9]. This technique benefits from its small size and low DC power consumption, but can be applied only to PAs whose input power is more than 20 dBm.

A linearizer based on a series diode with a parallel capacitor [10] can overcome the limitations of the linearizer reported in [9]. This is a very simple linearizer and utilizes the nonlinearity of the series resistance of the diode, which produces a characteristic positive gain and negative phase with increasing input power. This is a miniature and simple configuration, but requires an additional isolation mechanism between the linearization circuit and the PA. In addition, this linearizer has very limited control on the achieved characteristics and thus finds very limited usefulness in practical applications.

The diode based linearizer reported in [17] is adaptable and provides control through bias feed resistance. The amplitude modulation/amplitude modulation (AM/AM) and amplitude modulation/phase modulation (AM/PM) characteristics of the linearizer can be easily adjusted by varying the supply voltage, V_{cc}, and in turn the bias voltage of the diode, V_d. However, this linearizer has complete dependence on the variation of a single design parameter; hence, the control in the achieved performance is severely limited. Moreover, this method requires an isolation mechanism between the linearizer and the PA.

The linearizer reported in [18] is an improved diode based linearizer, which is based on a parallel diode with bias feed resistance and also incorporates a 90° hybrid coupler for isolating the linearizer

and the PA. However, this linearizer has very limited control in achieving the desired characteristics, as it can only be controlled by just one variable i.e., the bias voltage of diode.

This paper presents a comprehensive design approach of a flexible, dual-inflection point, radio frequency (RF), predistortion linearizer along with its complex gain synthesis methodology, which surpasses the approaches reported in [17, 18]. The complete theoretical, mathematical and experimental evaluation is presented to demonstrate the flexible design and operation of the proposed dual-inflection point linearizer. This linearizer has three degrees of control for achieving the required output characteristics, is miniature, and also provides the required isolation between the linearization circuit and the PA that is to be linearized.

2. CONCEPTUALIZATION OF THE LINEARIZER

The linearization circuit proposed in this paper is based on the technique discussed in [19]. The original circuit was designed for linearizing a 35 W vacuum tube amplifier operating at 7 MHz. The linearizer reported in [19] is unsuitable for operation at microwave frequency, due to the inherent presence of memory effects, which can produce severe phase distortion.

The linearizer proposed in this paper retains the main principles of the earlier realized linearizer from [19], shown in Fig. 1. The

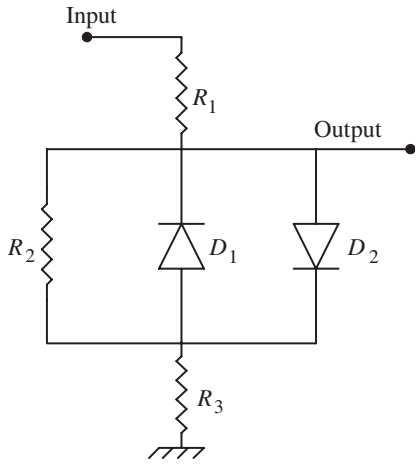

Figure 1. The basic linearization circuit with diodes connected in a head-tail configuration.

proposed linearizer utilizes two Schottky diodes connected in a head-tail configuration and a p-intrinsic-n (PIN) diode in parallel with the two Schottky diodes. The novelty of the proposed linearizer lies in the modifications, which allow it to become more flexible and adaptive for linearization of traveling wave tube amplifiers (TWTAs), as well as microwave solid state power amplifiers (SSPAs).

The most basic linearization circuit with diodes connected in a head-tail configuration is depicted in Fig. 1. It consists of semiconductor diodes as a nonlinear resistor in a divider arrangement, as initially reported in [19]. This configuration, however, suffers from linear phase distortions. This phase distortion can compound the AM/PM characteristic observed in the PA that is to be linearized. To mitigate this effect, the linearizer could be tuned to resonance at a center frequency, but the linearizer is a nonlinear circuit; hence, the resonance cannot be achieved for the full range of input signals.

At microwave frequencies, the problem is more severe as the capacitive effects of the junction capacitance, C_j, of the Schottky diodes limit the usefulness of this linearizer to a very moderate range of input signals. To overcome this capacitive effect, the resonance can be achieved by incorporating an appropriate inductance, L_s, in shunt, as shown in Fig. 2. With the incorporation of shunt inductance, L_s, the problem of linear phase distortion can be overcome for any input power and any bias voltage, V_{sch}, of Schottky diodes, D_1 and D_2. The actual bias voltage, V_{PK}, across the Schottky diodes, D_1 and D_2, configuration is regulated by the bias feed resistances, R_b, and the input RF power.

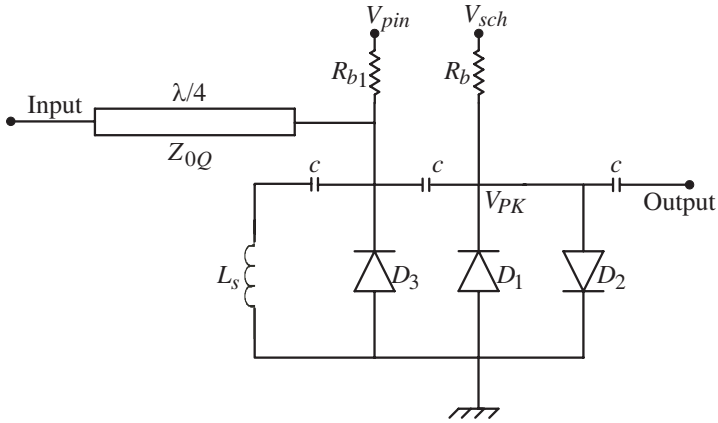

Figure 2. Configuration of the proposed linearizer circuit.

The PIN diode, D_3, offers a variable resistance in shunt to the Schottky diodes, D_1 and D_2. It serves two purposes: on one hand, it provides a dynamic control to obtain the required gain and phase characteristics; while on the other hand, it also provides the improved dynamic range in the gain and phase responses, which are governed by its bias voltage, V_{pin}. The actual bias of the PIN diode is regulated by the bias feed resistance, R_{b1}, and the input RF power. To ensure the proper operation of the linearizer in the high impedance region of the Smith chart, a fixed resistor controls the PIN diode. The linear resistance is the net fixed resistor in parallel with the resistance of the PIN diode and ensures that the impedance of the linearizer during operation does not get near the center of the Smith chart, i.e., the condition at which the linearizer loses the state of resonance.

The linearizer should have extremely low insertion loss and also exhibit very minimal phase dependent amplitude due to any residual diode reactance. For this purpose, it is imperative that the impedance of the diode configuration is transformed to a high value. The $\lambda/4$ line has characteristic impedance sufficiently high to transform the impedance of the semiconductor device approaching to an open circuit. The incorporation of the $\lambda/4$ line minimizes the phase dependent amplitude and also minimizes the insertion loss.

3. MATHEMATICAL ANALYSIS OF THE LINEARIZER

The analysis of the concept explained in the previous section is formulated here in detail. A simple block diagram of the linearizer is given in Fig. 3. The stimulus signal enters port-1 and exits port-4 of the 90° hybrid coupler. The stimulus signal is modified by the linearizer configuration attached at port-2 and port-3 of the coupler. The circuit configuration, L, shown in Fig. 4, generates a nonlinear reflection coefficient, Γ, which then relates the input signal, a_1, with the output signal, b_4, by the following matrix of the hybrid coupler:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 0 & 1 & -j & 0 \\ 1 & 0 & 0 & -j \\ -j & 0 & 0 & 1 \\ 0 & -j & 1 & 0 \end{bmatrix} \times \begin{bmatrix} a_1 \\ \Gamma \times b_2 \\ \Gamma \times b_3 \\ 0 \end{bmatrix} \tag{1}$$

where $a_2 = \Gamma \cdot b_2$ and $a_3 = \Gamma \cdot b_3$. Since port-4 is the transmitting port of the backward matched hybrid coupler, there is no reflected signal at this port i.e., $a_4 = 0$.

The following expression can be derived from (1):

$$b_4 = f(a_1) = -j \cdot \Gamma \cdot a_1 \tag{2}$$

The Equation (2) represents the variation of the signal at the output of

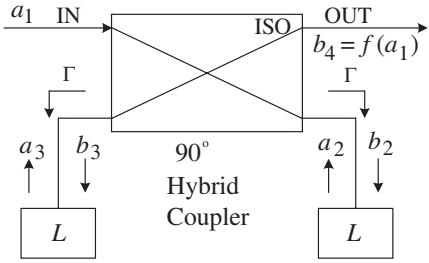

Figure 3. Block diagram of the linearizer with attached circuit configuration at port-2 and port-3.

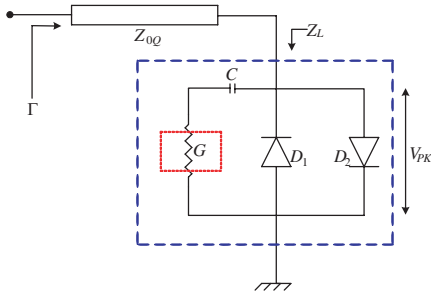

Figure 4. Circuit diagram depicting the inner description of configuration L.

the hybrid coupler depending on the input signal at port-1 of the hybrid coupler. As $|a_1|^2 = P_{IN}$ and $|b_4|^2 = P_{OUT}$, the following relationship for the output power versus input power for the linearization circuit can be derived:

$$P_{OUT} = |\Gamma|^2 P_{IN} \tag{3}$$

It is thus evident from (2) that the term $|\Gamma|^2$ regulates the gain and phase characteristics of the predistortion circuit.

The explanation for how the parameters of the coupler loading circuit, L, shown in Fig. 4 control the reflection coefficient, Γ, is described in the following paragraphs and equations. The parameter Z_{0Q} denotes the characteristic impedance of the line length, $\lambda/4$; Z_L is the total impedance presented by the diode network; V_{PK} is the sum of the biasing voltage and the rectified RF voltage across the Schottky diode configuration, P_{IN} is the input power; and, Γ is the reflection coefficient of the predistortion circuit, which needs to be determined. If P_{DISS} is the power dissipated in the network then:

$$P_{DISS} = P_{IN}\left(1 - |\Gamma|^2\right) \tag{4}$$

Since P_{DISS} is directly related to the electrical behavior of the network, the voltage across the Schottky diode configuration, V_{PK}, can be obtained as follows:

$$P_{DISS} = \frac{|V_{PK}|^2}{2 \cdot Re\{Z_L\}} = P_{IN}\left(1 - |\Gamma|^2\right) \tag{5}$$

where Z_L is the total impedance of the diode network consisting of two Schottky diodes, D_1 and D_2, in head-tail configuration and the PIN diode, D_3.

If Z_L is assumed to be real, then the above equation changes to:

$$|V_{PK}| = \sqrt{2 \cdot Z_L \cdot P_{IN} \left(1 - |\Gamma|^2\right)} \tag{6}$$

The above equation can be solved for the estimation of the reflection coefficient, Γ.

The Schottky diodes are used in a head-tail configuration; therefore, the net current of this diode configuration is given by:

$$i_D = I_S \left(e^{\lambda \cdot v} - 1\right) - I_S \left(e^{-\lambda \cdot v} - 1\right) = 2 \cdot I_S \cdot \sinh(\lambda \cdot v) \tag{7}$$

where i_D is the diode current, I_S represents the saturation current, and λ denotes a constant dependant on temperature ($\lambda = q/n \cdot K \cdot T$). Where q is the charge on an electron, n is the ideality factor, K is the Boltzman constant and T is the absolute temperature of p-n junction.

For an input signal of $V_{PK} \cdot \cos \omega_0 t$, the Blachman transformation [20] can be employed to transform (7) into a summation of current components given by:

$$i_D = 2 \cdot I_S \left[\sum_{m=1}^{\infty} 2I_m \left(\lambda V_{pk}\right) \cos(m\omega_0 t)\right], \quad m = 1, 3, 5 \ldots \tag{8}$$

where $I_m(\lambda \cdot V_{pk})$ is the modified Bessel function of first order for the integer values of m.

The magnitude of the fundamental component of the diode current can be deduced from (8) and given by:

$$i_D = 4 \cdot I_S \cdot I_1 \left(\lambda V_{pk}\right) \tag{9}$$

The admittance of the Schottky diode configuration can now be defined as:

$$y_D = \frac{i_D \left(V_{pk}\right)}{V_{pk}} = \frac{4 \cdot I_S \cdot I_1 \left(\lambda V_{pk}\right)}{V_{pk}} \tag{10}$$

The total admittance, Y_{TOTAL}, of the network is the parallel combination of y_D; and, the shunt admittance of the PIN diode is denoted by the parameter G.

$$Y_{TOTAL} = y_D + G = G + \frac{4 \cdot I_S \cdot I_1 \left(\lambda V_{pk}\right)}{V_{pk}} \tag{11}$$

Therefore, the total impedance of the diode network is given by the reciprocal of Y_{TOTAL}:

$$Z_L = \frac{V_{pk}}{G \cdot V_{pk} + 4 \cdot I_S \cdot I_1 \left(\lambda V_{pk}\right)} \tag{12}$$

The reflection coefficient, Γ, of the diode network can be written as:

$$\Gamma = \frac{\frac{Z_{0Q}^2}{Z_L} - Z_0}{\frac{Z_{0Q}^2}{Z_L} + Z_0} = \frac{Z_{0Q}^2 - Z_0 Z_L}{Z_{0Q}^2 + Z_0 Z_L} \tag{13}$$

where Z_0 is the characteristic impedance of the system.

Finally, the rearrangement of (12) and (13) gives the reflection coefficient, Γ, in terms of the design parameters, Z_{0Q}, G and V_{pk}:

$$\Gamma = |\Gamma| \measuredangle \phi = \frac{Z_{0Q}^2 \left[GV_{pk} + 4I_S I_1 \left(\lambda V_{pk}\right)\right] - V_{pk} Z_0}{Z_{0Q}^2 \left[GV_{pk} + 4I_S I_1 \left(\lambda V_{pk}\right)\right] + V_{pk} Z_0} \tag{14}$$

where $|\Gamma|$ is the magnitude of the reflection coefficient and ϕ is the phase of the associated reflection coefficient.

The term $|\Gamma|^2$ regulates the transfer characteristics as given in (3). It is thus evident from (14) that the transfer characteristics can be controlled by varying the parameters impedance of the $\lambda/4$ line (Z_{OQ}), the admittance of the PIN diode (G), and the voltage across the Schottky diode configuration (V_{PK}). The next section presents simulation results to show the effects of the variation of the design parameters on the transfer characteristics of the linearizer, thereby demonstrating the flexibility of the operation of the proposed linearizer.

4. EVALUATION OF THE LINEARIZER CONCEPT

As previously described, the characteristics of the proposed linearizer can be controlled by i) varying the bias voltage across the Schottky diode configuration; ii) the admittance of the PIN diode, i.e., the bias voltage of the PIN diode; and, iii) the shunt inductance, L_s.

It can be deduced from (14) that the reflection coefficient, Γ, gets smaller with an increase in the bias voltage, V_{PK}, of the Schottky diode. The smaller Γ results in a smaller gain of the linearizer, as can be seen in (3). This phenomenon is also evident in the results displayed in Fig. 5. It can thus be concluded that, by changing the bias voltages of the Schottky diode configuration, V_{sch}, and at the same time keeping a fixed bias voltage of the PIN diode, V_{pin}, one can achieve the effect of delay in the conduction of the Schottky diode. The shifts in the transfer characteristic along the axis of P_{IN} is due to the presence of series bias feed resistance, R_b, shown in Fig. 2. This shift is due to the increasing voltage drop across this bias feed resistance R_b with the increase in RF input power, P_{IN}. Therefore to maintain the Schottky diode in conduction it will require higher V_{sch} than the value used at low input power, and it is consistent with the result reported in [17].

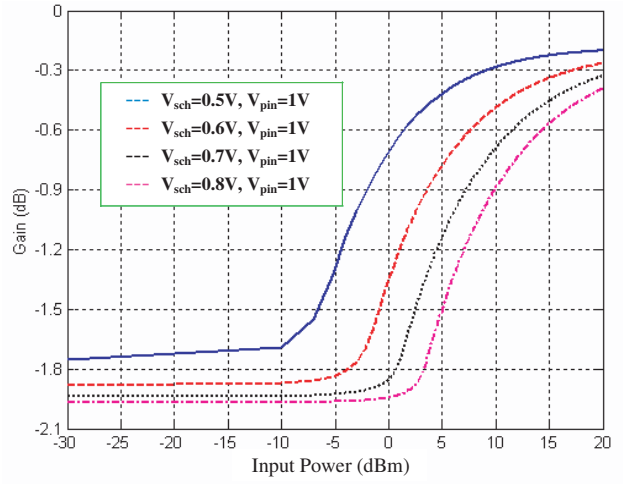

Figure 5. The theoretical characteristic of the predistortion circuit for varying values of the Schottky diodes' bias voltage.

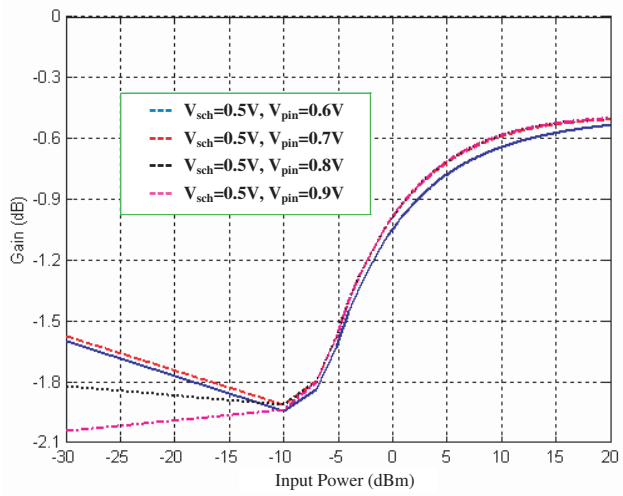

Figure 6. The theoretical characteristic of the predistortion circuit for varying values of the PIN diode's bias voltage.

The admittance, G, of the PIN is controlled by the bias voltage, V_{pin}. The effect of V_{pin} on the characteristic of the linearizer is shown in Fig. 6. The plot displays the family of curves for a fixed bias voltage, V_{sch}, for the Schottky diodes, while changing V_{pin}. It can be seen that the effect of delay in conduction was maintained, but the change in

the bias voltage of the PIN diode influenced the transfer characteristic for low powers. The dynamic range of the linearizer can, therefore, be managed by controlling the bias voltage of the PIN diode; and, it eventually helps in achieving the required compression in the gain characteristics for the linearizer.

The impact of the varying shunt inductance, L_s, on the gain characteristics is shown in Fig. 7. The results show the gain characteristics of the linearizer for four different inductance values, while the bias voltage of all the diodes was kept at a fixed level. This family of curves shows no deviation; and, it clearly demonstrates that the shunt inductance, L_s, resonates out the effect of the junction capacitance, C_j, of the Schottky diodes. Thus, the deployment of an appropriate value for the shunt inductance, L_s, in the linearizer mitigates the effect of C_j, which in turn prevents the linearizer from possessing any memory effects. The selection of the value of L_s is regulated by the bias voltage of Schottky diodes, as the junction capacitance, C_j, is dependent on the bias voltage.

From the above analysis, it is apparent that the combined changes in the design variables provided a wide variety of control for the transfer characteristics, thereby making the proposed linearizer very flexible. It has been demonstrated that the linearizer possesses three degrees of freedom; and, three different families of curves can be obtained with

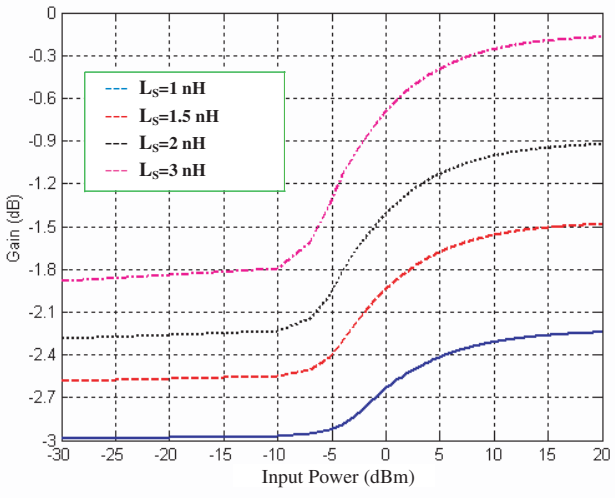

Figure 7. The theoretical characteristic of the predistortion circuit for varying values of the shunt inductance, L_s, while keeping $V_{pin} = 0.8\,\mathrm{V}$ and $V_{sch} = 0.6\,\mathrm{V}$.

this circuit for each situation, i.e., curves for the variation of the bias voltage for the Schottky diodes, the bias voltage of the PIN diodes, and the shunt inductance, L_s. Based on the requirements, any or all of the parameters can, therefore, be altered to achieve the desired characteristics.

5. DESIGN AND VALIDATION OF THE LINEARIZER

Through mathematical analysis and simulation, it has been established that the proposed linearizer provides the flexibility for achieving the desired characteristics by the variation of either bias voltages of the Schottky diodes or PIN diode, or by varying the shunt inductance, L_S. It is shown in this section that careful consideration of the linearizer's design and parameters allows it to obtain the two inflection points' gain characteristics exhibited by a gallium arsenide field effect transistor (GaAs FET) device.

To validate the performance of the linearizer, first a 1 W GaAs FET device was selected; and, its normalized inverse gain and inverse phase characteristics are given in Figs. 8 and 9, respectively. It can be determined from Fig. 8 that the inverse gain characteristics showed a dynamic compression of −0.16 dB and then an expansion of 1.18 dB. This gives a total dynamic characteristic of 1.34 dB. Fig. 9 shows that the GaAs FET device exhibited phase distortion of 10.25 degrees at

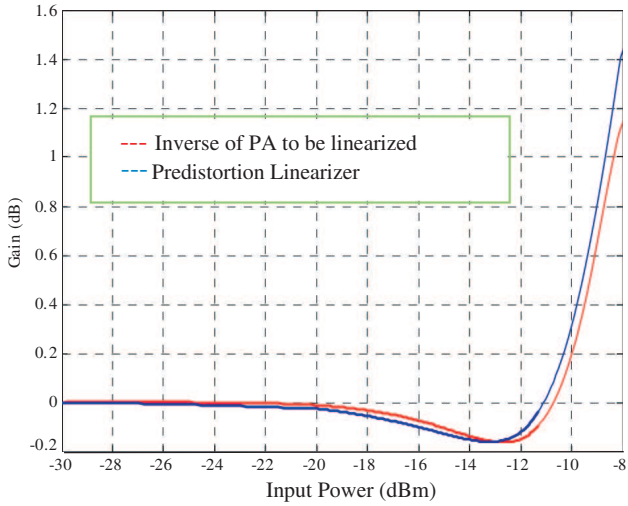

Figure 8. The gain characteristics of the linearization circuit and the inverse gain characteristics of the amplifier to be linearized.

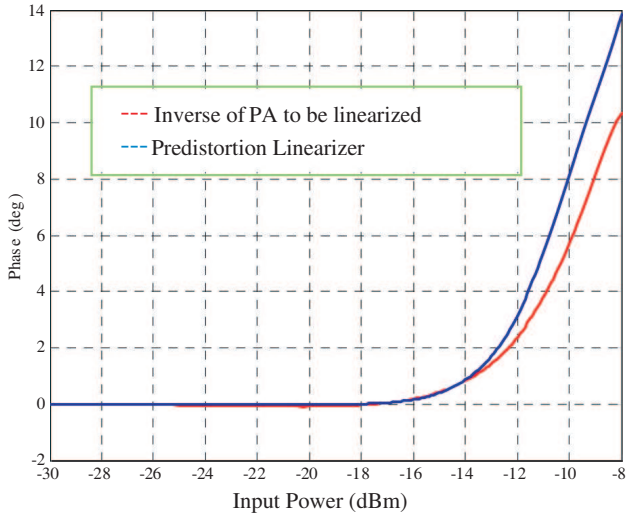

Figure 9. The phase characteristics of the linearization circuit and the inverse gain characteristics of the amplifier to be linearized.

the 1-dB compression point. The linearizer should, therefore, be able to replicate similar characteristics to remove the effect of AM/AM and AM/PM from any PA employing this GaAs FET device.

To achieve a linearizer with dynamic characteristics similar to the inverse characteristics of the PA that is to be linearized, a prototype was built based on the concept presented in the previous sections. The linearizer was built on a RT/5880 duroid substrate with a dielectric constant of 2.2 and thickness of 0.508 mm. Decoupling capacitors, C, as shown in Fig. 2, were needed to isolate the bias circuit and the RF signal paths and were chosen in such a way that they had an impedance of less than 10% of the characteristic impedance of the circuit, in order to create a short circuit at the operating frequency of the RF circuit. For an operation range of 1.4–2.8 GHz, the minimum value of C was calculated to be at least 15.91 pF; therefore, capacitors with values of 100 pF were chosen. The chosen PIN and Schottky diodes were from Agilent, while the chosen 90° hybrid coupler is from Anaren.

For achieving the gain and phase characteristics similar to the inverse of the GaAs FET device shown in Figs. 8 and 9, a simulation was performed prior to the design; and, the bias voltage for Schottky diodes was determined to be 0.6 V, while the bias voltage for the PIN diode was found to be 0.8 V. To remove the effects of memory due to frequency dispersion from the linearizer characteristics, a shunt inductance of 1.33 nH was needed; therefore, the linearizer prototype utilized the inductance 0604HQ from Coilcraft with a value of 1.5 nH.

The measured gain and phase characteristics of the linearizer prototype are superimposed in Figs. 8 and 9, respectively. It is evident from Fig. 8 that the gain characteristics of the linearizer achieved two inflection points and were very similar to the inverse gain characteristics of the 1 W GaAs FET device. The slight difference in the gain characteristics of the linearizer was the result of the usage of a slightly higher value for the shunt inductance, L_s, in the built prototype.

The phase characteristic of the linearizer, shown in Fig. 9, replicated the inverse of the phase characteristics of the GaAs FET device to be linearized. Although there was the requirement of only 10.25 degrees, the predistortion linearizer produced around 13.75 degrees of nonlinear phase at the 1-dB compression point. This small anomaly was due to the use of a slightly higher value of shunt inductance and the trade-off applied in the determination of requisite bias voltages for the diodes.

Overall, it is apparent from the above results that the developed predistortion topology achieved the desired characteristics to linearize the 1 W GaAs FET device with two inflection points in the gain and was also capable of significantly minimizing the phase distortion. The three degrees of control in the linearizer provided this flexibility; and, these three design parameters can be easily altered to linearize other GaAs FET based PAs.

6. EXPERIMENTAL VALIDATION OF THE LINEARIZER

This linearizer can work for a single carrier, two carriers or any complex modulation. In the current investigation, the two-carrier method was selected to carry out and validate the performance of linearization circuits. This method is simple, quick and easy to comprehend and gives ample proof of the functionality of the linearizer. The block diagram for performing the two-tone test is shown in Fig. 10.

The experiment was performed on a commercial ZHL-4240 from Mini-Circuits that utilizes a 1 W GaAs FET device. The variable attenuator and pre-amplifier were used to align the predistorter with the PA that was to be linearized, such that:

$$P^{PD}_{Out\_\mathrm{Max}G} = P^{PA}_{in-Sat} \tag{15}$$

where $P^{PD}_{Out\_\mathrm{Max}G}$ represents the output power at the predistorter when it is under the condition of maximum gain expansion, and P^{PA}_{in-Sat} is the input power for saturating the power amplifier. This also ensures

that the input power to the solid state power amplifier is the same as when the power amplifier is operated without the linearizer.

First, the power amplifier was excited by a single tone stimulus; and, the 1-dB compression point was found. For investigation and evaluation purposes, the two-carrier frequencies were chosen at $f_1 = 1.625\,\text{GHz}$ and $f_2 = 1.635\,\text{GHz}$. Then, the input power for the two tones was reduced in a symmetric manner; and, measurement was carried out for the carrier output power along with the third- and fifth-order intermodulation distortion (IMD). The ratios of carrier output power to the respective third-order IMD, *C/IMD3*, and fifth-order IMD, *C/IMD5*, are displayed in Figs. 11 and 12.

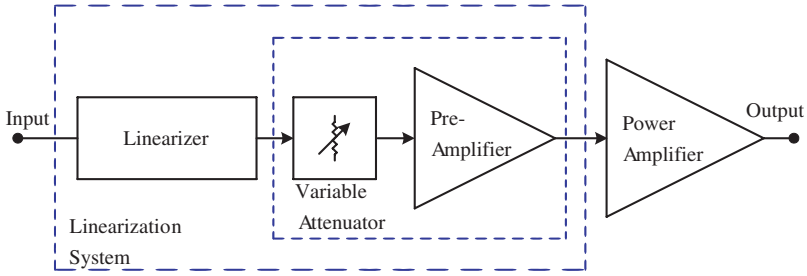

Figure 10. Block diagram of the linearization system for RF predistortion.

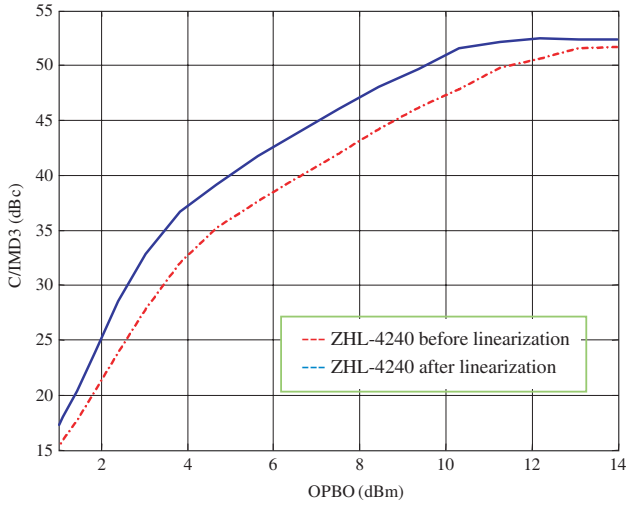

Figure 11. C/IMD3 vs. OPBO for amplifier ZHL-4240 before and after linearization.

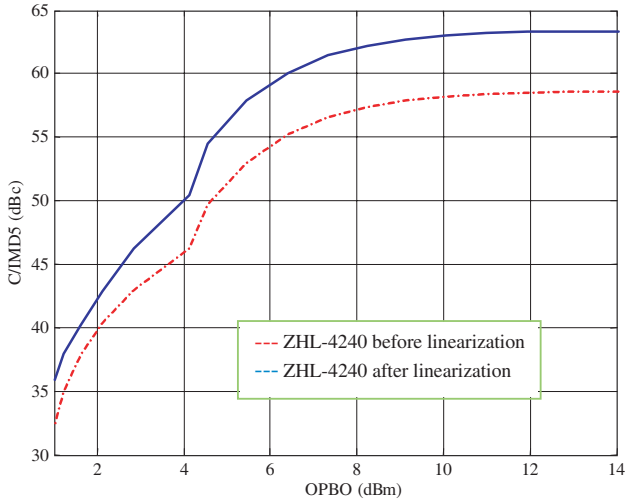

Figure 12. C/IMD5 vs. OPBO for amplifier ZHL-4240 before and after linearization.

The same experiment was repeated with the incorporation of the linearization block at the input of the amplifier. *C/IMD3* and *C/IMD5* after linearization are also shown in Figs. 11 and 12, respectively. From the above measurement results, it is apparent that the best *C/IMD3* was obtained for the output power back-off (OPBO) of 4.5 dBm. The improvement in *C/IMD3* and *C/IMD5* values at 4.5 dBm OPBO was 7.61 dBc and 9.48 dBc, respectively. These results are acceptable, as the utilized PA did not show very nonlinear behavior, considering that ZHL-4240 is a well-behaved commercial PA, as can be seen from the obtained results in Figs. 11 and 12. Nonetheless, the operating principle of the developed predistortion linearizer was demonstrated by the improvement in *C/IMD3* and *C/IMD5* of a commercial PA.

The linearizer's performance can be further estimated by considering the spectrum of the linearized PA and the nonlinearized PA. The experiment was performed for an OPBO of 4.5 dBm; and, the PA was excited by a two-tone carrier signal. The resulting spectrum, before and after linearization, is depicted in Fig. 13. The analysis of the results clearly shows that the improvement in the lower *C/IMD3* was 7.9 dBc, while this improvement in the upper *C/IMD3* was 8.1 dBc. The respective improvements in *C/IMD5* were 9.6 dBc and 9.8 dBc. This is consistent with the results shown in Figs. 11 and 12.

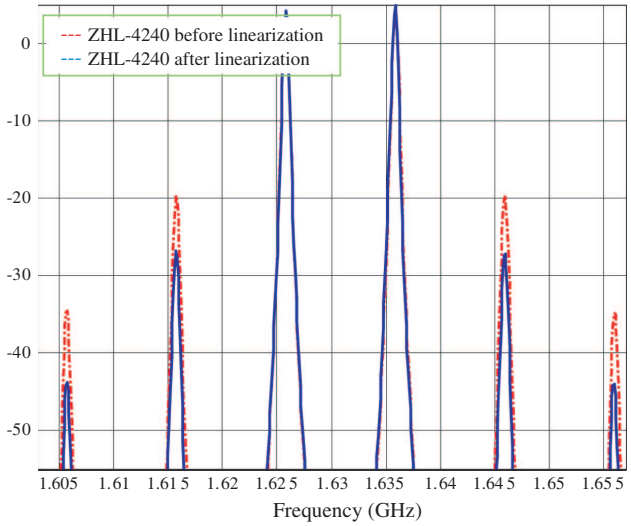

Figure 13. C/IMD with two carriers at $f_1 = 1.625\,\text{GHz}$ and $f_2 = 1.635\,\text{GHz}$ for 4.5 dB OPBO before and after linearization of the ZHL-4240 power amplifier.

7. CONCLUSION AND DISCUSSION

A new, miniature, dual-inflection point, analog, predistortion linearizer using a head-tail Schottky diode configuration, complemented with a PIN diode in shunt, has been presented. The linearizer possesses three degrees of control to achieve the desired output characteristics through i) control of the bias voltage of the Schottky diodes, ii) control of the conductance of the PIN diode, and iii) control of the shunt inductance, L_s, for mitigating memory effects. To verify functionality, a 1 W GaAs FET device was taken as a case study; and, the proposed linearizer's characteristic was controlled by the design parameters, V_{PK}, V_{pin} and L_s, to replicate the inverse characteristics of the GaAs FET device. The results clearly show a concurrent reduction of third- and fifth-order distortion over a wide dynamic range. Finally, measurements on a commercial power amplifier, ZHL-4240 based on a GaAs FET device, demonstrated the successful operation of the proposed linearizer.

ACKNOWLEDGMENT

The authors would like to acknowledge the financial support from Alberta Informatics Circle of Research Excellence (iCORE), the

Natural Sciences and Engineering Research Council of Canada (NSERC) and Canada Research Chair (CRC) program. The authors are also thankful to the staffs of the iRadio Lab for the technical assistance.

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