A 900-MHz 30-dBm BULK CMOS TRANSMIT/RECEIVE SWITCH USING STACKING ARCHITECTURE, HIGH SUBSTRATE ISOLATION AND RF FLOATED BODY

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Abstract—This paper presents comprehensive methods for the design of a 900-MHz CMOS transmit/receive (T/R) switch with high power-handling capability. Techniques such as RF floated body to extend the bandwidth and decrease the insertion loss, and stacking architecture with high substrate isolation to enhance the power-handling capability

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are used for the design of a T/R switch on a standard 0.18 μm triple-well CMOS process. The measured performance of the T/R switch demonstrates the effectiveness of the methods presented in this paper such that insertion loss less than 1.0 dB, isolation up to 35.2 dB, and input 1-dB compression point of 30-dBm can be achieved at 900-MHz.

1. INTRODUCTION

Gallium-Arsenide (GaAs) has been dominating high-performance RF front-end module and RF IC markets due to its excellent characteristics of semi-insulating substrate with both high breakdown voltage and high electron mobility [1–7]. In recent years, CMOS technology is extending its applications to the fields originally served by GaAs because of the speed improvements of the CMOS transistors. In spite of lossy silicon substrate, low-cost and fully integrated CMOS RF transceivers are in great demand with the explosive growth of wireless applications. RF IC designers have aggressively realized various RF blocks like LNA, mixers, and VCO by using CMOS technology and integrated them on the same silicon substrate. Following the previous success of the integrated CMOS RF transceivers, various CMOS T/R switches have been developed at different frequencies to further increase the level of the integration of RF CMOS front-ends [8–17]. Huang and Kenneth presented the design of a transmit/receive (T/R) switch with low insertion loss (IL) and improved 1-dB compression point (P1 dB) at 0.9- and 2.4-GHz by using off-chip impedance transformation network, sufficient substrate contacts, and optimized device sizes [8, 9]. The effects of high and low substrate resistance on the design of a 5.8-GHz CMOS T/R switch were discussed [10]. It has been demonstrated that the linearity of the CMOS T/R switch can be further improved by using stacking architecture and depletion-layer-extended transistors (DETs) [11]. By utilizing LC-tuned circuit to bias the substrate in the transmit (TX) path and matching network in the receive (RX) path, Talwalker et al. proposed novel designs of two CMOS switches [12, 13] operating at 2.4- and 5.2-GHz, of which the input 1-dB compression point (IP1 dB) of 28.5-dBm and insertion loss of 1.5 dB have been achieved. Due to the tuned LC circuits, the operation of these two switches is limited in a narrow frequency range. The body-floating technique is presented to improve the power performance of the CMOS T/R switch where the reported IP1 dB is 20-dBm with IL of 1.1 dB at 5.8-GHz [14]. Besides, A 0.35-μm CMOS T/R switch using enhanced compact waffle MOSFETs and a 3-V supply voltage gives an insertion loss of 1.7-dB, high isolation of more than

40-dB, and 7-dBm IP1 dB at 900-MHz [15]. T/R Switch for mobile
phone applications must have a high linearity to ensure that the high
power signals at the output of the PA are reliably transmitted to the
antenna with minimum loss. Recently, a 900-MHz CMOS T/R switch
with IP1 dB of 31.3-dBm and IL of 1 dB has been demonstrated by
using the control voltage from 2 to 6 V [16]. This work suggests that
integration of a bulk CMOS T/R switch for cellular applications is a
realizable goal.

This paper presents effective methods composed of RF floated
body and stacking architecture with high substrate isolation from
careful layout consideration to expand the working bandwidth,
decrease the IL and increase the IP1 dB of CMOS T/R switches. In
Section 2, which is the starting point toward the aim of this paper,
the method using RF floated body to design a NMOS switch with low
insertion loss is developed. In Section 3, the effects of the substrate
coupling which can devastate the linearity of a conventional non-
stacking shunt-series T/R switch are discussed. Then a method to
guarantee sufficient substrate isolation is proposed and verified. In
Section 4, an approach to design a stacking T/R switch which combines
RF floated body, high substrate isolation, and stacked transistor to
improve the linearity of the T/R switch is presented. The measurement
results of the insertion loss and the IP1 dB of the RF T/R switch
designed in this paper is demonstrated in Section 5. By applying
the presented methods, a 900-MHz CMOS T/R switch fabricated
on a standard 0.18-μm triple-well CMOS process shows satisfying
performance that a IP1 dB of 30-dBm in the TX path, and insertion
loss of 1 dB and 0.94 dB in the TX and RX paths, respectively, are
achieved.
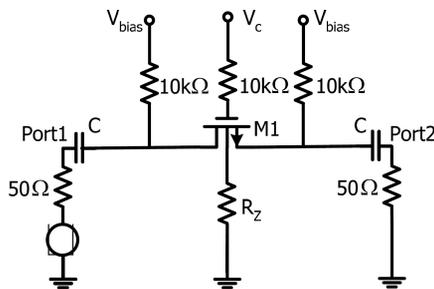
Figure 1. The single-transistor switch in a 50-Ω system.

2. DESIGN OF SINGLE-TRANSISTOR SWITCH

The standard 0.18-µm CMOS process used to fabricate the switch offers a deep N-well layer which separates the body of NMOS from the common substrate. Therefore, the body of the NOMS over the deep N-well becomes RF floated when it is connected to the ground through a large resistance. The impact of the body-to-ground resistance on the insertion loss of the single-transistor CMOS switch is analyzed at 900-MHz and the associated configuration is shown in Fig. 1. The voltage V_{bias} equal to 1.5 V provides the bias to both of the drain and source of the transistor through resistors of 10-kΩ which play the role of RF choke. The voltage V_c controls the on (3 V) and the off (0 V) of the switch through a resistor of 10-kΩ connected to the gate to make the gate RF floated. The body is biased through a large resistance R_Z to become a RF floated body. Fig. 2 shows the curves of insertion loss versus R_Z for 0.9-, 1.9- and 2.4-GHz when the switch is in the on state. The IL is approaching a minimum constant and becomes frequency independent when R_Z is larger than 10-kΩ, which makes the insertion loss of the NMOS transistor mainly determined by the on-resistance of the transistor. It is also evident from modified Fig. 2 that the IL is gradually becoming frequency dependent when R_Z is smaller than 10-kΩ. Under the condition $R_z < 10$-kΩ, except for the RF power consumed by the on-resistance of the NMOS, the RF energy leaking to the substrate through R_z severely impacts the insertion loss.

In addition, when the body of the single-transistor switch is connected to the ground via a large resistance, the transient voltage of the P-well bulk is boot-strapped to the signal voltage on the source and drain. This prevents the source-bulk and drain-bulk diodes from
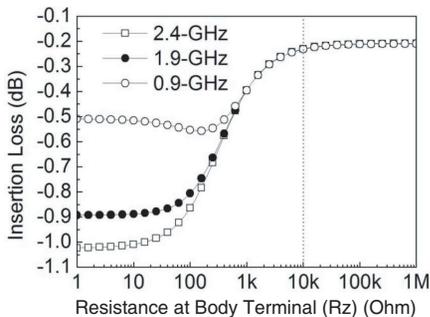
Figure 2. Simulated insertion loss versus R_Z at 0.9-, 1.9-, and 2.4-GHz for the single-transistor switch.
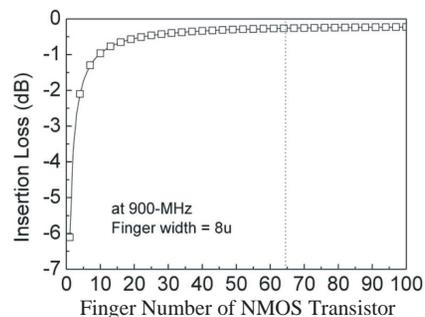
Figure 3. Effects of the transistor finger number on the insertion loss of the single-transistor switch.
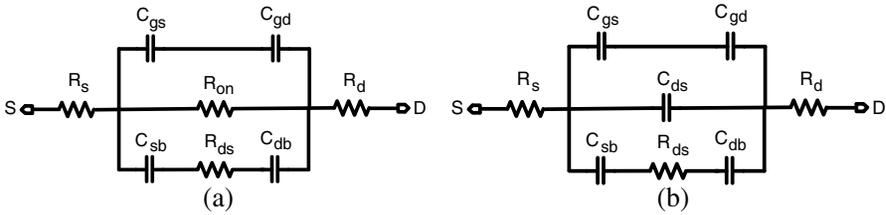
Figure 4. Small-signal models of NMOS transistor with RF floated gate and body under: (a) On state and (b) off state.

being turned on by large-swing signals. Therefore, the RF floated body is capable of avoiding signal self-clipping and improving the linearity of the single-transistor switch.

To optimally determine the size of the single-transistor switch, Fig. 3 shows the simulated input-to-output insertion loss as a function of the finger number of M1 when the body is RF floated by a resistor of 10 kΩ. Every single finger width used in the simulation is 8-μm. It is shown in Fig. 3 that when the finger number is increased, the insertion loss gradually decreases due to channel's on-resistance becoming smaller. As the transistor operates in the linear region, the on-resistance can be roughly given by a well-known equation as follows:

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}, \tag{1}$$

In other words, the on-resistance is inversely proportional to the total width of the transistor. On the other hand, when the finger number is increased, the input-to-output isolation decreases due to the existence of larger parasitic capacitances between the terminals of the transistor. Over high frequencies, these capacitances can further degrade the input-to-output isolation. Consequently, it is necessary to pay close attention to the layout of the NMOS transistor to minimize parasitic capacitances. In this paper, finger number equal to 64 is selected since it can lead to a lower insertion loss as shown in Fig. 3 and sufficient isolation.

For a transistor with a total channel width of 512-μm, of which the gate and source (drain) are respectively biased at 3 V and 1.5 V, the simulation-derived on-resistance R_{on} is about 4 Ω. Simplified small-signal equivalent models of the on- and off-states of the single-transistor switch with RF floated body and RF floated gate are shown in Fig. 4. R_{ds} represents the resistive loss in the P-well between source and drain. C_{gs} and C_{gd} represent the gate-to-source and gate-to-drain overlapping capacitances. C_{db} and C_{sb} are the drain-to-body and source-to-body junction capacitances, respectively. C_{ds} is primarily

due to the capacitance between source and drain diffusion areas. The IL measures the small signal power loss of the NMOS when it is turned on. The value of IL could be expressed as

$$IL = \frac{1}{|S_{21}|^2} = \left(\frac{2Z_0 + Z_{on}}{2Z_0}\right)^2, \tag{2}$$

$$Z_{on} = \frac{\begin{array}{l}\left[R_{on}\left(1 - \omega^2 C_G C_B R_{on} R_{ds}\right)\right.\\ \left.+\omega^2 C_B R_{ds} R_{on}\left(C_G R_{on} + C_B R_{ds} + C_B R_{on}\right)\right]\\ +j\omega R_{on}\left[C_B R_{ds}\left(1 - \omega^2 C_G C_B R_{on} R_{ds}\right)\right.\\ \left.-\left(C_G R_{on} + C_B R_{ds} + C_B R_{on}\right)\right]\end{array}}{\left(1 - \omega^2 C_G C_B R_{on} R_{ds}\right)^2 + \omega^2\left(C_G R_{on} + C_B R_{ds} + C_B R_{on}\right)^2},$$

$$C_G = \frac{C_{gs} \times C_{gd}}{C_{gs} + C_{gd}}, C_B = \frac{C_{sb} \times C_{db}}{C_{sb} + C_{db}}, C_T = C_G + C_{ds} + C_B, \tag{3}$$

where the complex impedance Z_{on} represents the total on-state impedance in Fig. 4(a). In addition, the isolation is written as

$$\text{Isolation} = \frac{1}{|S_{21}|^2} = \left(\frac{2Z_0 + Z_{off}}{2Z_0}\right)^2,$$

$$Z_{off} = \frac{\omega^2 C_B R_{ds}\left(C_T - C_G - C_{ds}\right) - j\omega\left[C_T + \omega^2 C_B^2 R_{ds}^2\left(C_G + C_{ds}\right)\right]}{\omega^4 C_B^2 R_{ds}^2\left(C_G + C_{ds}\right)^2 + \omega^2 C_T^2}, \tag{4}$$

where Z_{off} represents the total off-state impedance in Fig. 4(b).

Generally speaking, the value of C_{ds} is larger than any other capacitances and therefore it dominates the drain-source coupling effect in the off state. The input-to-output isolation can be improved by lowering C_{ds} with the careful layout of the NMOS transistor.

3. DESIGN OF NON-STACKING SWITCH CIRCUIT

In this section, we present the design methods of the T/R switch circuits with conventional series-shunt, non-stacking architecture as shown in Fig. 5(a). The cross section of NMOS transistor is shown in Fig. 5(b). The series transistors, M2 and M3, provide switching functions for transmit and receive paths. The shunt transistors, M1 and M4, are utilized to effectively improve the TX-to-RX isolation. The resistors of 10-kΩ are connected to the gates and bodies of M1 ∼ M4. The resistors make the bodies and gates of M1 ∼ M4 RF floated to decrease IL as described in Section 2. The shunt transistors, M1 and M4, improve the TX-to-RX isolation because of the carefully selected sizes of the transistors. The switching control voltages at the gates of M1 ∼ M4 are 3 V (on) and 0 V (off). The drain and source nodes
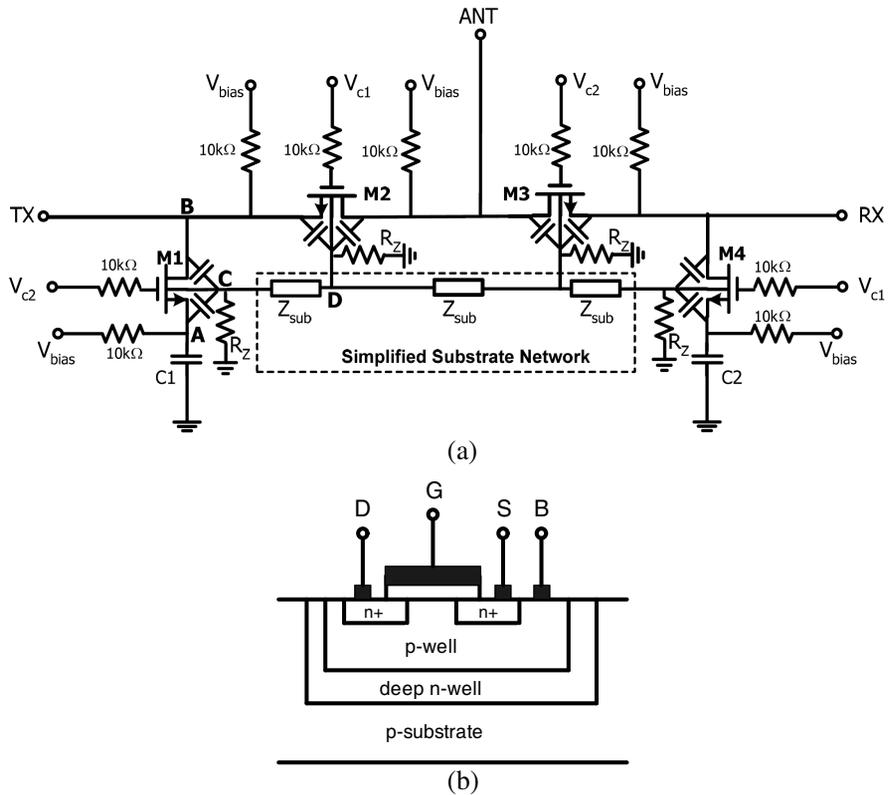
Figure 5. (a) The circuit schematic of the non-stacking T/R switch circuit including simplified junction capacitances and the substrate network. (b) The cross section of NMOS transistor.

of M1 ∼ M4 are biased at 1.5 V. These voltages are selected to lead to smaller C_{sb} and C_{db} of the NMOS transistors and therefore they can improve the insertion loss and the TX-to-RX isolation of the T/R switch. The width of M2 and M3 (W_{M2} and W_{M3}) are chosen to be 512-µm as analyzed previously to optimally obtain low insertion loss and adequate isolation for the conventional series-shunt T/R switch. According to the simulation results, the width of M1 and M4 are chosen to be 96-µm which can improve the isolation of the switch circuit by more than 10 dB with negligible impact on the insertion loss of the switch.

By assuming that the transistors in Fig. 5 are independent without considering the interconnects of the bodies through the substrate, Fig. 6 shows simulated transient voltage waveforms at the body
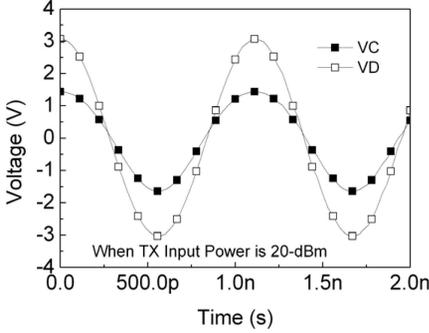
Figure 6. Voltage waveforms at the body terminals C and D of the non-stacking T/R switch circuit when TX input power is 20-dBm.
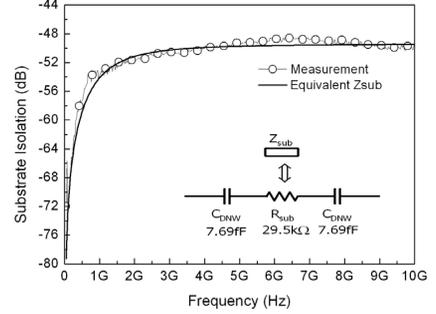
Figure 7. Measured and simulated substrate isolation of the 200-μm physical spacing versus frequency.

terminals C and D of M1 and M2 when TX input power is 20-dBm and RX path is turned off. Under the ideal assumption that M1 and M2 are independent, the voltage swing of V_C is about half that of V_D. However, considering the real condition for the transistors M1 and M2 sharing the same silicon substrate, V_D can be quite close to V_C if the substrate coupling between the transistors is severe. This condition will degrade the linearity of the T/R switch. Low impedance between the bodies of the transistors in the substrate can create unwanted electrical paths, called substrate network, and cause severe coupling between the transistors. In general, the substrate network can be represented by a complex combination of parasitic resistances and capacitances. For simplifying the following analysis, equivalent impedance Z_{sub} instead of the distributed R-C network is used to denote the impedance between the bodies of the transistors as shown in Fig. 5. In this paper, to ensure that the substrate coupling is dwindled without degrading the linearity of the T/R switch, a 200-μm physical spacing is reserved between the NMOS transistors of the T/R switch circuit. The measured substrate isolation of the 200-μm spacing in series with two deep N-well in the substrate reveals that substrate coupling between the transistor is less than -49 dB from DC to 10-GHz as shown in Fig. 7. The equivalent circuit of the Z_{sub} extracted from the measured scattering parameters is also shown in Fig. 7 which is given by

$$\text{Substrate\_Isolation} = \frac{2Z_0}{Z_{sub} + 2Z_0}, \ Z_0 = 50\,\Omega, \tag{5}$$

$$Z_{sub} = \frac{2Z_0(1 - \text{Substrate\_Isolation})}{\text{Substrate\_Isolation}} = R_{sub} + \frac{2}{j\omega C_{DNW}}, \tag{6}$$

The extracted real part R_{sub} is 29.5-kΩ and the extracted capacitance C_{DNW} is 7.69 fF. The equivalent circuit is added to the schematic of the T/R switch in Fig. 5 and the simulation results shows that the IP1 dB of the switch is identical to the one based on the ideal condition. That is to say, high substrate isolation between the transistors can be guaranteed by using the proposed 200-μm spacing. With the existence of high substrate isolation, RF floated bodies of the transistors are effective to sustain large voltage swing and the T/R switch can have a good performance in terms of linearity and power-handling capability.

4. DESIGN OF STACKING SWITCH CIRCUIT

In order to improve the power-handling capability of the T/R switch, a T/R switch circuit with stacking architecture is implemented as shown in Fig. 8. The transmit path of the switch is constructed with a single transistor M7 (width = 512-μm) as the design presented in Section 3. To support the TX port operating under higher power, six series
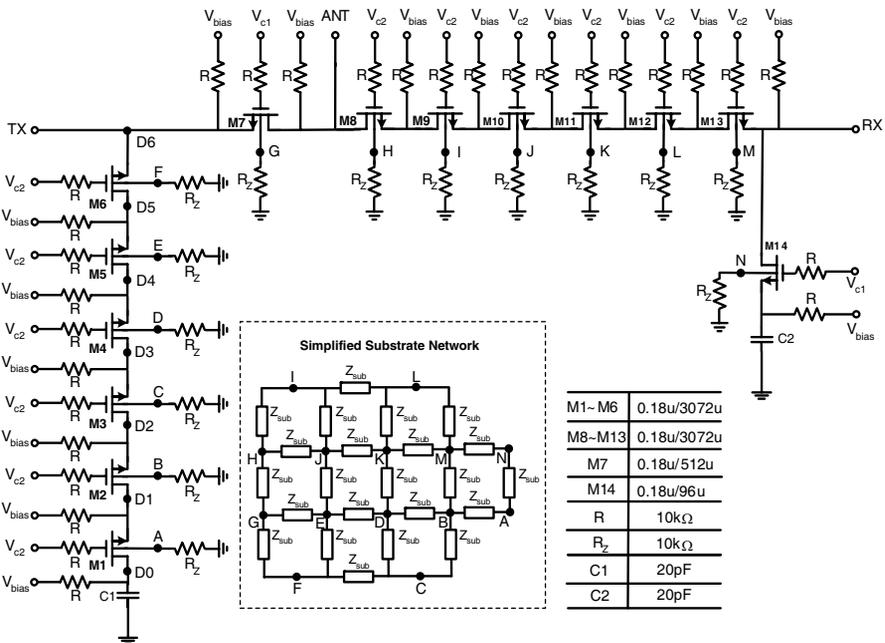
Figure 8. The circuit schematic of stacking CMOS T/R switch including simplified junction capacitances and the substrate network.

transistors M8-M13 (width = 3072-μm) are placed in the receive path.
The width of 3072-μm is selected to keep the insertion loss resulted by
M8-M13 of the RX path close to that of a single transistor with width
of 512-μm as shown in Section 3. In the shunt path, six transistors M1-
M6 (width = 3072-μm) are placed at the TX node to support a higher
input power and one transistor M14 (width = 96-μm) is placed at the
RX node to maintain a high TX-to-RX isolation. The bias condition
of the stacking T/R switch is the same as that of the non-stacking
T/R switch presented in the previous Section. The gates, sources,
and drains of all NMOS transistors are biased through on-chip non-
silicide polysilicon resistors of 10-kΩ. However, the bodies of all NMOS
transistors are RF floated through on-PCB surface-mounted devices
(SMD) to reserve the flexibility of changing the SMD for potentially
inadequate RF floated level of the bodies. The on-off switching control
voltages at the gates of the transistors are 3 V and 0 V. The sources
and drains of NMOS transistors are all biased at 1.5 V to maintain a
low on-state insertion loss and a high off-state isolation of the stacking
T/R switch.

Theoretically, compared to the non-stacking T/R switch, the
stacking T/R switch is capable of supporting sextuple AC voltage
swing at the TX node. By referring to Fig. 8, when the signal is
transmitted from the TX node to the ANT node, M7 is turned on
and the stacked shunt transistors M1–M6 and the series-connected
transistors M8–M13 are in the off state. Given that all transistors
keep high substrate isolation from each other, the voltage across the
path composed of the off-state M1–M6 and M8–M13 will be divided
evenly by drain-to-gate and gate-to-source capacitances due to the
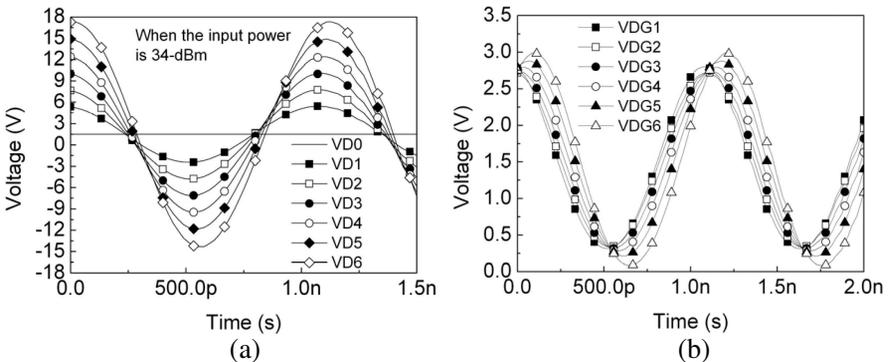
Figure 9. (a) Simulated voltage swings along the TX shunt arm. (b)
Drain-to-Gate voltages for M1 ∼ M6 when TX input power is 34-dBm.

symmetrical structure of M1–M6 and M8–M13. The even distribution of the signal voltage swing among M1–M6 and M8–M13 prevents the transistors from over-driven condition and is the principle with which the stacking T/R switch can ideally sextuple the voltage swing at the TX node without clipping the signal itself as shown in Figs. 9(a) and 9(b). However, the voltage-handling capability of the stacking T/R switch can degenerate to behave as a conventional non-stacking T/R switch when strong coupling between the transistors exists in the substrate. The strong substrate coupling can devastate the even distribution of the voltage among the off-state transistors and decrease the linearity of the stacking T/R switch.

The impact of the stacking number on the TX/RX insertion loss and TX IP1 dB is analyzed with EDA tools and the results are shown in Figs. 10(a) and 10(b). With Fig. 10(a) we can see that the simulated TX/RX insertion loss and TX IP1 dB will increase as the number of the stacking transistors is increased. However, in Fig. 10(b), we can observe that the IP1 dB of the T/R switch is approaching saturation as the stacking number increases. The mechanism to limit the IP1 dB of the stacking T/R switch in the TX path can be explained as follows. When the TX input power approaches the input referred 1-dB compression point, M6 and M8 suffer higher gate-to-body AC voltage than M1 and M13. This phenomenon results in that M6 and M8 are unintentionally turned on in a portion of the cycle when the input power at TX node is large enough and limits the power-handling capability of the stacking T/R switch.
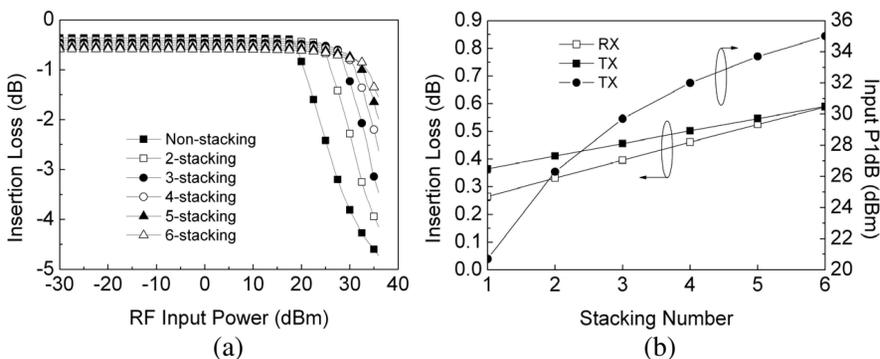
Figure 10. (a) Insertion loss vs. TX input power at 900-MHz. (b) The impact of stacking number on the TX/RX insertion loss and TX IP1 dB.
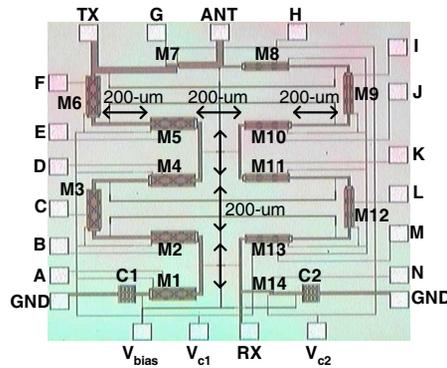
Figure 11. Die photograph of the stacking CMOS T/R switch with 200-μm spacing between transistors. The chip size is 1500-μm × 1500-μm.

5. MEASUREMENT RESULTS

The stacking CMOS T/R switch circuit is implemented with a standard 0.18-μm CMOS process which provides one poly layer and six metal layers. The die photograph of the stacking T/R switch circuit is shown in Fig. 11 which shows that a 200-μm spacing is kept between neighboring transistors of the stacking T/R switch circuit to get sufficient substrate isolation between each transistor. In order to be immunized against any package parasitics, the circuit has been wire bonded directly on the test printed-circuit board. On the board all the RF I/Os of the switch are connected to the SMA connectors through 50-Ohm microstrip line without using any impedance matching network. Besides, DC blocking capacitors are inserted between the DUT and SMA connectors. These setups ensure that the measurements will be as close as possible to the natural response of the T/R switch. The pads connecting the bodies of the transistors within the die are connected to the on-board R_Z through bonding wires to let the T/R switch get RF floated bodies. Fig. 12 shows the picture of the finished printed-circuit board.

As mentioned in the previous sections, all of the sources and drains of the NMOS transistors are biased at 1.5 V. In addition, the switches are turned on and off by two control voltages of 3 V and 0 V. The de-embedded performance of the RX path of the stacking CMOS T/R switch is shown in Fig. 13 which indicates that at 900-MHz the measured insertion loss is around 1 dB in the receive path. The isolation between TX and RX paths is better than 28 dB at 900-
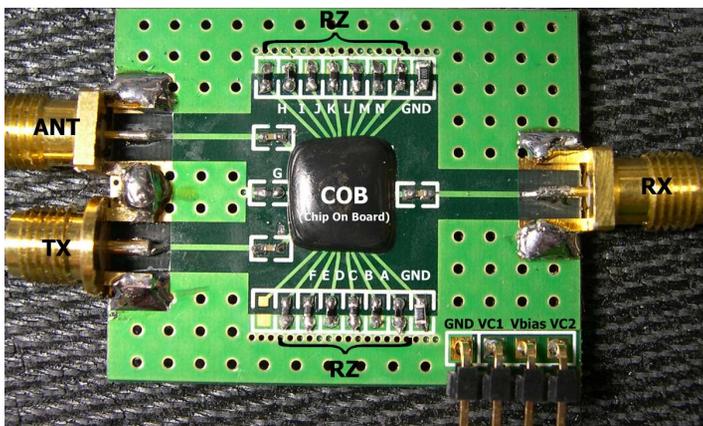
Figure 12. The evaluation PCB board was implemented to measure the chip performance of high power CMOS T/R switch.
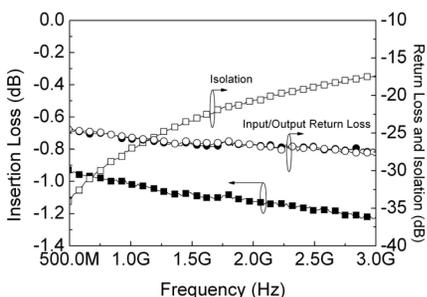
Figure 13. Measured scattering parameters for the RX path of the CMOS T/R switch over the frequencies from 0.5-GHz to 3-GHz.
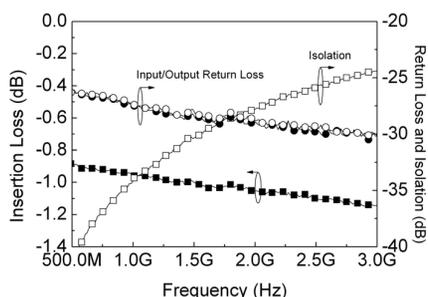
Figure 14. Measured scattering parameters for the TX path of the CMOS T/R switch over the frequencies from 0.5-GHz to 3-GHz.

MHz when the RX switch is turned off. Input and output return losses larger than 25 dB are simultaneously achieved as the RX switch is turn on. Fig. 14 shows the measured performance in the TX path. As is shown that at 900-MHz the insertion loss of 0.94 dB is obtained in the transmit path. The isolation between TX and RX paths is up to 35 dB at 900-MHz when TX switch is turned off. Input and output return losses are both larger than 27 dB when the TX path is in operation.

The linearity measurements of the chip on the PCB were carried out using an HP-E4421B signal generator accompanied by an external
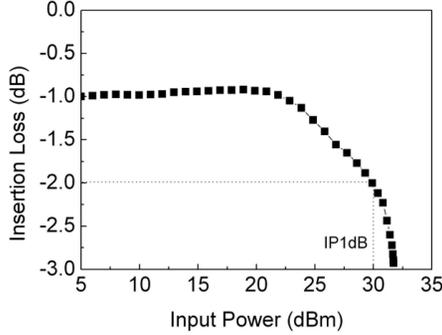
Figure 15. Measured insertion loss vs. TX input power for the stacking CMOS T/R switch operated at 900-MHz.

Table 1. Performance summary of bulk CMOS T/R switches.

Reference		[8]	[8]	[9]	[9]	[15]	[16]	[16]	[16]	[17]	This Work
Frequency (GHz)		0.928	0.928	0.928	0.928	0.9	0.9	0.9	0.9	2.4	0.9
Technology (µm)		0.5	0.5	0.35	0.35	0.35	0.26	0.26	0.34	0.25	0.18
Design Features		Low R_{sub}	Low R_{sub}	Low R_{sub}	Low R_{sub} +ITN	Enhanced Compact Waffle MOSFETs	3-stack SDR w/ cap	3-stack SDR w/o cap	2-stack	CMOS SOI	6-stack + Floated Body + High Substrate Isolation
Control Voltage		6V/2V	3.3V/0V	6V/2V	6V/2V	3V/0V	6V/2V	6V/2V	6V/2V	2.5V/0V	3V/0V
Insertion Loss (dB)	TX	-	-	-	-	-	0.5	0.5	0.5	-	0.94
	RX	0.73	0.97	0.46	0.97	1.7	1	1	1.2	0.7	1
Return Loss(dB)		-	-	> 15	> 15	> 15	> 20	> 19	> 19	-	> 25
Isolation (dB)	TX	-	-	-	-	> 27	37	37	35	54	35.2
	RX	41.8	40.1	39.5	35.4	> 27	29	29	31	-	28.4
IP1dB for TX (dBm)		17.2	11.5	17.7	24.3	7.8	31.3	30	26.5	12	30

power amplifier and a spectrum analyzer. The IP1 dB of the stacking CMOS T/R switch operating at 900-MHz is illustrated in Fig. 15. This switch can achieve input 1-dB gain compression point of 30-dBm in the transmit path which equally means that 200-µm spacing is sufficient to avoid strong substrate coupling between neighboring transistors of the T/R switch. The simulated input P1 dB is 35-dBm which is 5 dB larger than the measured one due to the lack of large-signal models of the transistors in the design phase and the mechanism destructing the linearity of the CMOS T/R switch discussed in Section 4.

To compare the performance of the switch proposed in this paper with previous arts, Table 1 summaries the measured insertion loss, return loss, isolation, and IP1 dB of the selected T/R switches at 900-MHz. The work presented in this paper demonstrates competitive

performance among the previously published results. The most prominent thing is that the proposed T/R switch can achieve an IP1B of 30-dBm by using 3 V (ON) and 0 V (OFF) control voltages. Smaller chip size can be achieved by using CMOS SOI technology [17].

6. CONCLUSION

The stacking T/R switch implemented with a standard 0.18-μm CMOS process has been designed, fabricated, and measured for 900-MHz applications. This work shows that combining stacked transistors with RF floated bodies and high substrate isolation is effective to largely enhance the power-handling capability of the bulk CMOS T/R switch. This stacking T/R switch shows an excellent performance of IP1 dB of 30-dBm in the transmit path and the insertion loss of 1 dB in the receive path at 900-MHz. Because of the application of a standard CMOS process to implement the CMOS T/R switch, it is expected that the proposed T/R switch can be easily integrated with CMOS RF transceivers for 900-MHz applications.

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