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CONTROLLING THE FREQUENCY OF SIMULTANEOUS SWITCHING NOISE SUPPRESSION BY USING EMBEDDED DIELECTRIC RESONATORS IN HIGH-IMPEDANCE SURFACE STRUCTURE

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Abstract—This work presents a novel design for high-impedance surface (HIS) embedded dielectric resonator (DR) structures to efficiently control bandwidth of suppression simultaneous switching noise (SSN) in high speed digital printed circuit boards (PCBs). The proposed structure is designed by periodically embedding high dielectric constant materials into the substrate between a continuous power plane and a middle patch. A conventional HIS structure has only one resonance frequency to produce stopband while the proposed structure has two resonances to widen the suppression bandwidth. The −30 dB stopband of the proposed structure is about two times wider than that of a conventional HIS structure. The excellent SSN suppression behavior was verified by measurements and simulations.

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1. INTRODUCTION

With increasing requirements on modern digital circuits with high clock frequencies and fast edge rates, simultaneous switching noise (SSN), ground bounce noise (GBN), or Delta-I noise appear as abrupt undesired fluctuations in the voltage on the power and ground planes. The noise, if undetected, can generate several low- and high-frequency anomalies; the most important of which is the biasing of the power planes, which leads to logic errors in digital circuits. The SSN also results in significant radiated emissions or electromagnetic interference (EMI). Several investigations have contributed to the elimination of the SSN. A typical way to suppress the SSN and EMI issues is adding decoupling capacitors [1] between power and ground planes, utilizing the isolation slots on the power or ground plane and selecting the location of the via ports to eliminate the excitation of the GBN.

Recently, a new concept for mitigating SSN using an electromagnetic bandgap structure (EBG) [2, 3] or a high-impedance surfaces (HIS) [4, 5] in place of the ground plane was proposed. The impact of the geometry on the performance of power planes with simple and inductance-enhanced HIS is investigated in [6]. But this approach is not easily manufactured as it requires a spiral structure in the PCB to obtain a larger inductance. Also described is a class of embedded electromagnetic band gap (EEBG) structures in which larger capacitances are used to create miniaturized unit cell designs [7], which obtaine a broadband suppression behavior by high-dielectric materials with thin film structures. In addition, cascaded EBG structures with different cell sizes have been used to increase the bandwidth of the EBG bandgap [8–10]. However, these EBG structures either occupy a large area of the substrate, or need a special thin film processing for the high-dielectric materials. A novel power delivery network design with an electromagnetic crystal power substrate (ECPS) to suppress the SSN has been proposed in [11]. This concept is to embed the high dielectric constant material into the substrate layer between power and ground planes. Hence, this structure needs higher dielectric constant material to obtain the elimination behavior below 10 GHz.

The HIS structures has a resonance frequency in the suppression bandwidth [12, 13]. Therefore, application of high dielectric constant of substrate is widely used to widen suppression bandwidth. In this work, we focus on controlling the SSN suppression bandwidth in high speed digital PCBs/packages. We present a new HIS structure with dielectric resonator (DR) to extend the noise suppression bandwidth, called a DR-HIS structure, fabricated on FR4 substrate. The DR is embedded into the original substrate layer between the solid power plane and

middle patch. There are two resonance frequencies in the stop-band. One is caused by the HIS structure, and the other is provided by the DR. The presented concept is based on change of the DR radius to dominate the stop-band width.

2. STRUCTURE DESIGN

Figure 1(a) shows a high-impedance surface structure with a dielectric resonator between the power plane and middle patch. The top layer is simply fabricated by drilling holes with 5-mm radius on the substrate and embedding the DR into the holes. The bottom layer consists of a regular patch with via positioned in its center. The dimensions of the two-layer PCB are 49 mm × 49 mm. The top view of the proposed structure is shown in Figure 1(b). The corresponding geometrical parameter set of a unit cell is denoted as $(d, a, r_d, r, h_1, h_2, \varepsilon_{r1}, \varepsilon_{r2}, \varepsilon_{r3})$, where d is the period of the unit cell; a is the patch length; r_d is the radius of the dielectric resonator; r is the radius of via; h_1 and h_2 are the distances between middle plane and power/ground planes, respectively; ε_{r1} and ε_{r2} are the dielectric constant of substrate; ε_{r3} is the dielectric constant of the DR. The dielectric resonator was prepared by using a solid-state reaction with ZnO, TiO_2, and MgO under the typical ceramic fabrication process. The dielectric constant of the DR (ε_{r3}) is approximately 30. Two measurement ports, named port 1 and port 2, are located at (8.5 mm, 16.5 mm) and (40.5 mm, 32.5 mm), respectively. The SMA probes through whole structure are used to measure the scattering parameters of the fabricated PCB.

In fact, the self-resonance frequency of the HIS is given as

$$f_{res} = \frac{1}{2\pi\sqrt{L\left(C_1 + C_2\right)}} \tag{1}$$

where L and C_2 represents the inductance of via and parallel-plane capacitance between ground and middle plane, respectively. C_1 is a capacitor which is caused by two metal planes with a dielectric resonator. As the HIS structure works in the resonating frequency, this structure can be seen as a series LC circuit which provides a short path leading the noise to the ground. Therefore, the suppression bandwidth of the HIS structure is approximated as

$$BW \propto \sqrt{\frac{C_1}{L}} \tag{2}$$

Equation (2) means that a wider suppression bandwidth will be obtained by increasing the capacitance of the proposed structure.

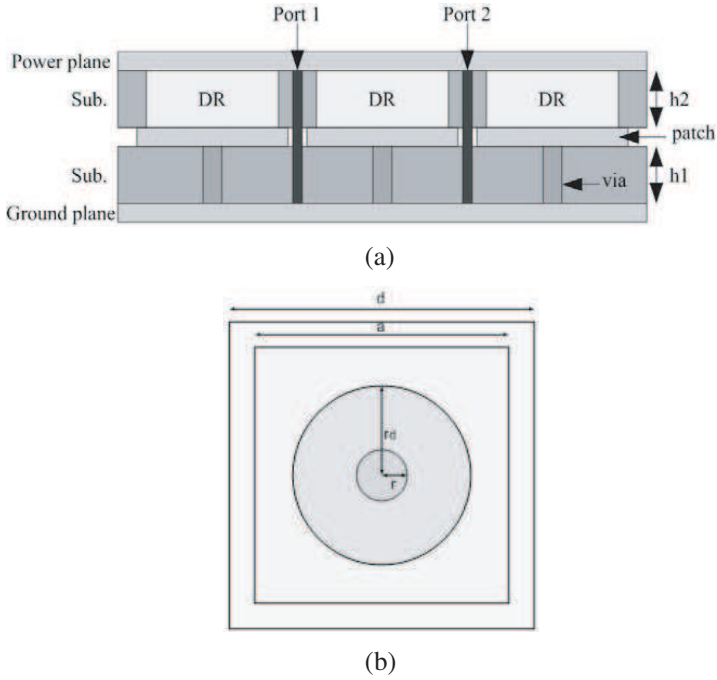

Figure 1. Schematic diagram of the proposed test boards. (a) 3D view. (b) Unit cell.

In the stop-band, the presented structure provides two resonance frequencies which are caused by the DR and HIS structures, respectively. The high-frequency resonance is based on the corresponding parameters of the HIS structure, and the low-frequency is determined by the DR. Modification of the DR radius can be used to control the suppression bandwidth.

3. CAPACITANCE-ENHANCED HIGH-IMPEDANCE SURFACE

3.1. Effect of DR Permittivity (ε_{r3})

The corresponding geometrical parameters of the unit cell for the design are (16 mm, 15 mm, 5 mm, 0.25 mm, 0.8 mm, 1.6 mm, 4.4, 4.4, 30), respectively. The thickness of the metal plane is 0.035 mm. The first parameter to be studied is the dielectric constant of the DR (ε_{r3}). Figure 2 shows the suppression behavior of the proposed structure with different dielectric constants for the DR, where the dielectric constant

is varied from 4.4 to 70, or without the DR. All other geometrical parameters are fixed. It is clearly seen that the structure with different dielectric constants leads to a new design with wider noise suppression bandwidth than the conventional HIS structure. The bandwidth of the proposed structure was enhanced as ε_{r3} increased due to the raised effective dielectric constant. The effective dielectric constant here is defined as [11]

$$\varepsilon_{eff} = A_r \varepsilon_{r3} + (1 - A_r)\, \varepsilon_2 \tag{3}$$

where A_r is defined as the total area of the embedded DR to the area of the substrate. With the dielectric constant of DR increasing, the resonant frequency will be shifted to lower frequencies, and the suppression bandwidth could be widened, simultaneously. There are two resonance frequencies at 1.6 and 1.95 GHz when dielectric constant is increased to 50. The reason could be that these frequencies were produced by two effective capacitances between the power plane and middle plane along with the inductance of via. One was caused by the effective dielectric constant, and the other was caused by the DR. The concept of the proposed structure is that the top layer has two material behaviors to control the suppression bandwidth. However, this concept will be broken when the dielectric constant of the DR is increased to 70, because there is only one material behavior in the top layer of proposed structure.

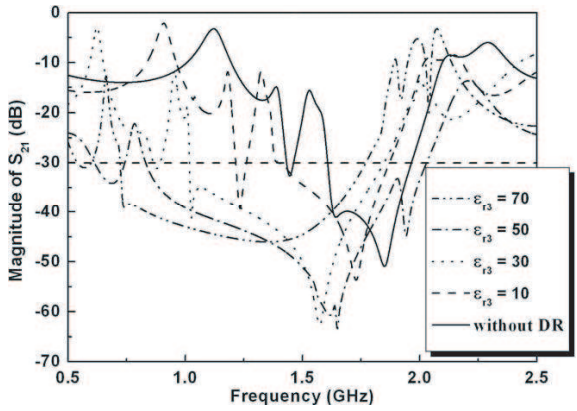

Figure 2. Magnitude of S_{21} versus frequency for the proposed structure with the different dielectric constant of the DR or without the DR.

3.2. Effect of DR Radius (r_d)

The second parameter to be studied is the effect of the DR radius. Figure 3 shows the suppression behavior of the proposed structure with different DR radii (r_d) when the radius is varied from 1 to 7. All other geometrical parameters are fixed. In comparison with the conventional HIS structure, it is observed that the suppression bandwidth gradually widens as the radius is increased, as shown in Figure 3. There are two resonant frequencies to expand the bandwidth. The high- and

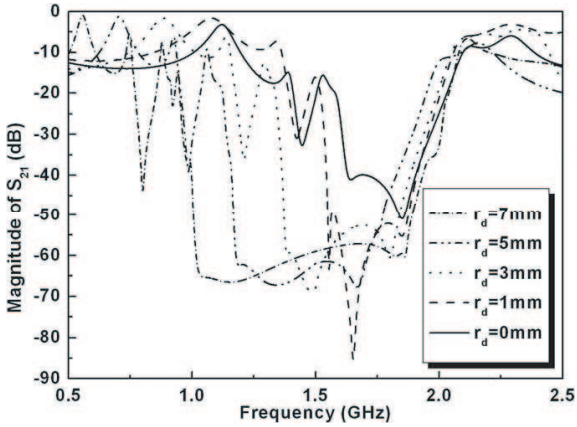

Figure 3. Magnitude of S_{21} versus frequency for the proposed structure with different DR radius.

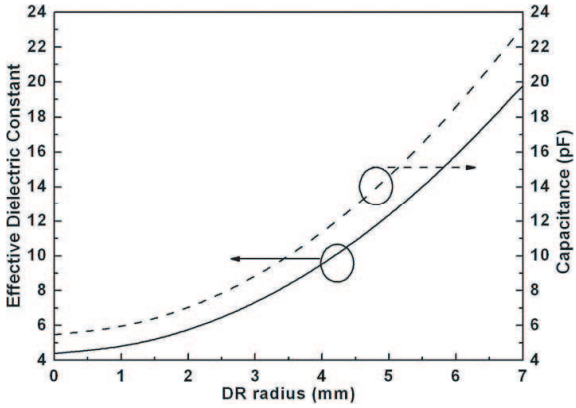

Figure 4. Comparison of the DR radius versus effective dielectric constant and capacitance of the DR.

low-frequency resonant modes were produced by the capacitance of the parallel-plate and DR with the inductance of via, respectively. It is seen that the higher mode would be slightly shifted to a lower frequency as the radius is increased due to the raised effective dielectric constant, as shown in Figure 4. On the other hand, the lower mode was significantly shifted, because the capacitance produced by the DR would be enhanced as the DR radius increased, as shown in Figure 4. Notice that the radius of the DR does not outstrip the 7 mm. Because the Ar ratio will be equal to 1, it means that the top layer exhibits one material behavior, and eventually the concept only has a resonance mode.

4. EXPERIMENTAL RESULTS AND DISCUSSION

Limited by fabrication, the height of the DR was selected as 1.6 mm in this work. The measurements were performed on an Agilent 8364A vector network analyzer (VNA). According to Figure 3, the optimum suppression performance of the presented structure occurred in the A_r of 0.66. Therefore, the patch size and radius of the dielectric resonator for this work are selected as 15 mm and 5 mm, respectively. The test board and conventional HIS structure with the same parameters are also fabricated and measured for comparison. The reference board with power and ground planes keeping continuity is used to compare. The comparison of suppression behaviors between the proposed structure, conventional HIS, and reference board is shown in Figure 5. The bandwidths of the proposed structure and

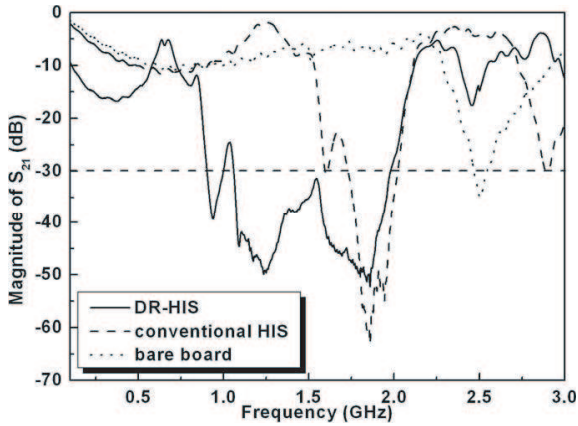

Figure 5. Comparisons of suppression SSN behavior between reference board, conventional HIS, and DR-HIS.

conventional HIS are approximately 0.92 GHz (from 1.06 to 1.98 GHz) and 0.3 GHz (from 1.73 to 2.03 GHz), respectively. The bandwidth is defined by an insertion loss less than −30 dB. It is clearly seen that the relative bandwidth is increased by about a factor of two. The stop frequency of the stopband is shifted to a lower frequency due to the effective dielectric constant, which is slightly increased compared to the conventional structure. In the situation of fixing the A_r ratio, the broadband SSN suppression can be efficiently obtained by reducing the dielectric resonator dimension and shrinking the HIS size, which also modify the presented structure for other applications operating at different frequency bands.

Figure 6 shows the measured and simulated magnitudes of S_{21} for the proposed structure. The performance of the reference board with both power and ground plane being continuous is also included in this figure for comparison. Good agreement between the measurement and simulation is obtained, as shown in Figure 6. The difference between measurement and simulation results could be caused by the dielectric resonator with rough surface, which leads to the decreased effective capacitance, and then the dielectric loss of the dielectric resonator was not considered in simulated results. The simulation results did not take these two problems into account to make a significant discrepancy, especially between 1 GHz and 2 GHz. There are significant resonance peaks below 1 GHz for the proposed structure. The reason might be caused by fundamental cavity mode of the parallel-plate waveguide with the effective dielectric constant of the substrate. Application of decoupling capacitors among the power and ground planes can suppress these resonances.

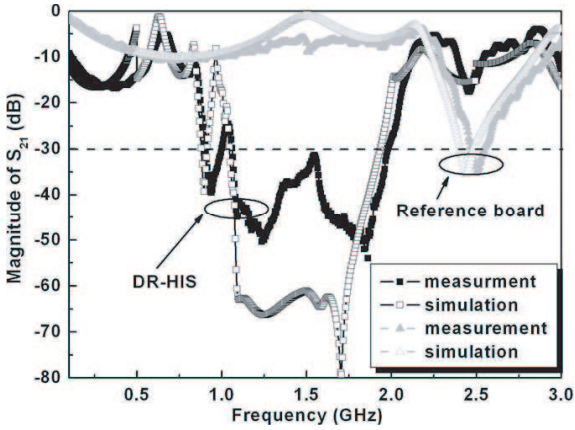

Figure 6. The measurement and simulation results of DR-HIS and reference board.

5. CONCLUSION

A novel design for HIS embedded dielectric resonator structure is proposed to efficiently mitigate SSN in high speed digital PCBs. The −30 dB suppression bandwidth of the proposed DR-HIS structure is about two times wider than for a conventional HIS structure. Broadband DR-HIS structures can be easily obtained by using the DR with a lesser thickness. A conventional HIS structure has a resonant frequency to produce a stopband. The proposed structure has two resonances to widen the suppression bandwidth. The stopband width was controlled by the dielectric constant and radius of DR. If these two modes were obviously separated, the suppression behavior would be shrunk.

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