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A 16–31 GHz MINIATURE QUADRUPLE SUBHARMONIC MONOLITHIC MIXER WITH LUMPED DIPLEXER

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Abstract—A novel 16–31 GHz quadruple subharmonic monolithic passive mixer with a chip dimension of $0.82 \times 0.7\,\text{mm}^2$ is designed and fabricated using the 0.15 μm GaAs pHEMT process. The novel configuration of the quadruple subharmonic mixer consists of a lumped frequency diplexer and a low-pass filter utilizing a pair of anti-parallel Schottky barrier diode to achieve quadruple subharmonic mixing mechanism. The lumped frequency diplexer formed with a low-pass network and a high-pass network is used to reduce the chip dimension while operating at low frequency band and to improve the isolation between the RF and LO ports with a broadband operation. The low-pass filter supports an IF frequency range from DC to 2.5 GHz. From the measured results, the mixer exhibits a 12.5–16.5 dB conversion loss, a LO-to-RF isolation better than 15 dB, a 50–59 dB high 4LO-to-RF isolation over 16–31 GHz RF bandwidth, and an input 1 dB compression power of 2 dBm.

1. INTRODUCTION

The emerging millimeter-wave communication systems demand broadband operation, compact size, low manufacturing cost, and low-power consumption for high performance transceiver solutions. One important component of these systems is the mixer to convert signals from one frequency to another. The mixing mechanism of most mixers employs the fundamental local oscillation (LO) signal to

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achieve frequency conversion. However, as the operating frequency is increased, the resonator quality used for the oscillator will be degraded resulting in the increase of phase noise and the degradation of the output power. Moreover, the fundamental mixers have LO self-mixing problems for direct-conversion transceivers caused by LO leakage to the radio frequency (RF) port, generating a DC offset at the intermediate frequency (IF) port. Accordingly, the frequency multiplier and subharmonic mixer (SHM) are the two most common approaches that allow the use of an LO signal at a relatively low frequency. This makes the local oscillator sources more reliable and less expensive.

Previously, several quadruple SHMs using the anti-parallel diode pair (APDP) topology on III-V process have been proposed in [1–3]. The APDP topology can suppress any even-order spurious mixing components because of its anti-symmetric current-voltage features. However, the operational bandwidth is limited by open/short stubs. Moreover, the required LO frequency is only one-quarter of the RF frequency, which causes the quarter-wavelength open/short stubs at LO frequency to occupy a large chip area. A miniature subharmonic mixer with a directional coupler can be found in [4]. The directional coupler was employed to excite RF and LO signals into APDP diodes. However, it is not suitable for quadruple SHM design due to the operating bandwidth of directional coupler. This makes the LO and RF signals combination hardly. Recently, a 10–40 GHz broadband CMOS subharmonic mixer based on two-stage Wilkinson power combiner has been proposed [5]. Although it shows broadband feature; however, the degeneration of LO-to-RF isolation is consequent on the limit of two-stage power combiner. Recently, a CMOS Ku-band quadruple SHM based on a modified Gilbert-cell topology has been proposed [7]. It shows high conversion gain within a narrow bandwidth; however, additional DC power consumption is necessary. Otherwise, the quarter-wavelength microstrip structures [1–6] are difficult to implement at quite low frequency for compact requirement. Accordingly, lumped or semi-lumped element devices requiring only a smaller area are very attractive for quadruple SHM.

In this work, a 16–31 GHz quadruple SHM with a compact chip size of $0.82 \times 0.7\,\mathrm{mm}^2$ fabricated in a $0.15\,\mu\mathrm{m}$ GaAs pHEMT process is described. The proposed quadruple SHM comprises a lumped frequency diplexer and a low-pass filter to accomplish wider bandwidth operation and maintain superior port-to-port isolation for down-converter applications.

2. CIRCUIT DESIGN AND IMPLEMENTATION

Owing to the drawbacks of narrow operational bandwidth and larger chip size in the conventional quadruple SHMs using APDP technology, a broadband quadruple SHM with a compact configuration and with good port-to-port isolation for down-conversion applications is proposed. The architecture of the proposed quadruple SHM, which consists of a frequency diplexer and a low-pass filter, is demonstrated in Figure 1. The mixing is performed between the RF signal and the fourth harmonic of the LO signal. This indicates that quadruple SHM requires one quarter of the LO frequency of a fundamental mixer. Consequently, it is difficult to combine the high-frequency RF signal with the relatively low-frequency LO signal by a hybrid. Accordingly, a lumped frequency diplexer is used to overcome the above problem and achieve high performance. Frequency diplexers realized by distributed circuit structures to attain low insertion loss and high isolation have been reported [8, 9]. However, the distributed circuit structures are unsuitable for MMIC design, especially if the operating frequency is relatively low. For this reason, the configuration of the proposed frequency diplexer, as shown in Figure 1, is composed of both fourth-order low-pass filter and high-pass filter served by lumped elements. The lumped inductors and capacitors can be supported readily in III-V pHEMT process. This will greatly benefit the reduction of design complexity and chip dimension. Furthermore, a thorough discussion of lumped diplexer synthesis can be seen in [10]. In order to ensure a maximally flat within the pass band, the Butterworth response is used. Moreover, the utilization of fourth-order frequency diplexer can also increase the isolation between RF and LO ports owing to the steeper slope of stop band response.

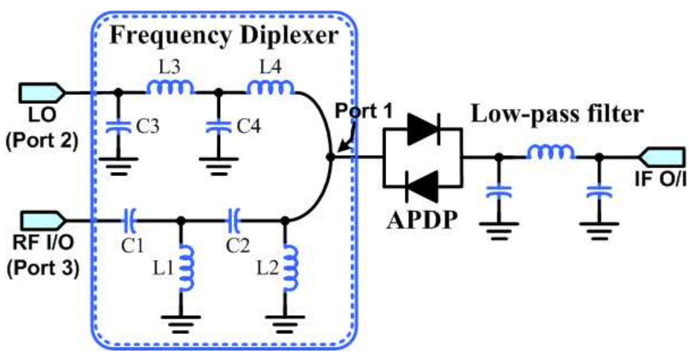

Figure 1. The proposed compact configuration of the quadruple SHM.

In this case, the purpose of the lumped diplexer is to excite a RF and LO signal into APDP simultaneously and to improve the isolation between the RF and LO ports with a broadband operation. It is a three-port device used to pass LO signal operating at 3–10 GHz by low-pass filter and RF signal operating at 16–31 GHz by high-pass filter, respectively. To improve the isolation between the RF and LO ports and attain good performance of the frequency diplexer, the lumped elements can be optimized by employing the full-wave electromagnetic (EM) simulator. The capacitance per unit area is $0.4\,\mathrm{fF}/\mu\mathrm{m}^2$, and the physical dimensions of C_1, C_2, C_3, and C_4, as shown in Figure 2, are calculated as $29\,\mu\mathrm{m} \times 29\,\mu\mathrm{m}$, $16\,\mu\mathrm{m} \times 16\,\mu\mathrm{m}$, $22\,\mu\mathrm{m} \times 22\,\mu\mathrm{m}$, and $30\,\mu\mathrm{m} \times 30\,\mu\mathrm{m}$, respectively. The inductor values are also obtained, where $L_1 = 0.37\,\mathrm{nH}$, $L_2 = 4.14\,\mathrm{nH}$, $L_3 = 1\,\mathrm{nH}$, and $L_4 = 1\,\mathrm{nH}$. Finally, the simulated insertion losses of the two pass bands are both less than 0.4 dB and the simulated isolation between ports 2 and 3 is also better than 18 dB within the operation bandwidth. This is more convenient in quadruple SHM design and is also more effective in extending the operational bandwidth with well impedance matching and reducing the chip area. In addition, the shorted inductor, L_2, provides a current-return path and is used to match the diode's junction resistance.

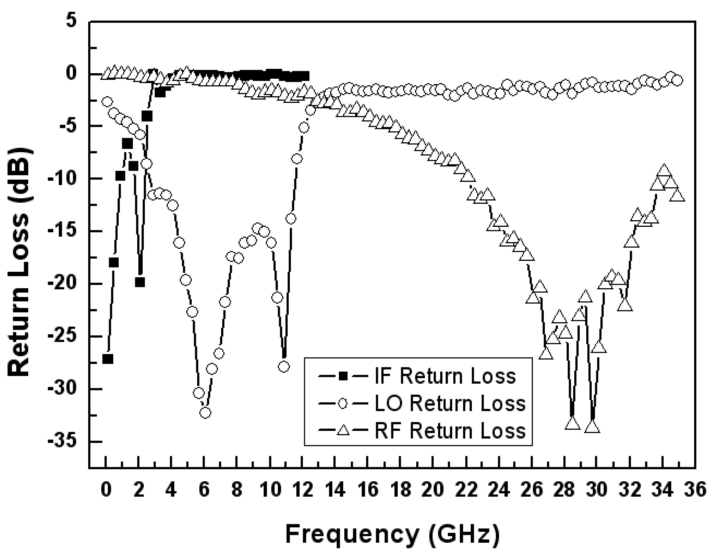

Figure 2. The measured RF, LO, and IF return loss of quadruple SHM as a function of frequency.

Figure 2 illustrates the measured RF, LO, and IF return loss as a function of frequency. The RF and IF return losses were measured with the LO fixed at 7 GHz and the LO input power of 10 dBm. The RF return loss varies from 4.1 to 33.6 dB over the 16 to 31 GHz frequency range. The IF return loss is also less than 6.6 dB within the 3-dB IF bandwidth from DC to 2 GHz. Moreover, the LO return loss is between 8.6 dB and 32.3 dB from 2.5 to 11 GHz. Therefore, the designed quadruple SHM is well matched to the RF, LO, and IF ports and not eminently affected by connecting the APDP. In this design, the diode with two fingers and 10 μm gate width is optimized to achieve good impedance matching and ensure minimum conversion loss. The substrate was thinned down to 100 μm with a relative permittivity of 12.9. A photograph of the fabricated quadruple SHM is shown in Figure 3. The chip dimension is reduced to $0.82 \times 0.7\,\mathrm{mm}^2$. Moreover, the core chip area, excluding the contact GSG testing pads, is only $0.62 \times 0.57\,\mathrm{mm}^2$.

3. EXPERIMENTAL RESULTS

The fabricated MMIC quadruple SHMs were attached to the carrier plates for testing. The measurement signals were provided by the coplanar GSG and GSGSG on a wafer probe measurement system based on the Agilent E4446A spectrum analyzer, which was calibrated with the E44198 power meter. The losses of the probes and cables were calibrated by the PNA E8364A network analyzer. Figure 4 demonstrates the measured and simulated conversion loss of the

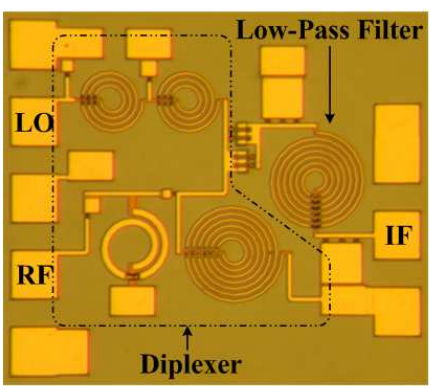

Figure 3. A photograph of the fabricated quadruple SHM. The chip dimension including the contact pads is $0.82 \times 0.7\,\mathrm{mm}^2$.

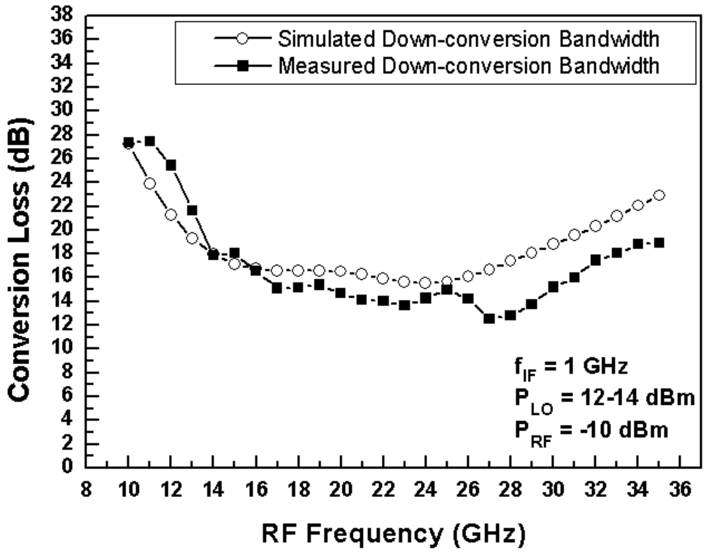

Figure 4. Conversion loss of the quadruple SHM at a fixed LO power of 12–14 dBm and 1 GHz IF frequency.

quadruple SHM as a function of RF frequency for down-converter modes. The measurements were performed with an LO power level of 12–14 dBm and 1 GHz IF frequency. The obtained conversion loss is 12.5 to 16.5 dB within an RF bandwidth from 16 to 31 GHz. Due to high frequency parasitics, the operating bandwidth was slightly shifted from the design goal to higher frequency band. The low conversion loss of 12.5 to 16 dB can be achieved at the high end of the band ranging from 26 to 31 GHz; however, the higher LO drive power of 14 dBm is necessary.

Figure 5 shows the measured and simulated conversion losses versus LO power level with an RF frequency of 18 GHz and input power of −10 dBm for the down-converter mode. A significant mixing effect of an LO drive level of 7 dBm can be seen. The lowest conversion loss is 15 dB at a 12 dBm LO power level. Figure 6 demonstrates intermodulation characteristics of the quadruple SHM. A two tone RF signal was applied at 18 GHz and 18.01 GHz to measure IP2 and IP3. The measured input 1 dB compression point is 2 dBm. In addition, The IIP2 and IIP3 were determined to be approximately 44 dBm and 9 dBm, respectively. The measured and simulated LO-to-RF, LO-to-IF, RF-to-IF, and 4LO-to-RF isolations of quadruple SHM for the down-converter mode are shown in Figure 7. Under the measured

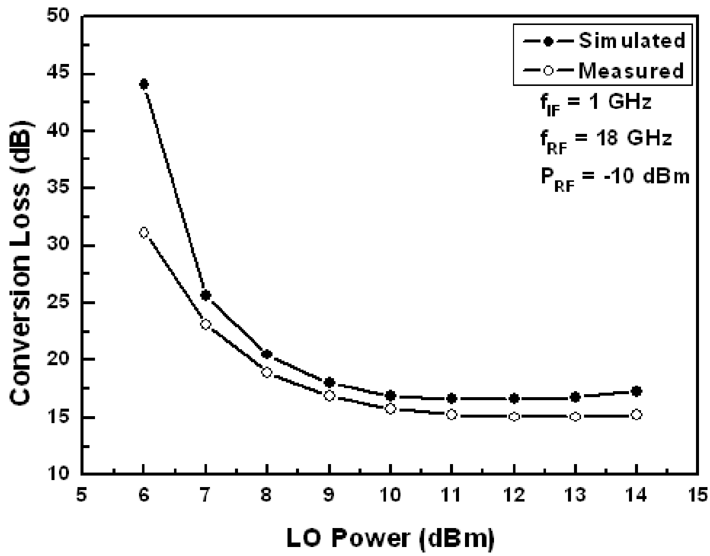

Figure 5. Conversion loss versus LO power at −10 dBm RF level and 1 GHz IF.

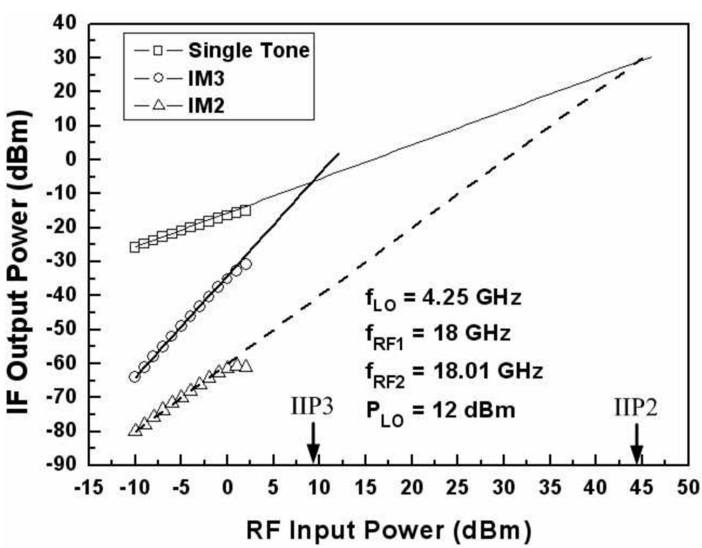

Figure 6. Intermodulation characteristics of the quadruple SHM.

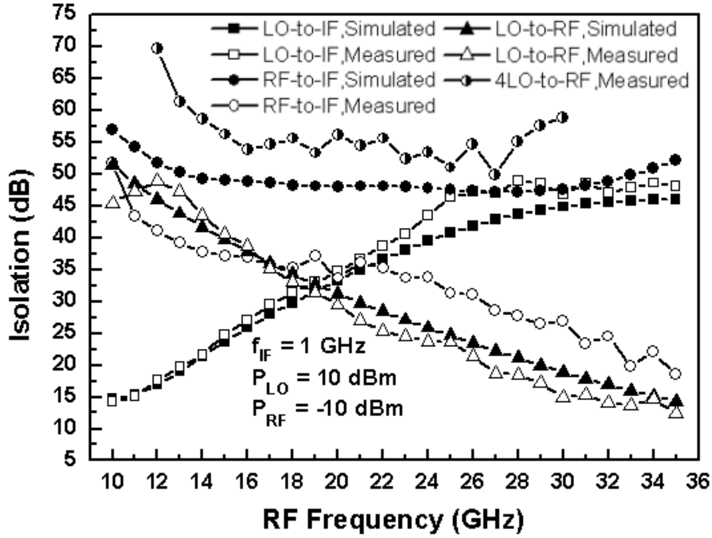

Figure 7. Isolation of the quadruple SHM at the 10 dBm LO level and 1 GHz IF.

Table 1. Comparison of reported subharmonic mixers.

Ref.	[1]	[2]	[5]	[4]	This Work
Technology	GaAs		0.18 μm CMOS	0.15 μm GaAs	
RF freq. (GHz)	58.5–60.5	94	10–40	23–37	16–31
LO harm.	4th	4th	2nd	2nd	4th
CL* (dB)	11.3 ∼ 13.3	11.4	15.6 ∼ 17.6	9.4 ∼ 12	12.5 ∼ 16.5
P_1 dB (dBm)	-	−9	8	6	2
LO Power (dBm)	7	10	8	13	12–14
Die Size (mm^2)	7	1.26	0.74	0.72	0.35$^+$

CL*: conversion loss; + core area excluded GSG pad

conditions shown in Figure 7, the LO-to-RF isolation is only between 14 and 20 dB at the high end of the band; however, it is greater than 30 dB at the low end of the band ranging from 14 to 20 GHz. The LO-to-RF isolation is limited by the proposed frequency diplexer. The

LO-to-IF isolation is higher than 21.7 dB from 14 to 35 GHz, and it is better than 35 dB from 20 to 35 GHz. The RF-to-IF isolation is higher than 24 dB over all the operational frequencies. This inherent LO/RF-to-IF isolation is due to the low-pass filter. Owing to the APDP technology, the 4LO-to-RF isolation in the required band is 50 to 59 dB. In addition, the measured input 1 dB compression point is 2 dBm with the RF fixed at 18 GHz. Comparisons of the proposed structure with other published works are summarized in Table 1. This work presents some significant advantages, such as an operating bandwidth of 16 GHz and compact chip size as compared to previously reported works.

4. CONCLUSION

A novel and compact-sized 16–31 GHz quadruple SHM is designed using the 0.15 μm GaAs pHEMT process A lumped frequency diplexer is utilized to excite the RF and LO signals into APDP for broadband application and eliminates the use of short/open circuited stubs in the conventional quadruple SHM. Based on the measured results, the proposed architecture has some significant advantages, such as wider band performance, superior isolations, and higher dynamic range, which are relatively suitable for millimeter-wave applications.

ACKNOWLEDGMENT

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