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DUAL BAND HIGH EFFICIENCY CLASS CE POWER AMPLIFIER BASED ON CRLH DIPLEXER

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Abstract—In this paper, the most adequate architecture to implement dual frequency amplifiers is shown. Composite Right/Left Hand (CRLH) and Extended Composite Right/Left Hand (ECRLH) transmission lines are studied and evaluated to find the most suitable structure for dual band power amplifiers. As an example, the performance of a class CE amplifier, working in TETRA and GSM frequency bands, is compared with simulations and measurement, showing good agreement.

1. INTRODUCTION

The increasing demand for wireless systems requires the use of higher frequency spectrum. Such high frequencies entail two major drawbacks: First, line transmission losses increase significantly. And second, solid state devices present power limitations at radio frequency (RF). Besides, when high RF power is demanded, there are some problems related with conventional system design and implementation, which can be overcome combining several RF devices to achieve the desired level. Another problem arises from the need of multifunction transponders to cope with several services, usually allocated at different frequencies, in the only terminal, being a well known example multiband or even GPS mobile phones. As a result of all these drawbacks, the development and use of multi-frequency high-performance power amplifiers is required. In this paper, TETRA

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(380 MHz) and GSM (960 MHz) have been chosen to exemplify the viability of the proposed structures and designs.

Different solutions have been suggested to solve these problems, the use of switches [1, 2] being the most widely implemented, although other topologies based on MMICs [3] have proven their validity.

The advent of CRLH lines in recent years [4, 5] has opened new possibilities in the design of dual band amplifiers, since lines or components can work at two frequencies using them [6, 7]. This fact has already been noticed by several authors, as can be checked in their published papers about double-band amplifiers based on CRLH lines [8, 9]. In these designs, suitable loads for harmonics have not been taken into account, and therefore they lack enough harmonic loading to achieve higher performances, as it has been demonstrated by Cripps [10]. Nevertheless, this great flaw has been analyzed for class E amplifiers by Thian [11], who proposes a dual network to match impedances at fundamental and harmonics, so as to synthesize the adequate loads required for high performance.

The use of class CE, defined by Sokal [12–14], offers several advantages over other high-performance topologies, such as third-harmonic low dependance; the opposite case can be found in class F. Also, class CE harmonic load conditions are suited to encapsulated-transistor typical parasitics. And finally, considering that some generalizations about CRLH lines, which have recently appeared, allow adequate phase conditions up to three [15] or four [16] different frequencies, it seems appealing that the study of them is applied to dual-band high-performance amplifiers.

In the first part of this paper, a brief analysis of the possible solutions to dual-band class CE amplifiers at 380 MHz (TETRA) and 960 MHz (GSM) will be carried out, analyzing the structure without harmonic loading as the proposals of Dupuy [9], using similar solutions as the ones of Thian [11], and via E-CRLH lines [16]. In the second part, a feasible solution will be proposed to obtain high performance in dual-band class CE amplifiers with meta-materials and a diplexer structure, at the end and out, based on D-CRLH lines [17, 18]. The structure has been simulated and manufactured with excellent results. Finally, some conclusions will be shown.

2. DESIGN OF DUAL-BAND HIGH-EFFICIENCY AMPLIFIER TOPOLOGIES WITH CRLH LINES

Due to the physical characteristics of bipolar transistors, class C amplifiers are not suitable for microwave frequencies. Similar amplifying features can be achieved with class CE amplifiers. The

maximum efficiency of this mode is reached when the load impedance (at fundamental frequency) approximately matches the Equation (1), and the impedance at 2nd harmonic is open circuit.

$$\begin{aligned} R_p &= 0.625 \cdot \frac{(V_{cc} - V_{sat})^2}{2 \cdot P_{out}} \\ X_p &= -\frac{1}{\omega \cdot C_{ob}} \end{aligned} \tag{1}$$

Input impedance will be the key factor allowing the highest power transfer with the proper load for this working mode. The shapes of the currents and voltages have been carefully described in [13]. If the quotient between the previous magnitudes is calculated, then the impedance load at the different harmonic frequencies will be obtained. In this case, open circuits at the harmonic frequency of the fundamental one will be found.

$$\begin{aligned} Z(f_o) &= \frac{1}{\frac{1}{R_p} + j\frac{1}{X_p}} \\ Z(n \cdot f_o) &= \infty(o \cdot c) \end{aligned} \tag{2}$$

where R_p and X_p are the equivalent parallel load impedance. In any case, it should be pointed out that this is an approach which needs to be adjusted by means of a load-pull analysis (to include the most significant parasitics of transistor output network and the overdrive effect). The input impedance will be the one that allows the maximum power transfer under the corresponding load conditions.

From a practical point of view, it would suffice to have second harmonic loading close to open circuit. So, matching networks at two frequencies, for input and output, must fulfill the conditions shown by Figure 1.

CRLH lines can be used to synthesize these networks. The first three network architectures are shown in Figure 2.

For the very first architecture (Figure 2(a)), we do not have control over impedance at second harmonic for both frequencies. Therefore, performance and obtained powers will show a wide range of values. This will be demonstrated later on a practical basis. Regarding the second and third architectures (Figures 2(b) and 2(c)), we do have control over impedance at second harmonic for both frequencies. Therefore, they seem to be optimum structures for this kind of amplifiers. Nevertheless, as we will show later, the only suitable architecture for dual band amplifiers with CRLH lines is the one in Figure 2(d).

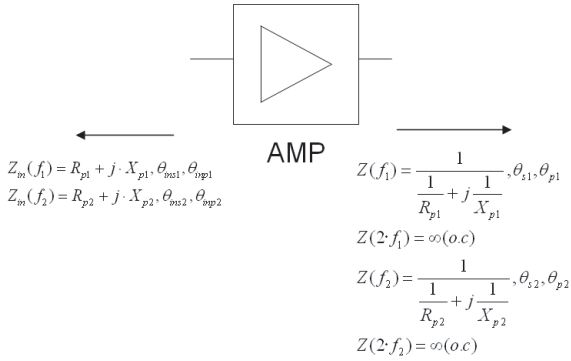

Figure 1. Load conditions in a class CE amplifier.

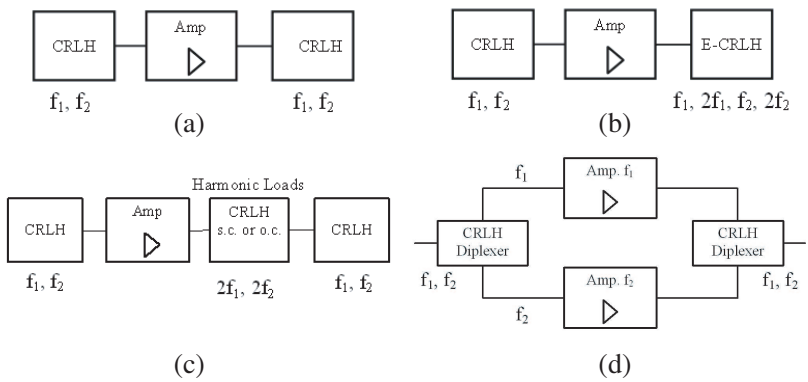

Figure 2. Possible architectures for a dual-band class-CE amplifier (a) with CRLH, (b) with ECRLH, (c) with CRLH + harmonic loading, and (d) with diplexers.

3. VIABILITY STUDY OF DUAL-BAND CLASS-CE HIGH-EFFICIENCY AMPLIFIERS WITH CRLH LINES

Prior to proceeding with the actual implementation of an amplifier, we will carry out a detailed analysis of Figure 2 architecture viability. So, an active device is chosen: BFG551. This selection is supported by several facts: First, there are non-linear models of the device. And second, it is a sound choice for medium-power low-tension-supply wireless systems. Resistive padding, at low frequencies and at the input, is used to stabilize the circuit, as it is shown in Figure 3.

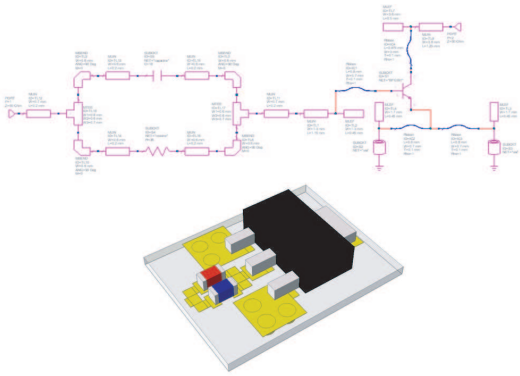

Figure 3. BFG591 transistor stabilisation circuit.

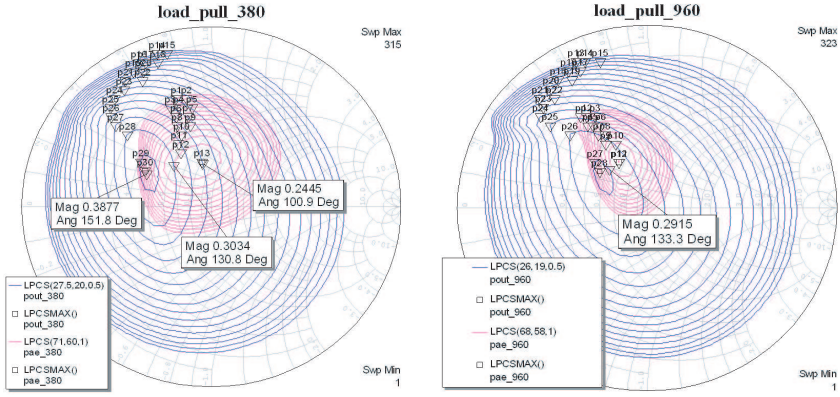

Figure 4. Load-pull contours for BFG591 at 380 MHz (left) and 960 MHz (right).

A load-pull analysis was undertaken with the circuit of Figure 3 in order to chose optimized input and output impedances, improving the approximate values of Equation (1), and reaching a trade-off between performance and output power. Figure 4 shows the corresponding contours of the load-pull analysis for the desired frequencies, output power P_{out} (blue contours), and PAE (rose contours).

The triangle markers show the values of P_{out} (dBm) and PAE (%) of every contour. It can be noticed that the performance contours are more compressed at the higher frequency, which involves a greater sensitivity in the amplifier design. Anyhow, the design's maximum specifications are achieved through an optimization process, with the proper impedances for the harmonics, as shown in Table 1.

Table 1. Design specifications.

$f_1 = 380\,\text{MHz}$		
PAE = 70.95%	DCRF = 81.18%	$P_{out} = 27\,\text{dBm}$
$V_{ce} = 4.41 \cdot V_{cc}$	$Z_{in} = 16.56 - 36.27j$	$Z_{out} = 30.67 - 15.26j$
PAE = 66.64%	DCRF = 92.77%	$P_{out} = 26\,\text{dBm}$
$V_{ce} = 3.23 \cdot V_{cc}$	$Z_{in} = 13.01 - 4.12j$	$Z_{out} = 30.95 - 14.33j$

Table 2. Transmission line lengths.

f (MHz) / Line	f_1 = 380 MHz	$2 \cdot f_1$ = 720 MHz	f_2 = 960 MHz	$2 \cdot f_2$ =1920 MHz
Input Serie Line	14.45°	N.D.	27.75°	N.D.
Input Shunt Line	127.6°	N.D.	54.31°	N.D.
Output Serie Line	57.5°	±90°	54.8°	±90°
Output Shunt Line	45.4°	±90°	39.9°	±90°

Impedances of Table 1 are synthesized via transmission lines, which will have the electric lengths shown in Table 2.

3.1. CRLH Architecture

The CRLH property of being able to synthesize two different electric lengths for any two frequencies is used in the CRLH architecture of Figure 2(a), as Caloz showed in his original paper [4]. The elements of a CRLH line can be found (see Figure 5) solving the two-equation non-linear system, from Equation (3) which describes the behavior of the aforementioned structure.

$$\Phi_{\text{c}} = \Phi_{\text{L}} + \Phi_{\text{R}} = -\frac{\omega}{\omega_R} + \frac{\omega_L}{\omega} \tag{3}$$

where ω_R and ω_L are the rightwise and leftwise pulsations of the CRLH line. The structure's elements are shown in Figure 5, and the equations are given by Caloz [6].

The input and output were adapted via CRLH, programming the equations of Caloz [6] into a small programme. The results are shown in Table 3.

The circuit in Figure 6 has been simulated.

Table 3. Value of components of CRLH lines.

Component / Line	C_R (pF)	L_L (nH)	Length (°)
Input Serie CRLH	11.94 pF	29.86 nH	47.41°
Input Shunt CRLH	11.12 pF	27.8 nH	85.38°
Output Serie CRLH	11.42 pF	28.34 nH	49.77°
Output Shunt CRLH	9.78 pF	24.45 nH	47.24°

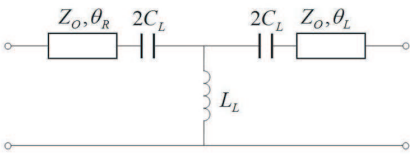

Figure 5. CRLH line elements.

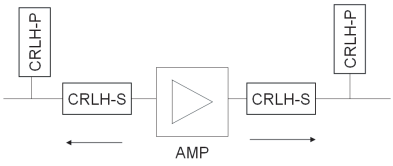

Figure 6. Amplifier with CRLH circuit.

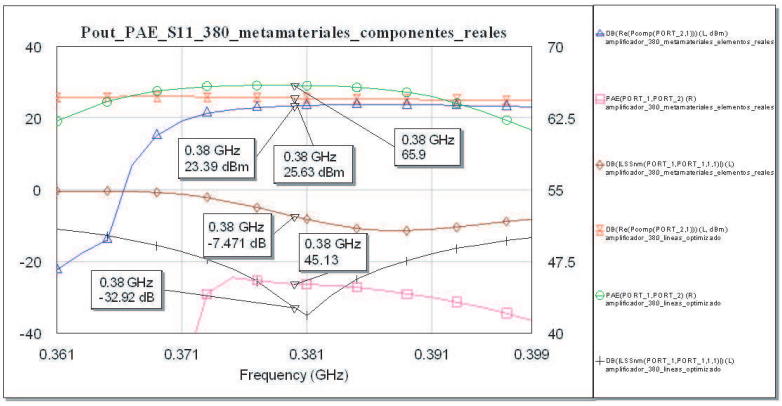

Figure 7. CRLH architecture simulation with actual components at 380 MHz.

Since the values obtained are lower than optimal, despite working with ideal lossless networks, it seems that actual implemented circuits will be even worse. It is worth noticing that results depend on the placement of harmonic loads, heavily regarding the second harmonic, and slightly concerning the third one. So, for second and third harmonics of TETRA band $Z_{2f1} = 60.2191 + 18.0293j$ and $Z_{3f1} = 59.5859 - 30.6641j$, whereas in GSM band $Z_{2f2} = 6.2524 - 14.4616j$

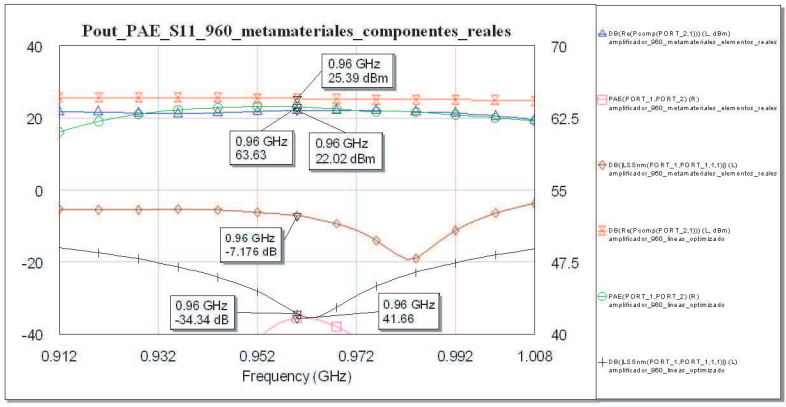

Figure 8. CRLH architecture simulation with actual components at 960 MHz.

and $Z_{3f2} = 56.6879 + 6.3468j$. This proves that control over harmonics is random or nonexistent. If we are considering lumped elements, from the analysis [19], we obtain the values of Figures 7 and 8. These results reveal an excessive circuit sensitivity and a drop in performance. So, it can be inferred that dual-band design, using CRLH structures as input and output matching networks, may present serious tuning problems and a slight drop in performance. Besides, a deep look at references [8, 9] makes authors doubt the design to have been carried out at the frequencies shown in the paper, being more likely that these frequencies were justified a posteriori.

3.2. E-CRLH Architecture

Compared to the former architecture, the new one, shown in Figure 2(b), offers an a priori improved control on length line for second harmonic at both frequencies, since E-CRLH line exhibits the property of handling its electric length at four frequencies, as Rennings describes [15]. To calculate the constituents of every E-CRLH line, the authors have had to develop a software capable of solving a non-linear four-equation system, following the Equation (4), from Rennings [15].

$$\Phi_c = \frac{\left(\omega^2 - \omega_{1e}^2\right) \cdot \left(\omega^2 - \omega_{2e}^2\right)}{\omega \cdot \omega_R^c \cdot \left(\omega^2 - \omega_o^2\right)} \tag{4}$$

where the different ω's correspond to the resonant pulsations of the E-CRLH line. They allow the evaluation of the line's components, as Rennings showed [15]. In Figure 9, the equivalent circuit of an E-CRLH line can be seen.

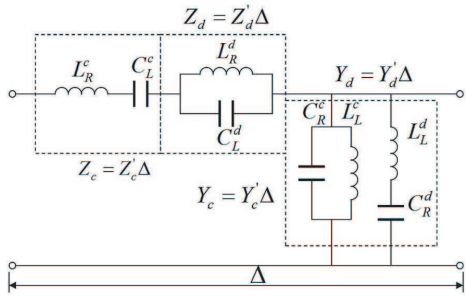

Figure 9. E-CRLH line.

Table 4. Components of E-CRLH lines.

Output Series ECRLH	$C_R^C = 1.34\,\text{pF}$	$L_R^C = 3.35\,\text{nH}$	$C_L^C = 10.25\,\text{pF}$	$L_L^C = 25.64\,\text{nH}$
	$C_R^D = 15.9\,\text{pF}$	$L_R^D = 39.7\,\text{nH}$	$C_L^D = 0.864\,\text{pF}$	$L_L^D = 2.161\,\text{nH}$
Output Shunt ECRLH	$C_R^C = 1.38\,\text{pF}$	$L_R^C = 3.35\,\text{nH}$	$C_L^C = 10.25\,\text{pF}$	$L_L^C = 24.81\,\text{nH}$
	$C_R^D = 1.0\,\text{pF}$	$L_R^D = 2.48\,\text{nH}$	$C_L^D = 13.78\,\text{pF}$	$L_L^D = 34.46\,\text{nH}$

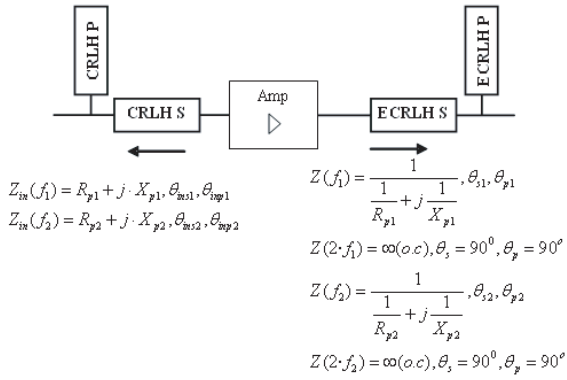

Figure 10. Simulated circuit with an E-CRLH line.

Input lines will correspond to conventional CRLH structures, and their values will be the ones previously calculated — see Table 3. On the other hand, the elements of output E-CRLH lines will be found out with the help of the developed programme, as shown in Table 4.

As in the previous case, the circuit shown in Figure 10 is simulated via AWR programme.

The obtained results (see Figures 11 and 12) have excessive losses that are mainly due to E-CRLH line behaviour. This behaviour is highlighted in Figure 13, where unacceptable losses can be observed at requested frequencies, making this line inadequate to implement high efficiency amplifiers.

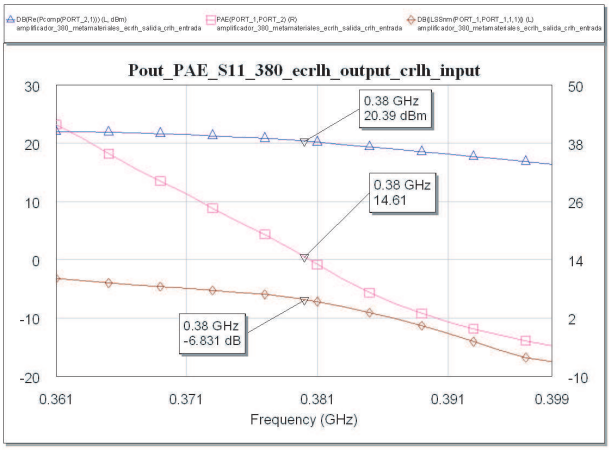

Figure 11. Simulation of E-CRLH architecture at 380 MHz.

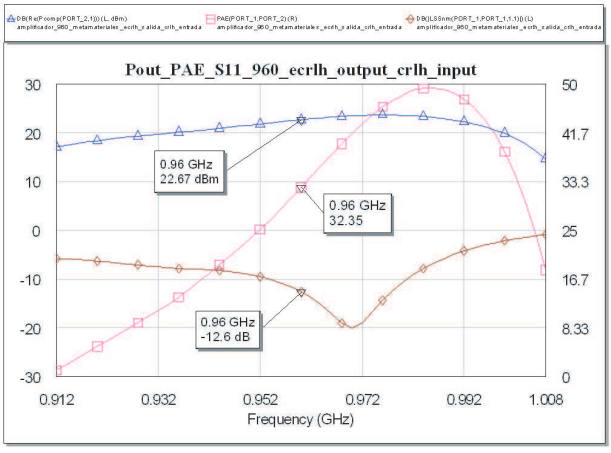

Figure 12. Simulation of E-CRLH architecture at 960 MHz.

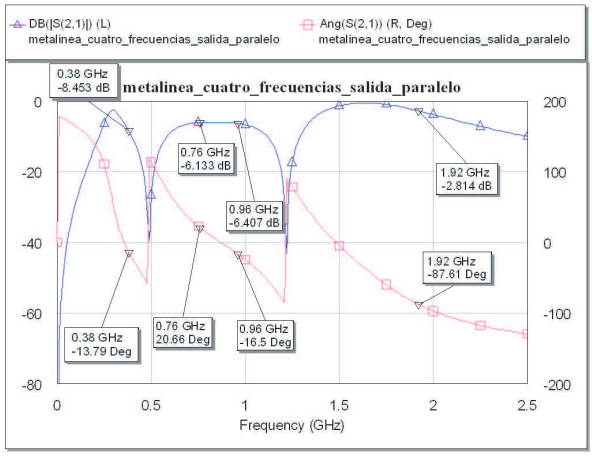

Figure 13. E-CRLH line behaviour.

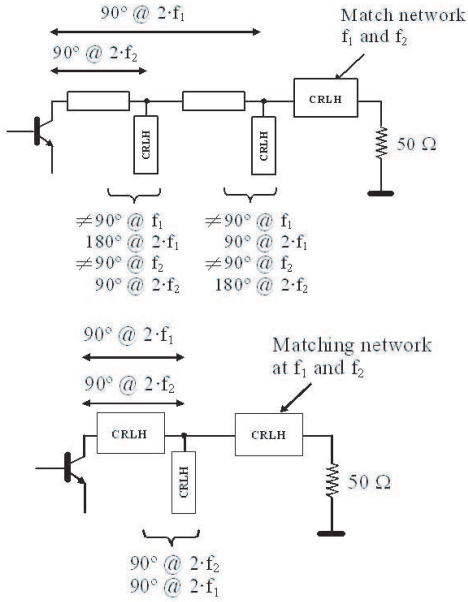

Figure 14. CRLH structures plus harmonic loading.

Given that the behaviour with ideal elements is inadmissible, there is no point in studying the sensitivity in order to evaluate the performance of a possible actual circuit. Therefore, this architecture is inadequate to implement dual band high efficiency amplifiers.

3.3. CRLH Architecture and Harmonic Ending

As a third way to develop the aforementioned amplifiers, different designs were tested (see Figure 2(c)). In this kind of architecture the key point is finding a structure capable of offering an open circuit at harmonics of the frequencies to amplify, while matching with a CRLH line at fundamental frequency. This architecture may show a great number of possible solutions, as the examples in Figure 14 that will be simulated later.

So, in the circuit of Figure 15, first, the open circuit was assured, and then, optimal impedances were obtained, for input and output, by means of load-pull. The results were $Z_{f_1} = 16.3206 + 9.0454j$ at f_1 and $Z_{f_2} = 5.6744 - 15.4851j$ at f_2, with a greater contour density in the surroundings of the impedances, meaning the structure is more sensitive at higher frequency.

As the former cases, simulations were carried out, resulting in Figures 16 and 17. While a better performance can be noticed with respect to Figures 2(a) and 2(b) topology, the bandwidth has decreased.

From the statistical sensitivity study of Figure 18, high values are achieved, as predicted in the previous analysis of power and

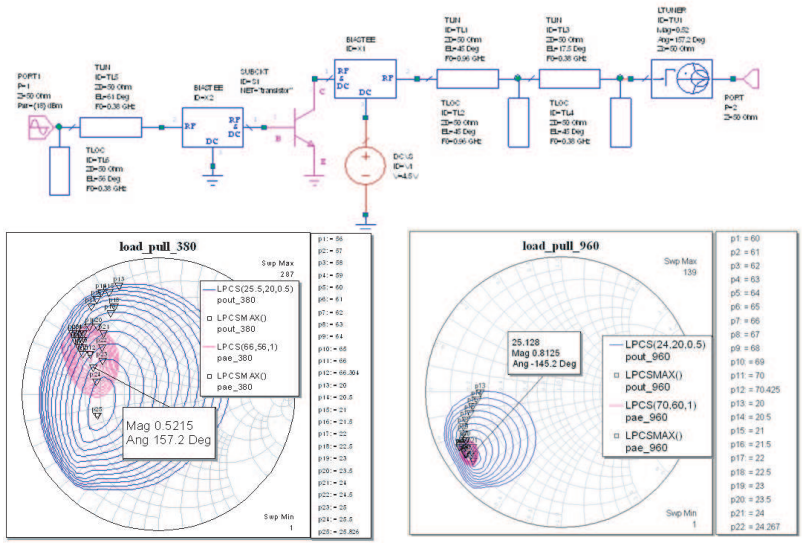

Figure 15. CRLH structures plus simulated harmonic loading.

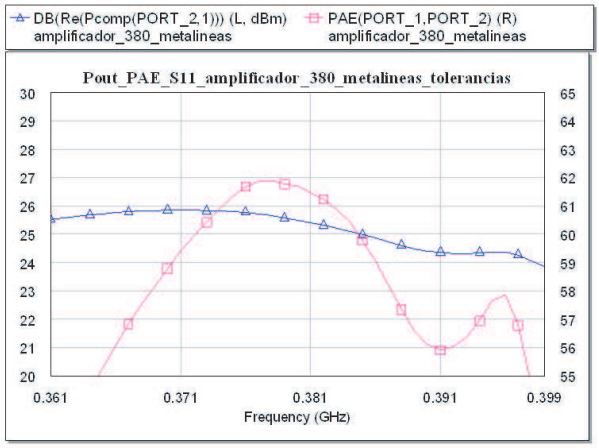

Figure 16. Simulation of CRLH architecture plus harmonic loading at 380 MHz.

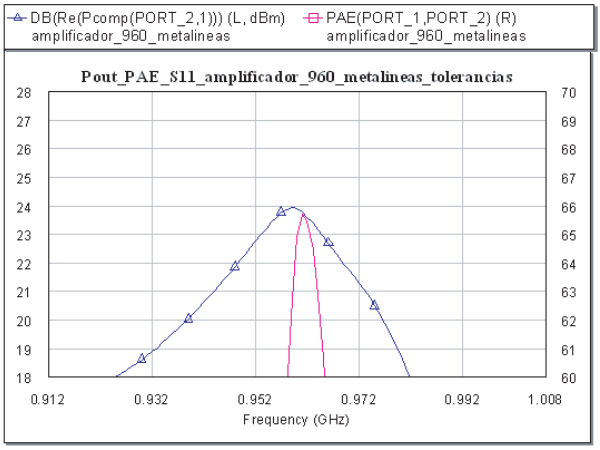

Figure 17. Simulation of CRLH architecture plus harmonic loading at 960 MHz.

performance circles of load-pull shown in the Figure 15. This makes us guess that we are not dealing with the most adequate structure to implement dual band high efficiency amplifiers, raising doubts on Dupuy claims [9].

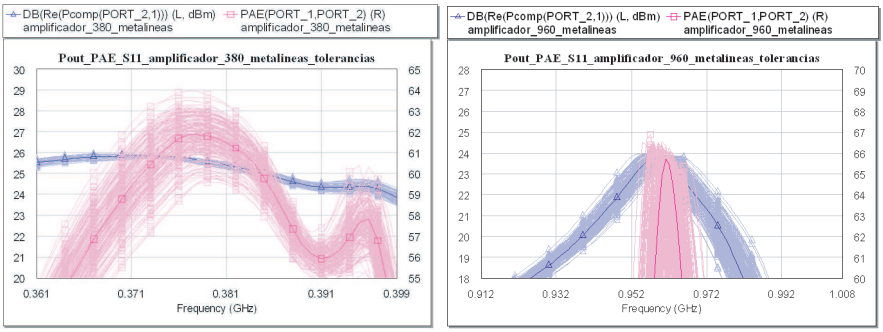

Figure 18. Statistical sensitivity study of CRLH architecture plus harmonic loading at 380 MHz (right) and 960 MHz (left).

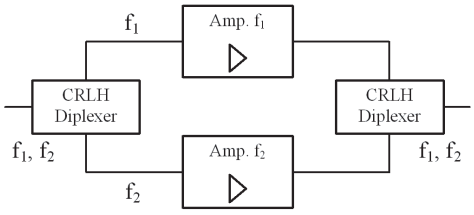

Figure 19. Dual band high efficiency class CE power amplifier with diplexers.

4. DUAL-BAND CLASS-CE AMPLIFIER WITH D-CRLH

In the previous sections we established CRLH lines based on that lumped components do not seem to be adequate to implement dual-band high-efficiency class CE amplifiers. As a way to overcome this problem, authors suggest the use of CRLH lines when implementing diplexer or combiner structures (see Figure 19).

A new diplexer structure with D-CRLH was developed by authors, at the aforementioned bands [18], taking into account Caloz's previous experience in passive structures and his work about D-CRLH lines [17] to minimize some similar-behaviour circuits, like the baluns proposed by Xin [20].

4.1. Design Process of Dual-band Class CE Amplifier with D-CRLH

The design process of dual-band class CE amplifier with D-CRLH is detailed above. The following steps are to be done:

- A device and two frequencies are selected. Both frequencies must be far away enough, since close ones would not allow a wide band design. In this case, as in all the others, the choice will be BFG591, 380 MHz (TETRA) and 960 MHz (GSM).
- Two completely equal diplexers are designed, making use of the equations of [18], to obtain the circuit of Figure 20.

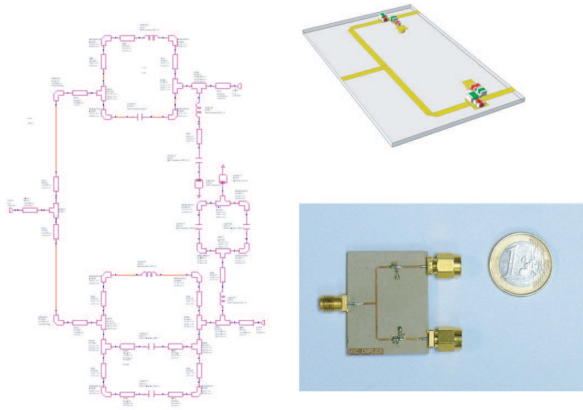

Figure 20. D-CRLH diplexer.

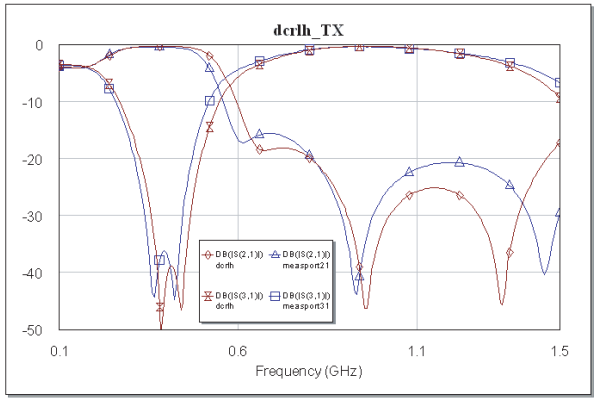

Figure 21. D-CRLH diplexer simulations and measures.

The excellent agreement between simulation and measurements is shown in Figure 21. The insertion losses of diplexer are 0.2 and 0.3 dB, in each band, respectively, and the isolation is above 35 dB. This agreement can be extended to the rest of the diplexer parameters.

- High efficiency CE amplifiers are designed, in an individual way, for every selected frequency, using load-pull contours. The obtained designs at 380 and 960 MHz are shown in Figures 22 and 23. The final structure has been manufactured with an additional class A amplifier for every frequency, working as a amplifier driver. The obtained results and measures can be observed in Figures 24 and 25.

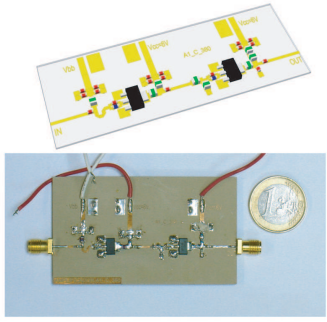

Figure 22. High efficiency CE amplifier at 380 MHz.

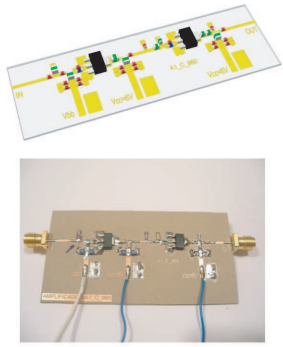

Figure 23. High efficiency CE amplifier at 960 MHz.

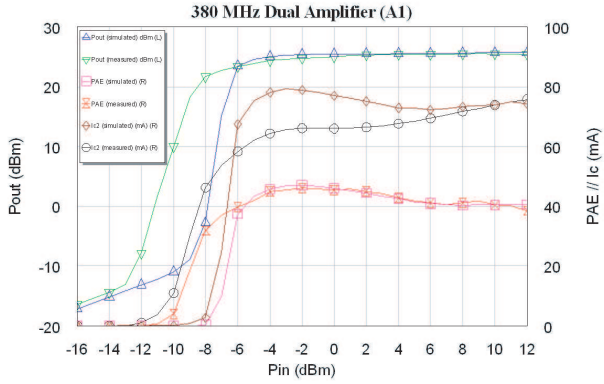

Figure 24. Simulations and measures of single CE amplifier at 380 MHz.

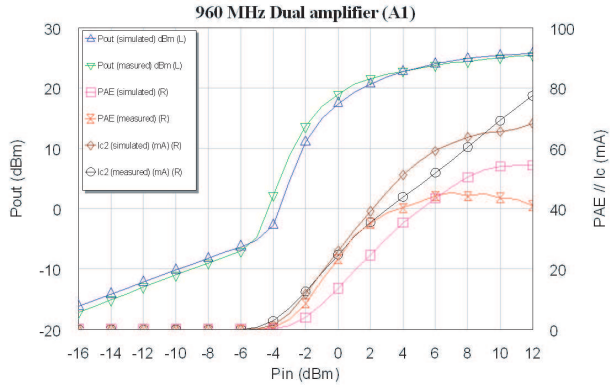

Figure 25. Simulations and measures of single CE amplifier at 960 MHz.

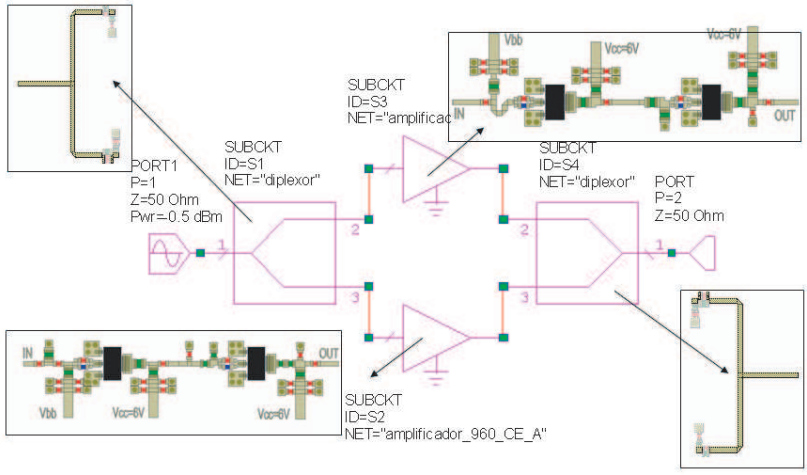

Figure 26. Dual-band high efficiency CE amplifier at 380 and 960 MHz.

The results show that while initial power requirements are fulfilled, PAE is not. An improvement of the driver was undertaken, using as load the class CE input impedance. This way, a 10% increase is achieved, which can be regarded as an adequate value.

- Simulation of the whole structure. The structure made by both amplifiers and diplexers, as can be seen in Figure 26, is simulated and optimized.

The obtained results are shown in Figures 27 and 28, where it is worth noticing that PAE values are high, above 60%, at both frequencies, and collector efficiency is 77% at 380 MHz and 89% at 960 MHz. These can be regarded as excellent results, despite the fact that there is a small convergence error for low powers in the optimal region.

- And last, before the manufacturing process, a statistical sensitivity analysis is made to assure the viability of the final design and the scattering in the obtained results. The sensitivity analysis was undertaken with 200 samples, with uniform distribution, ±5% tolerance for coils, capacitors and transistors, and ±1% for substrate permittivity. As shown in Figures 29 and 30, sensitivity is low. Therefore, this design seems optimal for dual band

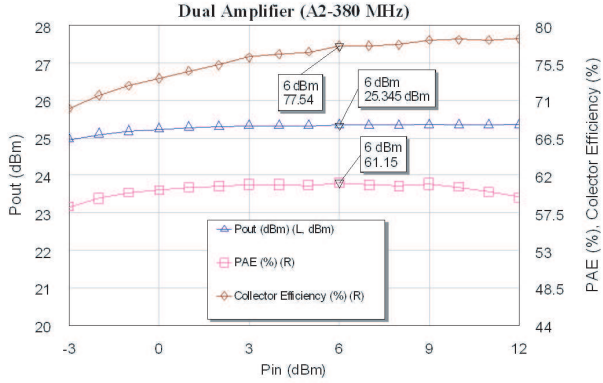

Figure 27. Dual-band high efficiency CE amplifier simulations at 380 MHz.

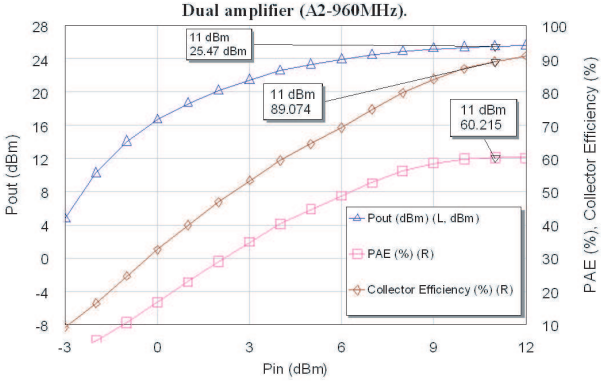

Figure 28. Dual-band high efficiency CE amplifier simulations at 960 MHz.

amplifiers.

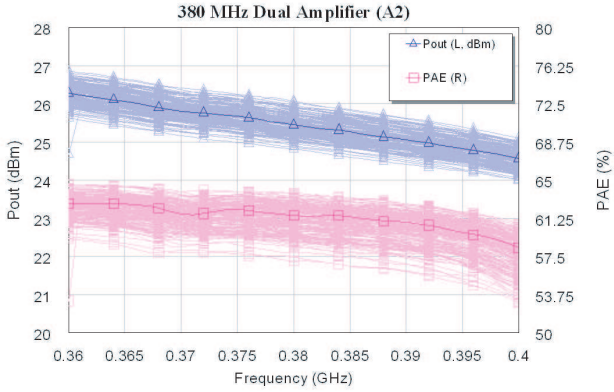

Figure 29. Statistical sensitivity study of a dual-band high-performance amplifier at 380 MHz.

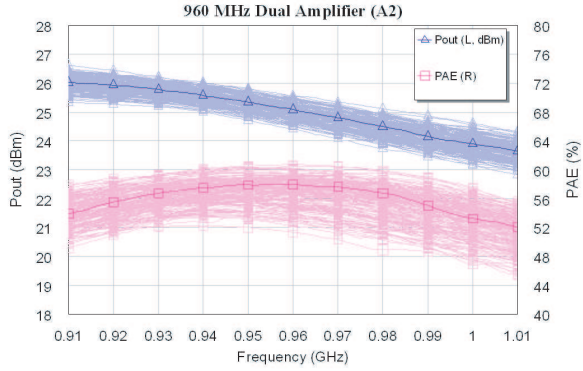

Figure 30. Statistical sensitivity study of a dual-band high-performance amplifier at 960 MHz.

4.2. Prototypes and Obtained Results

At least two prototypes of the aforementioned structure have been made. In Figure 31, the photograph of one of the prototypes is shown. The driver, high performance final stages, diplexers, and additional needed circuits to polarize the amplifier can be seen.

Once measurements were made, the excellent results were confirmed, as well as the great agreement between simulations and measurements, as can be seen in Figures 32 and 35.

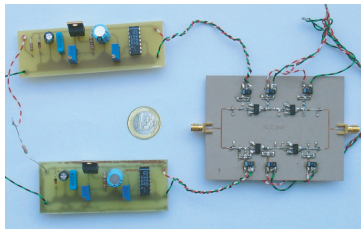

Figure 31. Implementation of a dual-band high-performance amplifier at 380 and 960 MHz.

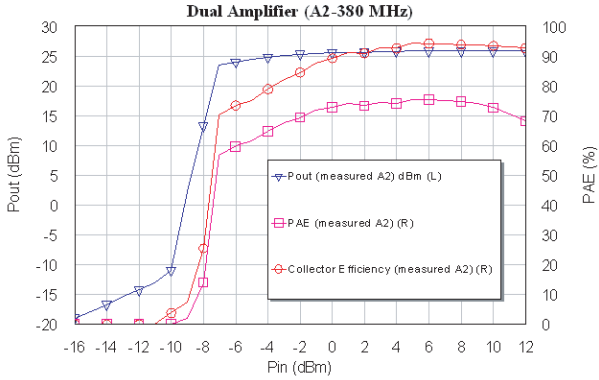

Figure 32. Power measures of a dual-band high-performance amplifier at 380 MHz.

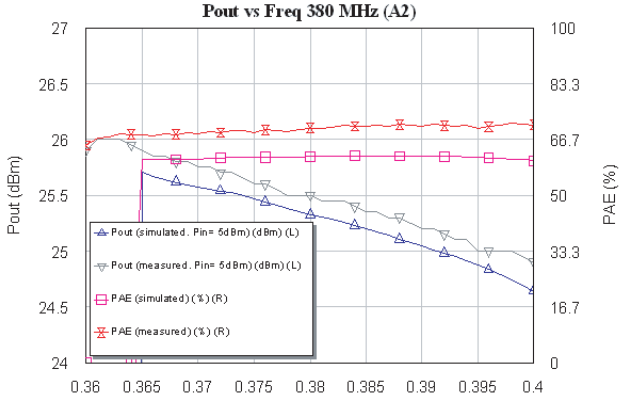

Figure 33. Frequency measures of a dual-band high-performance amplifier at 380 MHz.

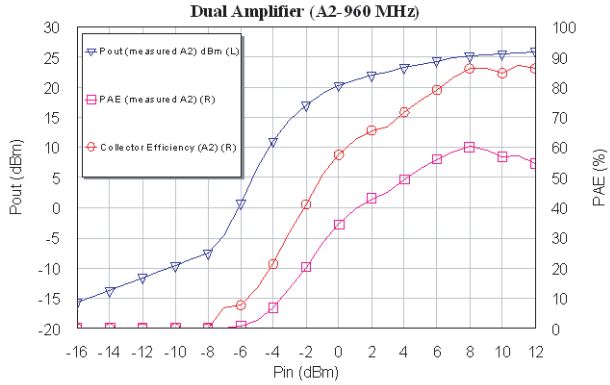

Figure 34. Power measures of a dual-band high-performance amplifier at 960 MHz.

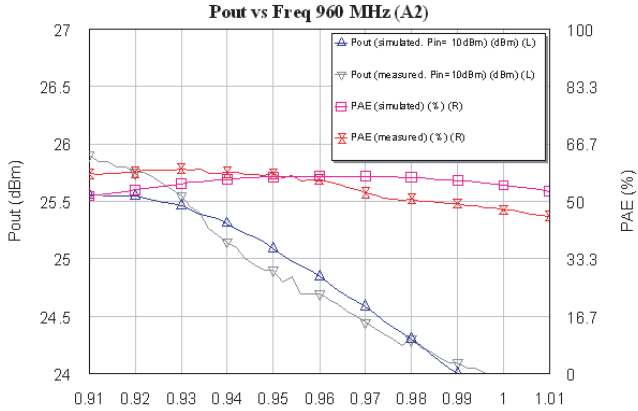

Figure 35. Frequency measures of a dual-band high-performance amplifier at 960 MHz.

These results highlight the goodness of the proposed design, supporting the use of CRLH as mixer structures in dual band amplifiers.

5. CONCLUSION

The obtained conclusions follow the two paths shown in this paper. In the first part, a study of the different structures based on CRLH lines

has been undertaken. As it has been proven via simulations, CRLH lines made by conventional components are not suited to implement dual-band class CE amplifiers. This could be extended to any type of amplifier, concluding that these structures lack of interest, due to the narrow band they offer, and the excessive statistical sensitivity with component's tolerance.

In the second part, a dual-band high performance amplifier, based on metamaterials, is shown. CRLH lines (concretely D-CRLH ones) have been used to synthesized two diplexers, one at the input and another at the output, which have an excellent behaviour. As far as the authors are concerned, this is the only acceptable solution so as to use CRLH lines in the field of dual band high performance amplifiers in CE mode.

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