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DESIGN OF 3 TO 5 GHz CMOS LOW NOISE AMPLIFIER FOR ULTRA-WIDEBAND (UWB) SYSTEM

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Abstract—A single-stage ultra-wideband (UWB) CMOS low noise amplifier (LNA) employing interstage matching inductor on conventional cascode inductive source degeneration structure is presented in this paper. The proposed LNA is implemented in 0.18 µm CMOS technology for a 3 to 5 GHz ultra-wideband system. By careful optimization, an interstage inductor can increase the overall broadband gain while maintaining a low level of noise figure of an amplifier. The fabricated prototype has a measured power gain of +12.7 dB, input return loss of 18 dB, output return loss of 3 dB, reverse isolation of 35 dB, noise figure of 4.5 dB and input IP3 of −1 dBm at 4 GHz, while consuming 17 mW of DC dissipation at a 1.8 V supply voltage.

1. INTRODUCTION

Currently, the emerging of high speed and high data-rate wireless communications has encouraged intensive research in both academic and industrial fields. Ultra-wideband (UWB) system, as compared to Bluetooth and WiMax has emerged as a new technology capable of offering a high data-rate and wide spectrum of frequency (low

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frequency band from 3.1–5 GHz and high frequency band from 6–10.6 GHz) with very low power transmission [1]. Two major solutions, MB-OFDM based on frequency hopping and DS-UWB are proposed to transmit the data rate up to 480 Mbps by using only the low frequency band. This low frequency band (3168 MHz to 4752 MHz) is decided as the mandatory mode (Mode 1) for the development of the first-generation UWB system.

The low noise amplifier (LNA) circuit remains as one of the challenging tasks in receiver design as it must meet several stringent requirements such as low noise figure (NF) to improve sensitivity, optimum gain to reduce the noise of mixer, broadband input matching to improve reflection coefficient and reasonable efficiency for low power consumption. Various topologies have been used in the implementation of wideband low noise amplifiers. Among that have been reported are the resistive shunt feedback topology [2], distributed topology [3], multi-stage cascaded amplifiers (common gate-common source) topology [4] and the LC matching and filtering topology [5–7]. Generally, the choice of topology used compromise the required noise performance, power dissipation as well as overall gain of the amplifier.

In this paper, the design and implementation of a modified single-stage cascode inductive degeneration with interstage matching inductor LNA for UWB receiver using 0.18 µm standard RF CMOS process is proposed. The design considerations and on-wafer (die) measurement results of the implemented 3 to 5 GHz UWB LNA are also presented. The paper is organized as follows. Section 2 describes the design approach for the proposed LNA which cover the topology used together with its optimization and selection criteria. The chip layout and measurement results for the proposed LNA in a 0.18 µm CMOS process are reported in Section 3. Finally, Section 4 presents the conclusion of this work.

2. UWB LNA CIRCUIT DESIGN

In this work, the proposed LNA rely on the use of interstage inductor in order to achieve optimum noise figure and gain while maintaining a wideband bandwidth. The proposed design are simulated and optimized with Agilent Technologies's Advanced Design System (ADS) software before CMOS IC layout and fabrication. BSIM (Berkeley Short-channel IGFET Model) signal model version 3.3 is used for the CMOS transistor modeling and the passive on-chip components (spiral inductors, metal-fingered capacitors, pads and interconnects) are modelled by RLC equivalent networks in the circuit schematics. Thus, all relevant parasitic values are taken into account for circuit

simulations.

Although the modified single-stage cascode with interstage matching inductor topology has been introduced and simulated in [8, 9], their simulation works are mainly confined to narrowband amplifiers design in the range of 2 to 2.4 GHz. In this work, this topology is further studied with careful optimization for wideband frequency operation. The proposed modified single-stage cascode with interstage matching inductor LNA (without buffer) is shown in Fig. 1. The proposed cascode topology can be viewed as a two-stage amplifier configuration consisting of a common source (CS) stage, an interstage inductor and a common gate (CG) stage, as shown in Fig. 2. In this work, the CS stage is designed to produce an optimum gain at 3 GHz using inductive degeneration while the noise figure of the CG stage is optimized at 5 GHz together with an interstage matching inductor. By ignoring the Miller effect of gate-drain capacitance (C_{gd1}) of transistor M_1, the input impedance of M_1 is given by [10]:

$$Z_{in1} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs1}} + \frac{g_{m1}L_s}{C_{gs1}} \tag{1}$$

where g_{m1} and C_{gs1} are the transconductance and the gate-source capacitance of M_1. Inductors L_s and L_g are the source degeneration inductor and the gate input inductor. The real part of the input impedance in (1) is given by:

$$\mathrm{Re}\{Z_{in1}\} = \frac{g_{m1} \cdot L_s}{C_{gs1}} \tag{2}$$

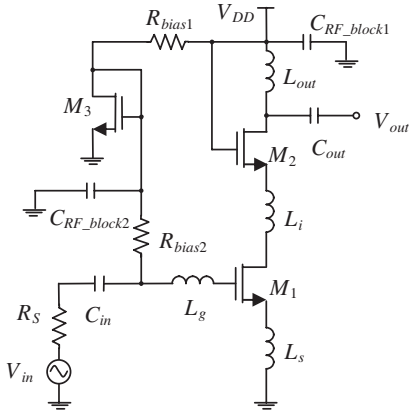

Figure 1. Schematic of the proposed single-stage UWB LNA.

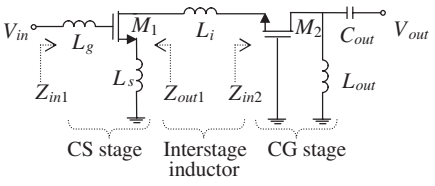

Figure 2. The cascode topology viewed as two cascading stages.

With given values of g_{m1} and C_{gs1}, the desired impedance to match to R_s (usually 50 Ω) can be obtained by setting L_s accordingly. Next, the imaginary part of the input impedance can be compensated with an input matching inductance L_g. The corresponding resonance frequency is approximated by:

$$\omega_0 \approx \sqrt{\frac{1}{(L_s + L_g)C_{gs1}}} \tag{3}$$

The output impedance of the CS stage and the input impedance of the CG stage are given as follow [11]:

$$Z_{out1} = \frac{r_0}{jr_0\omega C_{ds1} + 1} \tag{4}$$

$$Z_{in2} = \frac{1}{j\omega_0 C_{gs2} + g_{m2}} \tag{5}$$

where r_0 is the parallel connection between the small signal output resistance and the parasitic channel resistance and C_{ds1} is the drain source capacitance for M_1. Both g_{m2} and C_{gs2} are the transconductance and the gate-source capacitance of M_2 respectively.

Since both the impedances are capacitive, a series inductor L_i can be placed to improve the matching between these two stages. This will significantly increase the gain at the CG stage due to maximum power transfer. In addition, the overall noise figure of the amplifier will also be reduced. However, due to the parasitic capacitance values of the on-chip inductor, a proper optimization is required to determine the optimum value of L_i.

In the CS stage, the source degeneration inductor L_s is added for simultaneous noise and input matching where as L_g is needed for the impedance matching between the source resistance (R_s) and the input of transistor M_1 [10]. In this stage, the size of M_1 is chosen to be 160 µm for optimum input matching and noise performance. After determining the optimum size of M_1, the inductor L_s needs to be selected carefully since it improves linearity and stability but at the same time it reduces the gain of the LNA [10]. In order to reduce the chip area, the value of L_s is chosen to be small enough, approximately 0.5 nH. The importance of L_s in stabilizing the LNA (for Rollet's stability factor, $K > 1$) is illustrated in Fig. 3. Next, the values of R_{bias2} and L_g are optimized carefully because they affect the overall gain of the CS stage. The simulated frequency response of the CS stage is shown in Fig. 4. Here, R_{bias2} is fixed at 2 kΩ, which is sufficiently large enough to provide an optimum voltage V_{gs} to transistor M_1, while L_g is optimized at 3.5 nH in order to provide

good matching at the input. As depicted in Fig. 4, the simulated gain of the CS stage is approximately 8.9 dB at 3 GHz.

In the CG stage, an inductor L_{out} of approximately 4 nH is placed as shunt peaking inductor resonating with its parasitic capacitances at the drain of transistor M_2 around 5 GHz. In addition, it is also used as RF choke to block any RF signal leaking back to the DC supply. In practice, a large transistor size M_2 is often used to provide high reverse isolation and gain of the amplifier at high frequency. However, large transistor size usually has high parasitic capacitance and transconductance, which will increase the power consumption [12]. In some cases, large value of peaking inductance (L_{out}) is usually used to tolerate a larger size of M_2 due to its high parasitic capacitance, but it will further increase the area of the chip. The simulated response together with power dissipation of the CG stage using different transistor size is shown in Fig. 5. As seen in this simulation result, the gain of the CG stage will increase significantly with the use of large transistor size for M_2. However, a large size of M_2 will have higher transconductance which will increase the velocity of the carriers, and hence a higher dc current in the drain. This will result in larger dc power consumption. Therefore, the transistor size for M_2 is maintained at 160 µm for its reasonable parasitic capacitance and moderate power consumption. After determining the required transistor size, the value of the interstage matching inductor L_i is now optimized for optimum gain and noise figure. The simulated gain and noise figure using different on-chip spiral inductor is shown in Fig. 6. Here, a large value of L_i will produce a high gain and low noise figure performance, but with the expense of larger chip area. A 3 nH square spiral inductor occupied an area of approximately 40 nm^2 where as a

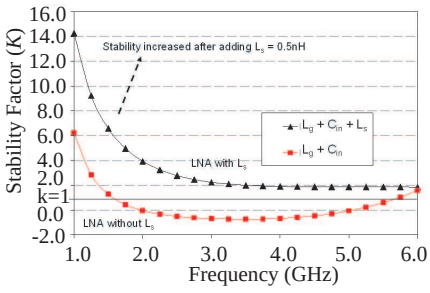

Figure 3. Stability of LNA represented by Rollet's factor (K) with L_s.

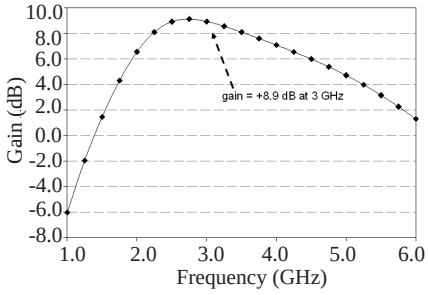

Figure 4. Simulated frequency response of the CS stage.

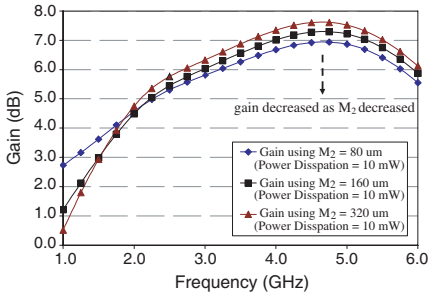

Figure 5. Simulated frequency response of the CG stage using different M_2.

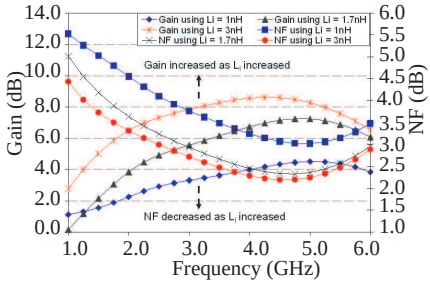

Figure 6. Simulated gain and noise figure of the CG stage using different interstage matching spiral inductors, L_i.

1.7 nH inductor only has an area of approximately 22 nm^2 [10]. In this work, the value of 1.7 nH is chosen due to its optimum gain and noise performance. In addition, it will be relatively easier to replace L_i with a bondwire inductance if necessary.

Finally, a capacitor C_{out} is placed at the output as a dc block. The overall biasing network of the LNA is formed by two resistors R_{bias1} and R_{bias2} and a transistor M_3. Transistor M_3 is a current mirror with M_1, and its width is some small fraction of M_1's width in order to minimize the power overhead of the bias circuit. The current through M_3 is set by the supply voltage (V_{DD}) and biasing resistors in conjunction with the V_{gs} of M_1. The biasing resistors are chosen large enough so that their equivalent noise current is small enough to be ignored [10]. A large value of R_{bias2} is also used as RF choke to provide RF signal isolation from the input. Depending on the amount of bandwidth and noise required, these resistors can be varied accordingly to provide their conventional roles of flattening the gain over a wide bandwidth. In order to provide RF shunting, two large on-chip capacitors (C_{RF_block1} and C_{RF_block2}) are included in the circuit. The simulated frequency response of the combined CS and CG stages is shown in Fig. 7.

3. EXPERIMENTAL RESULTS

The proposed LNA have been fabricated in Silterra Malaysia Sdn Bhd 0.18 µm CMOS process with testing pads and it occupies an area of 1.10 mm × 1.23 mm. The die microphotograph is shown in Fig. 8. L_i and L_g are arranged at the bottom, so that they can be easily removed and replaced by bondwire inductance during packaging,

if required. The NMOS used in the design is multi-fingered thin gate oxide transistor where each finger is of size 2.5 µm/0.18 µm. Body of the transistors are connected using a Metal 1 ring structure and are biased to the lowest potential signal such as ground. All capacitors are implemented by metal-fingered where it is made up of unit capacitor cells consisting of interdigitated tines connecting to alternating terminals of the capacitor array. For the ease of on-wafer characterization, all inductors are also implemented on on-chip spiral inductors, where each inductor is drawn within a deep $N-$ Well layer. The line width of the inductor is 10 µm and the spacing between the metal lines is 2.0 µm. The resistors used are of type silicide-blocked $N+$ Poly resistor. A guard ring is used in all three layouts in order to prevent latch-up and also to reduce the substrate noise.

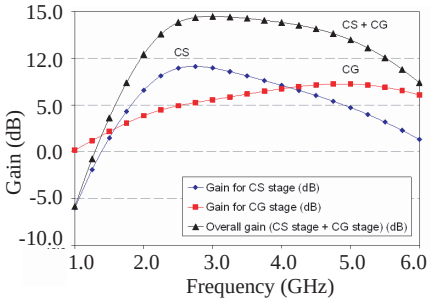

Figure 7. Simulated gain of the LNA.

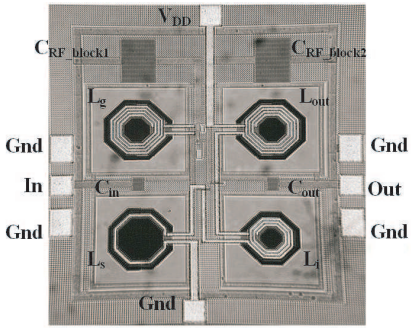

Figure 8. Die micrograph of the proposed LNA.

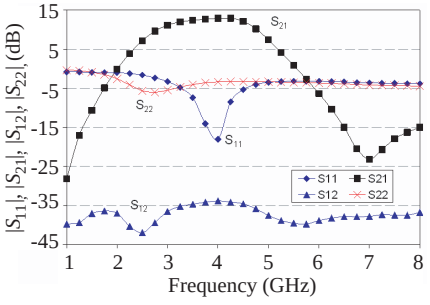

Figure 9. Measured S-parameters.

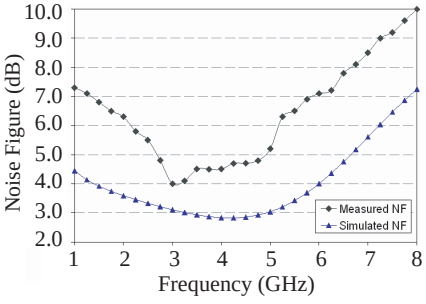

Figure 10. Measured noise figure.

On-wafer measurements are carried out for gain, input/output return loss, noise figure (NF), 1 dB gain compression (P1dB) and third order intercept point (IP3). Small-signal measurements were conducted using network analyzer with SOLT calibration performed at the probe tips using standard Alumina calibration substrate. The measured S-parameter data are shown in Fig. 9. The measured results show that the LNA has a maximum gain of +12.9 dB at 4.25 GHz and a 3 dB bandwidth covers 2.8 to 4.7 GHz. The minimum input return loss (approximately −18 dB) occurred at 4 GHz, which means that the input impedance is matched at this frequency. As shown in Fig. 9, the LNA has a minimum output return loss of −3.3 dB over the 3 to 5 GHz range. The input and output return losses can be further improved by using external components if necessary. It also maintained a high reverse isolation (S_{12}) of more than −35 dB across 1 to 8 GHz. Using the measured S-parameter data, the stability factor (K) is also computed and its value is larger than 1 (unconditionally stable) across the interested frequencies, ranging from 1 to 8 GHz.

The measured and simulated NF results are shown in Fig. 10. The measured NF is approximately 4 to 5.3 dB from 3 to 5 GHz. The discrepancies in NF between the measurement and simulation results are probably due to the inaccuracies in transistor noise model, as well as the parasitic capacitances in the interstage matching inductor. As shown in Fig. 11, the input P1dB for 3, 4 and 5 GHz are −9 dBm, −9.2 dBm and −12 dBm respectively The two-tone test is performed with 10 MHz spacing for third order intermodulation distortion, which is shown in Fig. 12. At 4 GHz, the measured input IP3 is approximately −1 dBm. Table 1 summarize the measurement results and compare them with previously reported works using 0.18 µm CMOS processes especially for UWB LNAs.

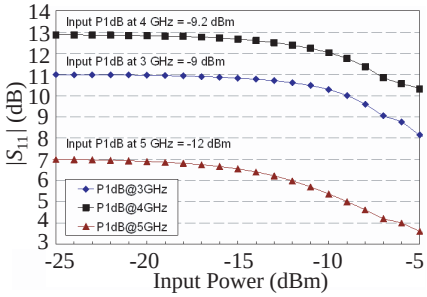

Figure 11. Measured input P1dB for 3, 4 and 5 GHz.

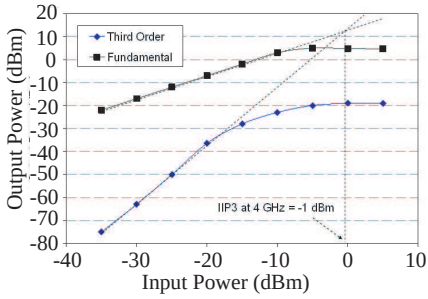

Figure 12. Measured input IP3 at 4 GHz.

Table 1. Comparison of wideband LNAs : Published and the present works.

Ref.	Tech.	3 dB BW (GHz)	S_{11} (dB)	S_{21max} (dB)	NF (dB)	IIP3 (dBm)	Supply (V)	Power (mW)	Remarks
[2]	0.18 µm CMOS	2–4.6	< –9	9.8	2.3–5.2	–7	1.8	12.6	Resistive feedback (2-stage)
[3]	0.18 µm BiCMOS	1–8	< –10	8	2.9–4	–3.4	1.8	21.6	Distributed (3-stage)
[4]	0.18 µm CMOS	0.4–10	< –5	12.4	4.4–6.5	–6	1.8	12	Multi-stage (3-stage)
[5]	0.18 µm CMOS	3.4–8.2	< –7	20.4	3.3–6.4	–14.7	1.8	17.3	LC filters (2-stage)
[6] [Simulated]	0.18 µm CMOS	2.8–5	< –5	19.9	0.6	+18	1.8	23	LC filters (2-stage)
This work [Measured] [Simulated]	0.18 µm CMOS	2.8–4.7 2–5	< –3* < –6	12.9 14.9	4–5.3 2.8–3.2	–1 +3.1	1.8	17 14	Interstage matching inductor (1-stage)

* can be improved with bondwire or off chip components.

4. CONCLUSION

A 0.18 µm CMOS UWB LNA for lower band UWB system (3 to 5 GHz) is systematically designed, simulated and tested in this work. By using an interstage matching inductor on the conventional cascode amplifier, the proposed LNA achieved a +12.7 dB gain and +4.5 dB noise figure at 4 GHz with a 3 dB bandwidth of 2.8 to 4.7 GHz, while consuming a DC power of 17 mW. The proposed circuit occupy an area of $1.10 \times 1.23\,\text{mm}^2$. This size can be further reduced if external bondwires inductance are used to replace L_i and L_g during packaging. Compared to other broadband techniques, the proposed LNA has less design complexity with only three transistors in a single stage topology and it is very cost effective if bondwires inductance are used.

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