INTEGRATED COMPACT BROAD KA-BAND SUB-HARMONIC SINGLE SIDEBAND UP-CONVERTER MMIC

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Abstract—Design, simulation and measurement results of the integrated compact up-converter MMICs (microwave monolithic integrated circuits) are presented and discussed. The design is performed to achieve low cost and high performance transmitter system for the Ka-band frequency applications. It is designed using anti-parallel diode pair sub-harmonic single sideband mixer and three stage RF (radio frequency) amplifier. Microstrip lines and lumped elements are used together to achieve a compact chip size. The layouts of the circuits are designed with careful EM (electromagnetic) simulations to avoid inter-component couplings and effect of the microstrip bending discontinuities. The chip is operated for the wide bandwidth of the RF frequency from 22–38 GHz. Due to sub-harmonic mixing the required local oscillator frequency (LO) is reduced to half (10–19 GHz) to that of the RF frequency. The conversion gain of the chip is 9–15 dB and $P_{-1\,\text{dB}}$ output power is 7–12 dBm. The single sideband and anti-parallel diode pair suppress the in-band unwanted sideband and second harmonic of the local oscillator (2LO), respectively. The suppression of sideband and 2LO signals is typically 20–35 dB and 20–30 dB, respectively. The size of the chip is as compact as 4.2 mm^2 on a 100 μm-thick GaAs substrate.

1. INTRODUCTION

Wireless systems at Ka-band frequencies have application in point-to-point, point-to-multipoint, and very small aperture terminal (VSAT) systems. These systems support the growing needs for low cost and higher data transmission rates in consumer and professional

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interactive media (telephone, video, and computer data) for the family entertainment and business applications. The LMDS (local multipoint distribution systems) at Ka-band are developed for this purpose. The transceiver system at such high frequency band is the most expensive part and is realized using number of the MMICs such as LO frequency doublers, mixers, RF amplifier, low noise amplifier, variable attenuator, and power amplifier. The design of transceiver module using such large number of chips becomes complex. The complexities exist in fabrication and processing of the number of chips, assembly, interconnect mismatches and losses. This increases the cost of the system and degrades performance. The multifunction chip integrates a number of functions in a single chip to reduce the number of chips in transceiver module. However, for the integrated solution the chip size should be compact to reduce the cost of the system and with the high performance. Due to number of advantages the integrated chips become ultimate solution for the low cost and high performance transceiver systems at high frequency band. The performance of some Ka-band sub-harmonic and single sideband mixers can be found in the references [1–9]. Vaudescal et al. have presented the integrated up- and down-converter MMICs for the customer premise equipment application at 28 GHz [10]. The design was focused for the compact chip size to provide low cost solution. The conversion gain and output power of the up-converter was only 5 dB and 3 dBm, respectively. Mahon et al. have also reported low band and high band up- and down-converters [11]. However, there is lack of publications on the integrated Ka-band up- and down-converter MMICs and their detailed study by comparison of simulation and measurement results.

In this paper, we presented in detail the design of compact integrated Ka-band up-converter to replace number of MMICs in the transmitter module. This will reduce transmitter design complexity, cost, and provide high performance. A wideband compact sub-harmonic single sideband mixer and wideband three stage RF amplifier is integrated. Sub-harmonic mixing reduces local oscillator frequency requirement by half as it is easier to obtain high performance oscillator at lower frequency. The circuit is designed to meet the conversion gain (> 10 dB) and output power (0–10 dBm) requirement of the transmitter module. The single sideband design suppresses the unwanted sideband frequency. In addition the anti-parallel diode mixing suppresses the undesired second harmonic of the local oscillator (2LO) signal. The suppression of sideband and 2LO signals is indispensable as these undesired signals are very close to the desired one. The topology of the circuit is decided to meet the compact layout size and advanced circuit performance. The circuit was implemented

using WIN semiconductor's standard $0.15\,\mu m$ GaAs pseudomorphic high electron mobility transistor MMIC technology on a $100\,\mu m$ substrate thickness.

In Section 2 of this paper we presented design concept and simulation results of the each individual sub-circuits of the chip. In Section 3 the simulation and measurement results of the integrated chip is presented and discussed. Finally, the performance of the circuit is concluded in Section 4.

(a)

(b)

(c)
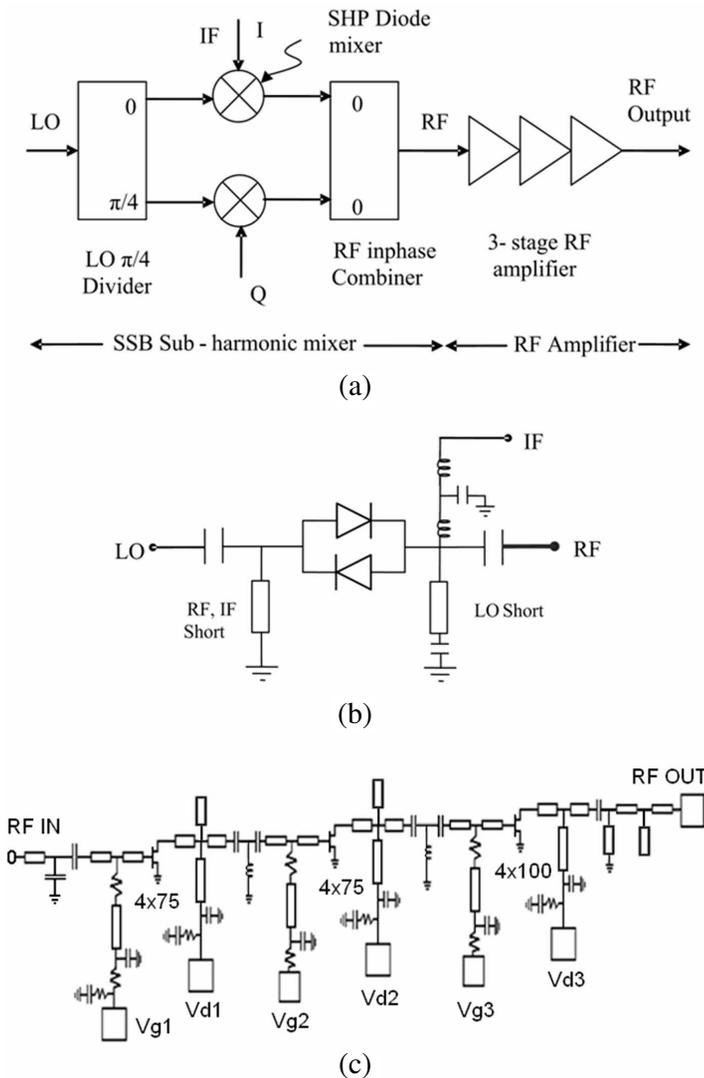
Figure 1. Schematics of the (a) integrated circuit, (b) SHP mixer, and (c) 3-stage RF amplifier.

2. DESIGN AND RESULTS OF THE UP-CONVERTER SUB-CIRCUITS

The schematic of the integrated up-converter chip is shown in Figure 1(a). It consists of wideband sub-harmonic single sideband (SSB) mixer followed by a three stage wideband RF amplifier. To achieve the sideband suppression, the LO signal is divided into two ways with 45° phase shift at sub-harmonic frequency to pump two sub-harmonically pumped (SHP) mixers. After mixing the IF frequency (f_{IF}) with second harmonic of LO frequency ($2f_{LO}$), two RF signals are generated at frequency $2f_{LO} + f_{IF}$ (upper sideband) and $2f_{LO} - f_{IF}$ (lower sideband). The RF outputs of the two SHP mixers are combined by in-phase combiner and only one sideband appears at output of combiner. The other sideband is suppressed due to their opposite phase angles. The amount of this sideband suppression depends on phase and amplitude imbalance of LO divider and that of I/Q IF signals.

The schematic of the SHP mixer is shown in the Figure 1(b). The anti-parallel diode pair (APDP) is utilized for the sub-harmonic mixing. The APDP has a beautiful feature of the suppressing unwanted 2LO frequency signal which is very close to the desired RF signal. Each sub-circuit is designed separately and then integrated circuit is simulated to meet the required performance. Sub-circuits are designed to meet the compact layout size. The simulations of the circuits are performed using AWR's Microwave Office software. Both linear and nonlinear (harmonic-balance) simulations are used to design the circuits. The EM (electromagnetic) simulations of the layouts are done with Zeeland's IE3D simulator.

The schematics of the 45° LO power divider is shown in Figure 2(a). The L_1-C_1 and C_2-L_2 circuits are used at the output of the Wilkinson divider for the 45° phase difference between ports 2 and 3, respectively. The lumped elements and microstrip lines are used to realize Wilkinson divider at LO frequency. Design equations for the 45° phase difference circuit is presented here. The magnitude and phase of the S_{21} parameter of L_1-C_1 circuit at port 2 are given by,

$$|S_{21}| = \frac{100}{\sqrt{(100 - 50\omega^2 L_1 C_1)^2 + (\omega L_1 + 50^2 \omega C_1)^2}} \tag{1}$$

and

$$\angle S_{21} = -\tan^{-1} \frac{\omega L_1 + 50^2 \omega C_1}{100 - 50\omega^2 L_1 C_1} \tag{2}$$

Choosing the value of the angle of S_{21} equal to the $-22.5°$, the L_1
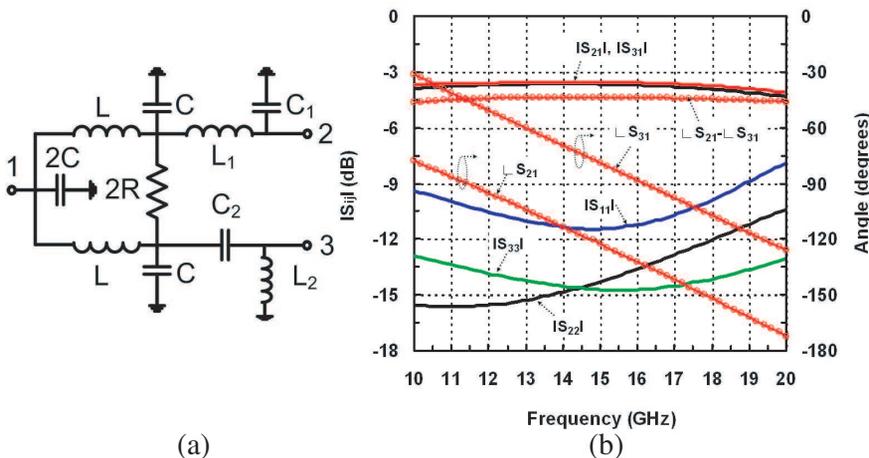
Figure 2. (a) Schematics, and (b) simulated S-parameters of the 45 degree LO divider.

can be given in terms of C_1 as;

$$L_1 = \frac{41.42 - 50^2 \omega C_1}{20.71 \omega^2 C_1 + \omega} \qquad (3)$$

Putting the value of L_1 from Equation (3) into Equation (1), the value of C_1 can be determined for the minimum value of the magnitude of S_{21}. For example, at the frequency of $15\,\text{GHz}$ the value of the C_1 is $0.08\,\text{pF}$ for $|S_{21}| = -0.02\,\text{dB}$. Then the estimated value of the inductance L_1 is $0.21\,\text{nH}$. This small value of capacitance (C_1) is realized using open stub to avoid process variations.

Similarly, the equations for the magnitude and angle of S_{21} for the circuit C_2-L_2 can be given as:

$$|S_{21}| = \frac{100 \omega^2 L_2 C_2}{\sqrt{(100 \omega^2 L_2 C_2 - 50)^2 + (\omega L_2 + 50^2 \omega C_2)^2}} \qquad (4)$$

and

$$\angle S_{21} = \tan^{-1} \frac{\omega L_2 + 50^2 \omega C_2}{100 \omega^2 L_2 C_2 - 50} \qquad (5)$$

Again choosing the value of the angle of S_{21} equal to the $22.5°$, the L_2 can be given in terms of C_2 as;

$$L_2 = \frac{20.71 + 50^2 \omega C_2}{41.42 \omega^2 C_2 - \omega} \qquad (6)$$

The values of the C_2 and L_2 are estimated to be $0.56\,\mathrm{pF}$ and $1.36\,\mathrm{nH}$, respectively for the $|S_{21}| = -0.02\,\mathrm{dB}$, and $\angle S_{21} = 22.5°$ at the frequency of $15\,\mathrm{GHz}$.

The EM simulated S-parameters of $45°$ LO divider is shown in Figure 2(b). The phase of the L-C circuit at both of the output ports of the divider changes linearly with frequency and phase difference
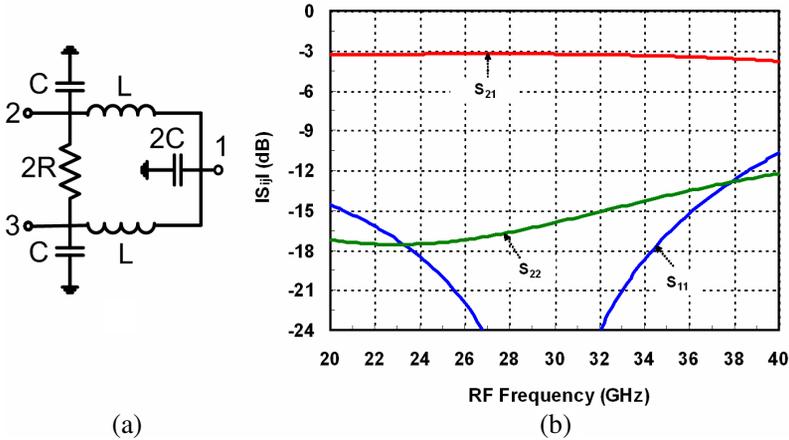
Figure 3. (a) Schematics, and (b) simulated S-parameters of the RF combiner.
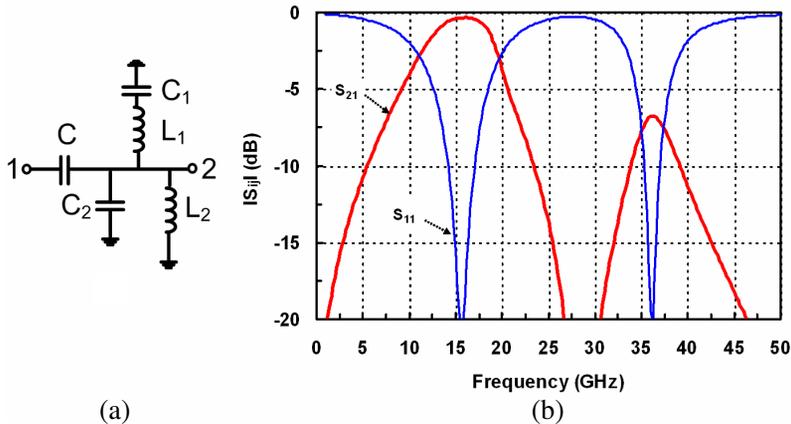
Figure 4. (a) Schematics, and (b) simulated S-parameters of the RF/IF short circuit.

between the ports remains constant for the wide bandwidth. The circuit has 45° phase difference between the ports 2 and 3 in wide frequency range from 10–20 GHz. The phase imbalance is 2° and amplitude imbalance is below 0.2 dB for the frequency range of 10–20 GHz, respectively.

For the RF in-phase combiner the lumped element Wilkinson combiner is used. The lumped element approach is useful for realizing the compact layout size as well as wide bandwidth. The magnitude of the S-parameters of the RF combiner is shown in Figure 3(b). It shows wide bandwidth and low insertion loss.

The SHP mixer as shown in Figure 1(b) is designed using anti-parallel diode pair for the second harmonic mixing. The size of the each diode used in mixer is $2 \times 30\,\mu$m. At the LO port of the SHP mixer, a circuit for shorting IF (intermediate frequency) and RF signals is used. Similarly, the LO short circuit is used at the RF port of the mixer to short the LO signal. The IF is fed through the low pass filter at RF port end of the diode. The schematic and S-parameters of the RF/IF short circuit at LO port is shown in Figure 4. The quasi lumped (microstrip and capacitor) circuit is used to achieve a compact size of the circuit. The IF is grounded through short circuited microstrip (L_2) and RF by L_1-C_1 circuit. The higher RF frequencies are also shorted by capacitor (C_2). The S_{21} of the circuit shows that IF is attenuated more than 20 dB at 1 GHz and better than 15 dB up to 2.5 GHz. The attenuation for the RF signal is greater than 10 dB for the frequencies of 23–33 GHz. It further attenuates higher frequencies

(a)   (b)
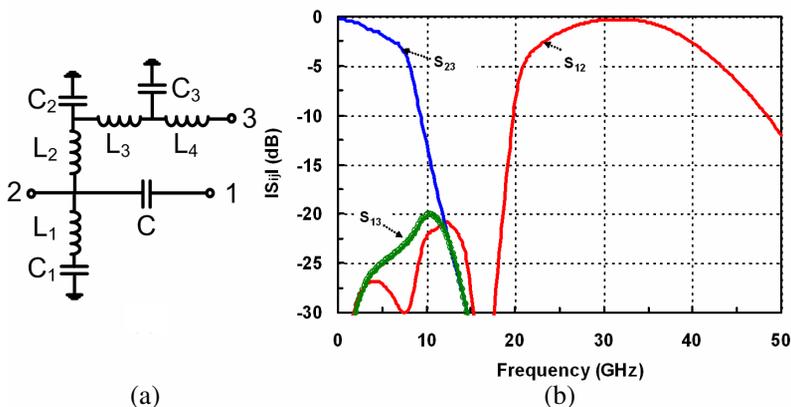
Figure 5. (a) Schematics, and (b) simulated S-parameters of the LO short and IF feed circuit.

above 40 GHz. The insertion loss of RF short circuit for the LO signal
is between 0.5–3 dB for the frequency of 12–18 GHz. The schematic
and S-parameters of the LO-short circuit is presented in the Figure 5.
The IF is fed at port 3 and RF is collected from the port 2.The LO
signal is attenuated about 15–30 dB from 10–19 GHz at the RF port.
The passband frequency for the IF is greater than 5 GHz. The IF is
also attenuated better than 25 dB at the RF port. The insertion loss
of the LO short circuit for the RF frequency of 23–40 GHz is less than
3 dB.

    The conversion gain of upper sideband (USB) and lower sideband
(LSB) of the SSB mixer is shown in Figure 6(a). The USB conversion
gain of the mixer is between −13 to −10 dB for wide range of the RF
frequency of 21–40 GHz. The decreases of conversion gain at lower
and higher RF frequencies are due to the insertion loss of LO short
circuit at RF port of the SHP mixer. The −10 dB conversion gain at
the Ka-band frequency for the sub-harmonic mixing is among the best
reported values [2, 5, 6, 8, 9]. The LSB suppression is above 20 dB for
20–40 GHz. The lower suppression of LSB at the higher RF frequencies
is for the phase imbalance degradation of the 45° LO divider due to
the effect of the RF/IF short circuit at LO port of the SHP mixers.

    The RF output of the SSB mixer is fed into the RF amplifier to
amplify the RF signal up to the level of 0–10 dBm to drive the driver
amplifier of the transmitter. The 3-stage RF amplifier is designed to
get gain above 20 dB. The schematic of the RF amplifier is shown
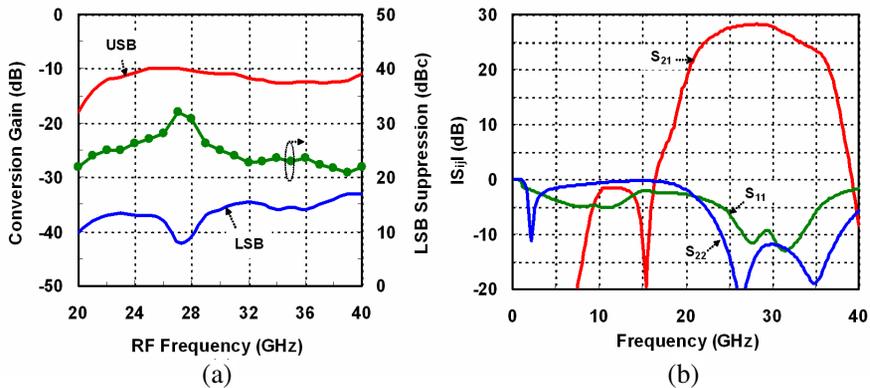
Figure 6. (a) Simulated conversion gain of upper sideband (USB)
and lower sideband (LSB) of the SSB mixer (LO = 8–17 dBm, IF =
−20 dBm, 1 GHz), and (b) Simulated S-parameters of the 3-stage RF
amplifier.

in Figure 1(c). For the design of the amplifier the wide bandwidth, linearity, and compact layout size are the major consideration. The simulated S-parameters of the amplifier are shown in the Figure 6(b). The simulated gain of the amplifier is above 20 dB for the wide bandwidth of 20–36 GHz. The simulated output return loss (S_{22}) is better than 10 dB for the frequency range of 24–38 GHz. The input return loss (S_{11}) of the amplifier is better than 5 dB over 25–35 GHz.

3. RESULTS OF THE INTEGRATED UP-CONVERTER MMIC AND DISCUSION

The microphotograph of the fabricated MMIC chip is shown in Figure 7. The circuit was implemented by WIN semiconductor's standard 0.15 μm GaAs MMIC technology on a 100-μm substrate thickness. The chip dimension is 2.3 mm × 1.8 mm. The measured and simulated results of the integrated up-converter MMIC are presented in this section. Chip is mounted on the carrier and bonded for the DC bias. Microwave signals are provided/collected by 50 Ohm G-S-G (ground-signal-ground) probes and off chip quadrature hybrid is used to provide two I/Q (inphase/quadrature phase) IF signals. Measurements presented here are for the drain bias voltage of 4.5 V and current of 195 mA.

The conversion gain versus LO power for the RF frequency of 31 GHz and IF frequency of 1 GHz is shown in Figure 8. The measured
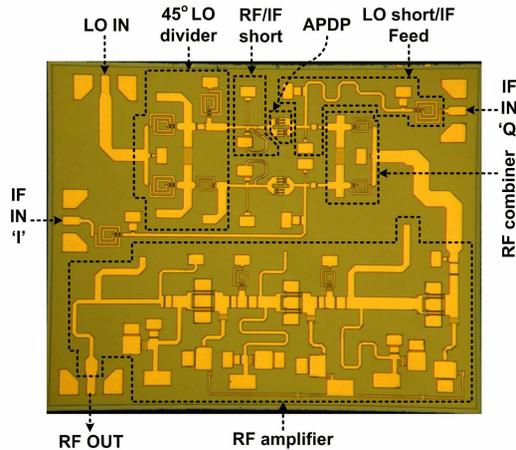
Figure 7. Microphotograph of the fabricated MMIC chip. The area of the layout is 4.2 mm^2.

maximum conversion gain of 15 dB occurs at the LO power of 9 dBm. The maximum conversion gain for the RF frequency of 22–38 GHz is between 9–16 dB. The required LO power for the maximum conversion gain varies between 9–16 dBm for different LO frequencies of 10–19 GHz. This variation is because of the insertion loss of the RF/IF short circuit at LO port of the SHP mixers and return loss due to the mismatch at the LO port of the integrated up-converter.

The conversion gains of the upper sideband (USB) and lower sideband (LSB) are shown in Figure 9 for the RF frequency of 20–40 GHz and IF frequency of 1 GHz. The USB conversion gain is above 9 dB for the RF frequency from 22–38 GHz. The decrease of the conversion gain above 39 GHz and below 22 GHz is due to the decrease of the RF amplifier gain as well as effect of the mixer conversion gain. The measured gain is also higher than the simulated gain at the high frequency end above 37 GHz. This indicates that the fabricated RF amplifier provides gain up to the frequency of 39 GHz in comparison to 37 GHz as in simulation result. It can be expected from the measurement result that the conversion gain of the mixer is between −10 to −13 dB and gain of the RF amplifier is above 20 dB.

The LSB suppression with respect to the USB is given in Figure 10. The measured LSB suppression is better than 20 dB for the frequency of 21–35 GHz and about 15 dB up to the 39 GHz. Any degradation in the measured result of the LSB suppression in comparison of simulation result is expected due to the higher phase imbalance of the fabricated
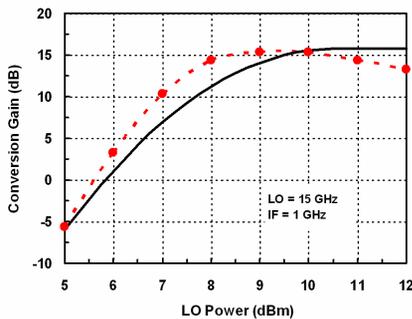
Figure 8. Measured (dashed line) and simulated (solid line) conversion gain of USB vs. LO power of integrated up-converter.
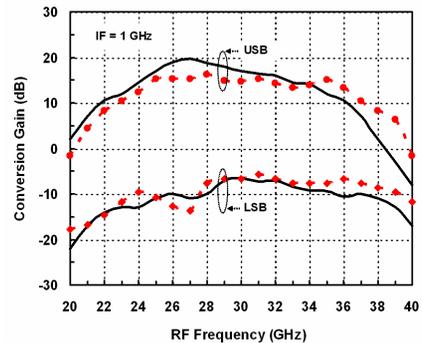
Figure 9. Measured (dashed line) and simulated (solid line) conversion gain of USB and LSB versus RF frequency of integrated up-converter.
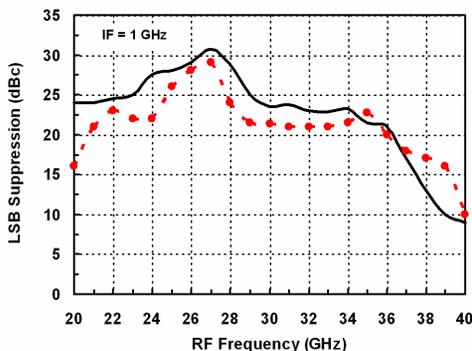
Figure 10. Measured (dashed line) and simulated (solid line) LSB suppression versus RF frequency of integrated up-converter.
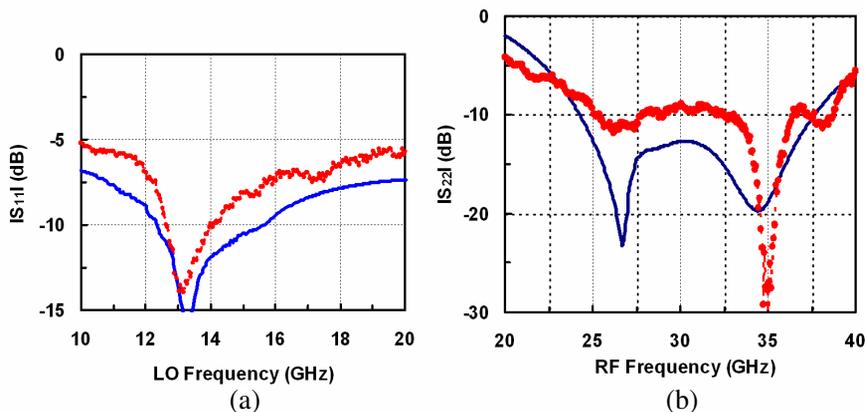
Figure 11. Measured (dashed line) and simulated (solid line) S-parameters for the mismatch at (a) LO port, and (b) RF port.

$45°$ LO divider. Also, due to the effect of short circuits (LO short circuit, RF and IF short circuit) the phase of the $45°$ LO divider is affected slightly. This decreases the sideband suppression. Overall the 20 dB suppression of LSB shows good performance of the up-converter

Measured and simulated S-parameters for the mismatch at the LO and RF ports of the integrated up-converter are shown in Figure 11. The magnitude of S_{22} at the RF port is about -5 dB for the frequency range of 20–40 GHz and better than -9 dB for 25–38 GHz. Also, measured magnitude of S_{11} at the LO port is about -5 dB or better for the frequency from 10–20 GHz. The LO port mismatch losses is one of

the reason for the variation of LO power at different LO frequencies to achieve maximum conversion gain. The minimum LO power of 9 dBm is required at the LO frequency of 14.5 GHz and increases to the value of 16 dBm at the frequencies of 10 GHz and 19 GHz.

The RF output power versus IF input power at the RF frequency
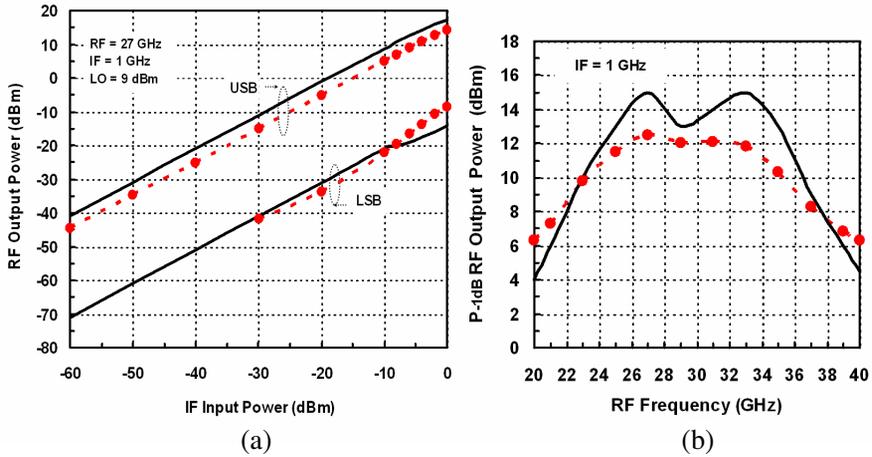
Figure 12. Measured (dashed line) and simulated (solid line) results of integrated up-converter, (a) RF output power versus IF input power, and (b) $P_{-1\,dB}$ RF output power for different RF frequencies.
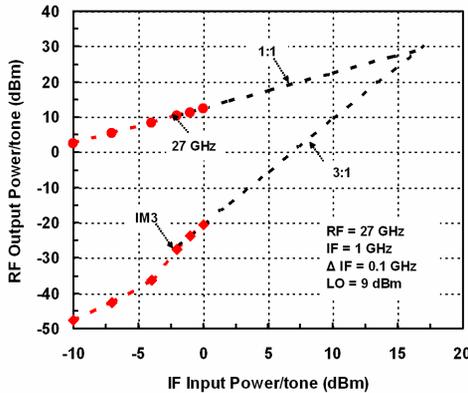
Figure 13. Measured third order inter-modulation distortion of the integrated up-converter.

of 27 GHz and IF frequency of 1 GHz is shown in the Figure 12(a) for the LO power of 9 dBm. The RF output power varies linearly with the IF input power as low as −60 dBm and saturates for the IF input power greater than 0 dBm. The variable attenuator at the IF frequency can be used for the dynamic control of the RF output power level and linearity as per requirement in the field application. The saturated RF output power is greater than 12 dBm. The $P_{-1\,dB}$ RF output power for the frequency from 20–40 GHz is given in Figure 12(b). The measured $P_{-1\,dB}$ RF power of 12 dBm is obtained for the frequency of 27–33 GHz and above 7 dBm for 21–39 GHz.

Figure 13 presents third order inter modulation product (IM3) for the two tone test of the integrated up-converter with IF frequency of 1 GHz, frequency difference between the tones of 0.1 GHz and RF frequency of 27 GHz. The measured OIP3 (output referred third order intercept point) and IIP3 (input referred third order intercept point) are greater than 20 dBm and 15 dBm, respectively.

The suppression of 2LO signal below USB is shown in Figure 14(a) for the IF frequency of 1 GHz and power of −2 dBm. The 2LO is suppressed more than 30 dB for the RF frequency of 28–34 GHz. However, the 2LO suppression decreases for the lower and higher RF frequencies. The presence of the 2LO signal is also due to the second harmonic generation of the LO signal by wideband RF amplifier. The isolation between LO and RF port is shown in Figure 14(b). The LO to RF port isolation is 20–35 dB for the LO frequency from 10–20 GHz. The bandwidth of the LO suppression is dependent on the bandwidth of the LO short circuit at the RF port of the mixer. The amount of LO
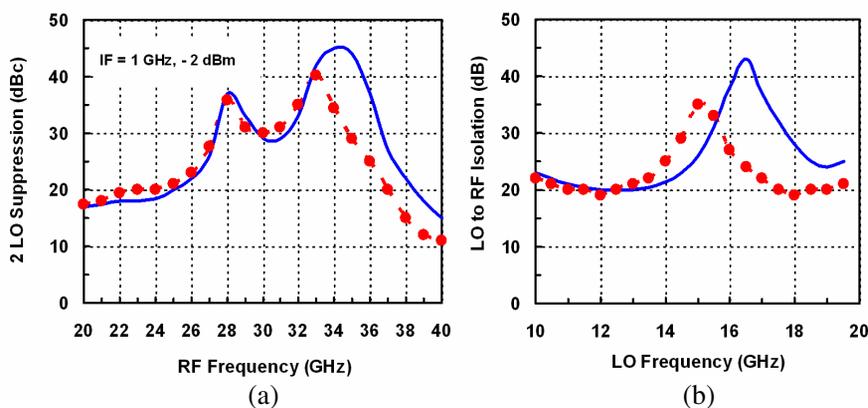
Figure 14. Measured (dashed line) and simulated (solid line), (a) 2LO suppression, and (b) LO to RF isolation of the integrated up-converter.

suppression is also affected by the wideband RF amplifier. The wide bandwidth design of the RF amplifier does not help to suppress the LO signals deeply in wideband. The filter circuit for further suppressing LO frequencies before RF amplifier will be useful to suppress both of the LO and 2LO signals.

The comparison of the simulation and measurement results is presented in Table 1. It is interesting that the simulation results are very close to the measured results which are useful for the optimizing circuit performance especially for the integrated circuits. The comparison of the measured results with other published results of the integrated Ka-band up-converters is presented in Table 2. The performance of the presented chip is better than that of [10] in terms of bandwidth, conversion gain, and output power. The performance of the chip is very similar to that of [11] with compact layout area.

Table 1. Comparison of the simulation and measurement results.

Paramenters	Simulation	Measurement
Vds, supply voltage (V)	4.5	4.5
Ids, supply current (mA)	200	195
LO frequency (GHz)	10–19	10–19
LO power (dBm)	8–17	9–16
RF frequency (GHz)	21–37	22–38
Conversion gain (dB)	9–20	9–16
Output RF power, $P_{-1\,\mathrm{dB}}$ (dBm)	7–15	7–12
Side-band suppression (dBc)	15–30	17–27
2LO suppression (dBc)	18–45	15–40

Table 2. Typical comparison of measured performance of the presented chip with other's chips.

Parameters	[10]	[11]	[11]	This Work
RF frequency band (GHz)	24–29	17–36	32–45	22–38
Conversion gain (dB)	0–5	10–13	3	9–16
$P_{-1\,\mathrm{dB}}$ output power (dBm)	1	-	-	7–12
IIP3 (dBm)	-	12	15	17
Side-band suppression (dBc)	16	0	15	17–27
2LO suppression (dBc)	-	5–15	>0	15–40
LO to RF isolation (dB)	15	15–40	-	20–35
LO power (dBm)	0	0	2	9–16
Layout area (mm^2)	4.2	6.8	5.9	4.2
D. C. power consumption (W)	0.8	2	0.8	0.9

However, the required LO power (9–16 dBm) is higher which can be reduced to 0 dBm by further integrating single stage LO amplifier.

4. CONCLUSION

The design and implementation of the integrated compact broad Ka-band sub-harmonic single sideband up-converter MMIC has been presented in this paper. The measured conversion gain is 9–16 dB for the RF frequency from 22–38 GHz. The $P_{-1\,dB}$ RF output power level is 12 dBm. The amount of the sideband suppression is between 17–27 dB. The suppression of the 2LO frequency component is above 20 dB for the RF frequency from 26–36 GHz. Simulation results are very close to that of measured results. This is useful for the optimization of integrated circuit performance for any specific application. The size of the MMIC is as compact as $4.2\,mm^2$. This integrated chip is suitable for the low cost and high performance Ka-band transmitter module applications.

ACKNOWLEDGMENT

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