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A 802.11a PULSE-SWALLOW INTEGER-N FREQUENCY SYNTHESIZER

C.-C. Tien

National Chiao-Tung University
Taiwan, R.O.C.

T.-M. Tien

National Cheng-Kung University
Taiwan, R.O.C.

C. F. Jou

National Chiao-Tung University
Taiwan, R.O.C.

Abstract—This article presents the complete design of a 802.11a pulse-swallow integer-N frequency synthesizer. Except for the loop filter, the entire circuit is designed on the chip. The reference frequency is set to 10 MHz and a pulse-swallow counter is designed for the purpose of controlling the dual-modulus divider ($\div 8/9$). The frequency tuning range varies from 4.98 GHz to 5.73 GHz meanwhile the output power of the voltage-controlled oscillator is -13.5 dBm, and the phase noise measured at 1 MHz is -126 dBc/Hz. The settling time of the closed loop is about 20 μs, the total power dissipation is 26.35 mW with 1.8 V supply voltage. The chip size is 1.15 mm × 1.06 mm and fabricated under TSMC CMOS 0.18 μm.

1. INTRODUCTION

The two most popular structures of RF frequency synthesizers are the fractional-N frequency synthesizer and the integer-N frequency synthesizer. Although fractional-N synthesizer owns a great performance in frequency resolution and settling time, its division number depends on accumulator carrier which may lead to spur

Corresponding author: C.-C. Tien (socrate1118@gmail.com).

noise closing to the wanted signal due to the periodically produced characteristic. Consequently, compared with the integer-N frequency synthesizer, a more complicated modulator is needed to alleviate the influence of noise for fractional-N synthesizer. Since frequency resolution is not the main factor among designing progress such as 802.11a/b/g WLANs systems, integer-N structure will be the better choice due to its spectrum purity [3].

A 802.11a pulse-swallow integer-N frequency synthesizer is shown in Fig. 1. Since passive components are generally larger than active ones, a circuit out of the chip is implemented under the consideration of performance adjustment. The output frequency of the voltage-controlled oscillator is 5.2 GHz, and the total division is 520 while the reference frequency is set to be 10 MHz [1].

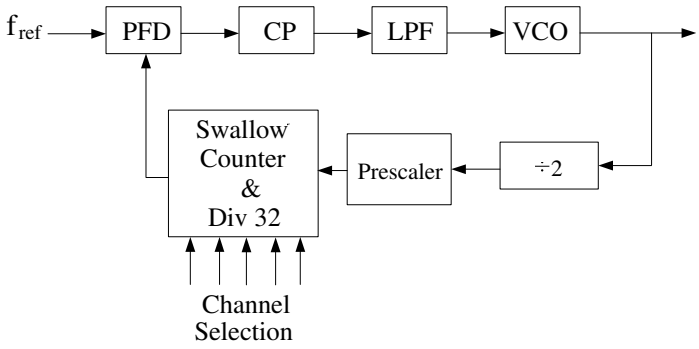


Figure 1. Basic architecture of an integer-N frequency synthesizer.

2. VCO DESIGN

In order to fit the specifications of 802.11a WLANs system, differential and complementary cross-coupled pairs were applied to generate 5 GHz differential symmetric signal outputs. The circuit is shown in Fig. 2; both PMOS and NMOS cross-coupled pairs are adopted at the same time to provide higher negative resistance and symmetries of the output waveform. With differential outputs, the common-mode noise coupled from substrate can certainly be alleviated and will lead to impressive low phase noise; meanwhile, since PMOS owns great ability against flicker noise, it can suppress noise up-converted from $1/f$ noise and other low frequency noise sources efficiently.

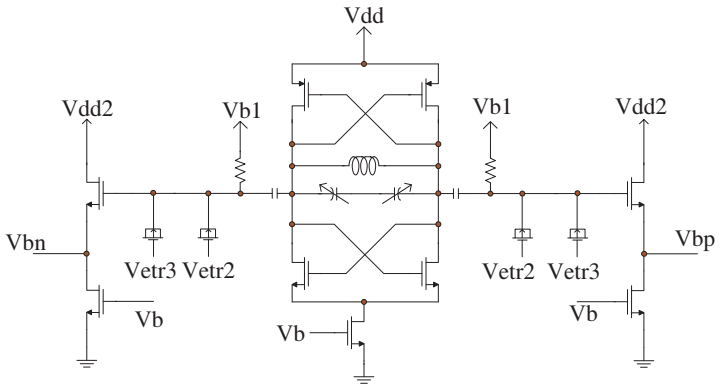


Figure 2. 5.2 GHz voltage controlled oscillator architecture.

3. DUAL-MODULUS FREQUENCY DIVIDER (DMFD)

Since the oscillating frequency is modulated by setting control signals to change the total divisor, a circuit which can carry out more than one division is needed. In this design work, we realize a dual-modulus frequency divider that can switch division between 2 and 3 by combining NOR gates to D-type flip-flops. The circuit prototype is shown in Fig. 3 with clock time diagram analyzed, and the single analog D-type flip-flop. Also, a DMFD can also accomplished by substituting the NOR gates for NAND gates [5].

A DMFD must be well constructed and carefully dealt with its parasitic effects which are due to the complicated cross-coupled signal lines. So the layout is laid in a compact way and the estimated parasitic capacitances about 25 fF are connected to the output nodes.

4. PRESCALER AND PULSE-SWALLOW COUNTER DESIGN

The prescaler in this design work is actually a combination of two divide-by-2 dividers and a DMFD, thus makes the total division varies between 8 and 9. It is connected right after the outputs of a divider that the main function is to lower the oscillating frequency. The circuit blocks are shown in Fig. 4; the modulus control signal (mc) is provided by the pulse-swallow counter [6].

Pulse-swallow counter is the key circuit in the close loop design since it controls dual modulus division. It consists of a channel detecting circuit and a loading/resetting counter. The basic way it

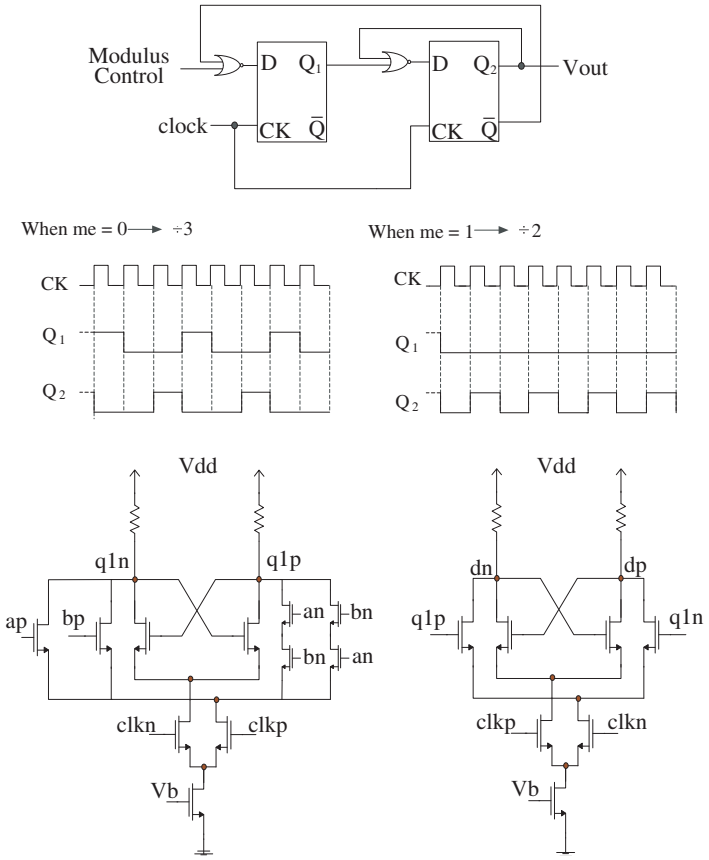


Figure 3. The prototype of DMFD with its clock timing diagram and single analog DFF.

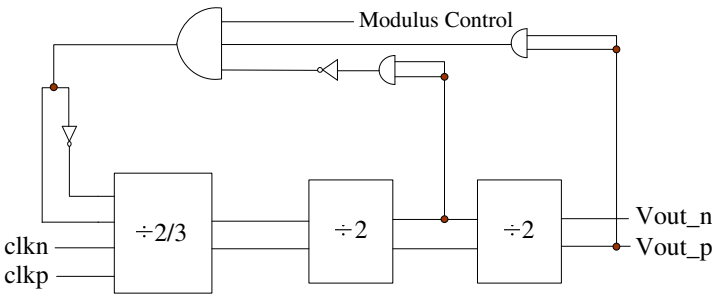
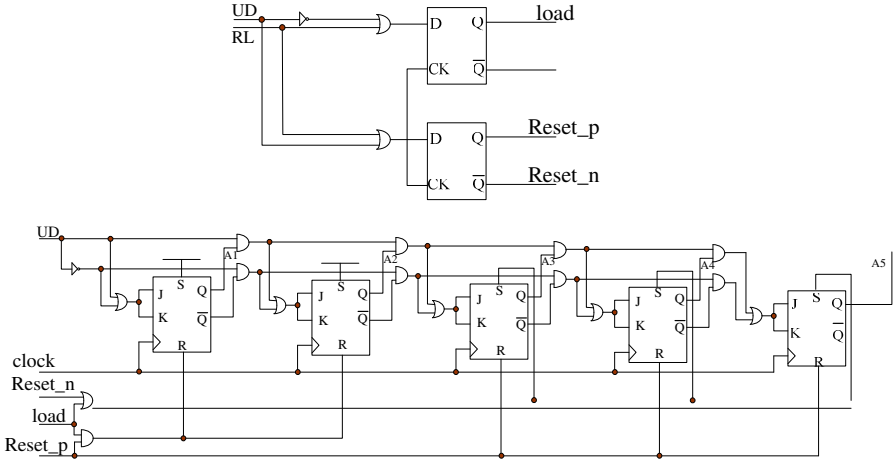


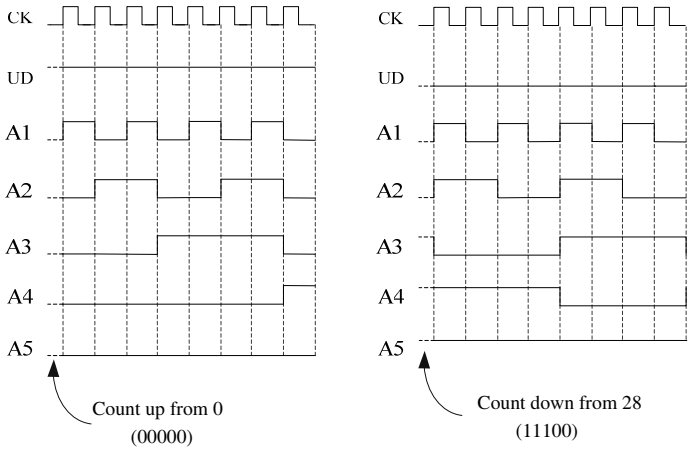
Figure 4. Components of a prescaler.

operates is that the counter counts up from zero to the setting input codes (e.g., 00111), then it is reset to count down from 28 to the input codes thus makes a period of 32.

Figure 5(a) shows a loading and resetting counter consists of 5 JKFFs with which J and K are shorted together and Figure 5(b) shows timing diagram. The control signal UD determines the counting mechanism of the circuit; when the signal is low, the counter will count up, and comparatively it will count down if the control signal UD is



(a)



(b)

Figure 5. (a) Loading and resetting counter; (b) Timing diagram of loading and resetting counter.

set to high.

The fully-integrated pulse-swallow counter is shown in Fig. 6; the 5 output signals of the loading/resetting counter are connected to XORs to compare with the external channel input signals. Be aware that the load number of the counter should be set to 28 instead of 32, since no matter the counter counts up from 0 or counts down from 28, the load digit is calculated twice, and the same circumstance occurs during loading the codes and reset the counter. The analysis is shown in Fig. 7.

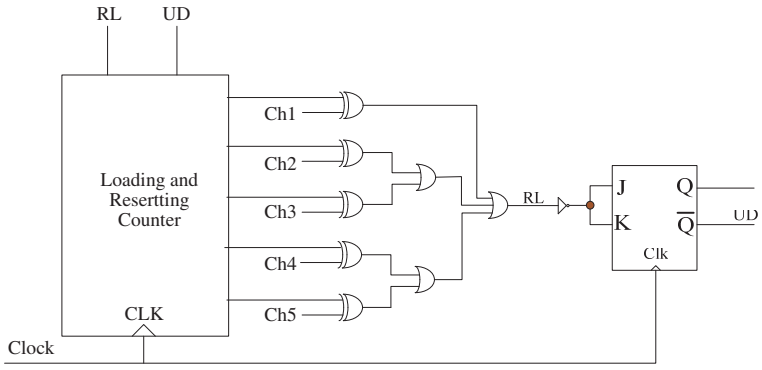


Figure 6. Architecture of fully-integrated pulse-swallow counter.

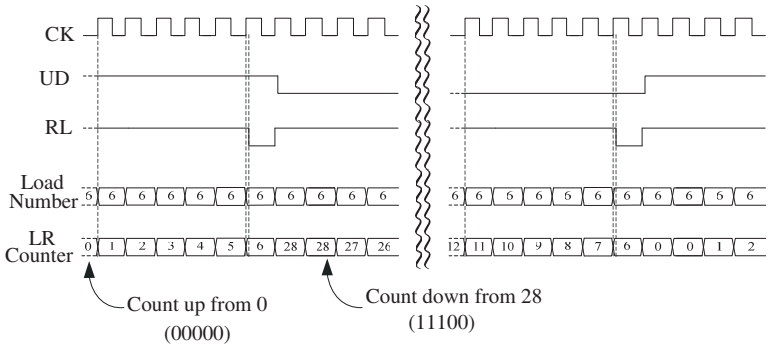


Figure 7. Analysis of a pulse-swallow counter.

5. PHASE FREQUENCY DETECTOR/CHARGE PUMP

Below is shown the basic implementation of PFD and a charge pump. As shown in Fig. 8, if the reference signal (V_{ref}) is faster than the signal scaling down from VCO (V_{div}), the upper flip flop will send the

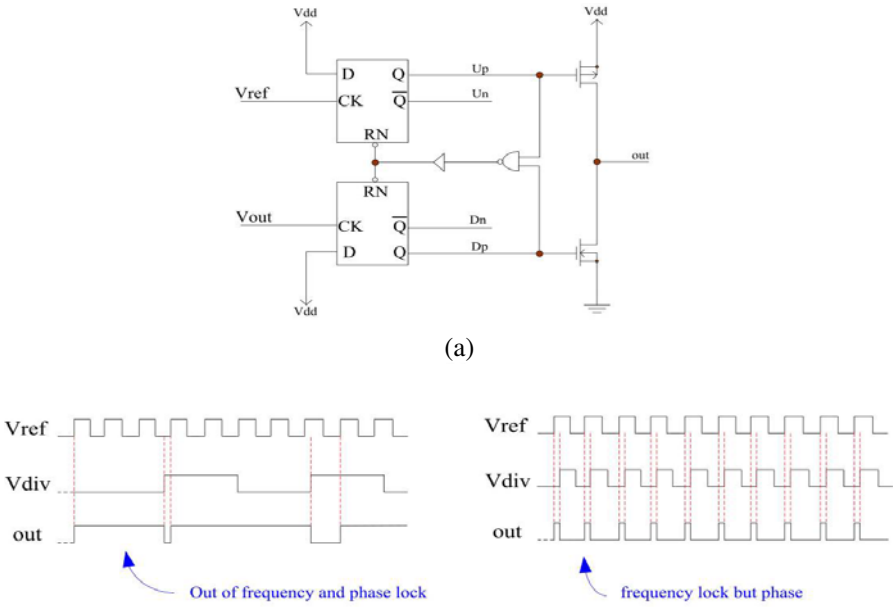


Figure 8. (a) Phase/frequency detector; (b) Time diagram comparison between V_{ref} and V_{div}.

output high and this is maintained until the first rising edge occurs on V_{div}, till then the NAND gate will generate a low signal back to reset both flip flops. In a practical system this means that the output which input to the VCO is driven higher forcing the oscillating frequency to catch up with the reference signal, vice versa.

Figure 9 is the architecture of a charge pump which functions as a transforming mechanism turn the phase mismatch detected by PFD into a charging current. In this project the charge pump works with a fixed reference current, and in order to obtain high voltage output range, the transistor size of the current mirror transistors ($M_1 \sim M_{11}$) must be designed considerably.

Furthermore, since the mismatched current produced at the time the two input signals are out of phase which will cause interference with adjacent channel and spurious tones in RF receiver, two extra implement transistors (M_{12}, M_{14}) will be implemented in the circuit to solve the problem. Those two NMOS guarantee that M_{13} and M_{15} sources are already pre-charged when switching takes place. Also an accurate layout of the circuit can improve the matching among the

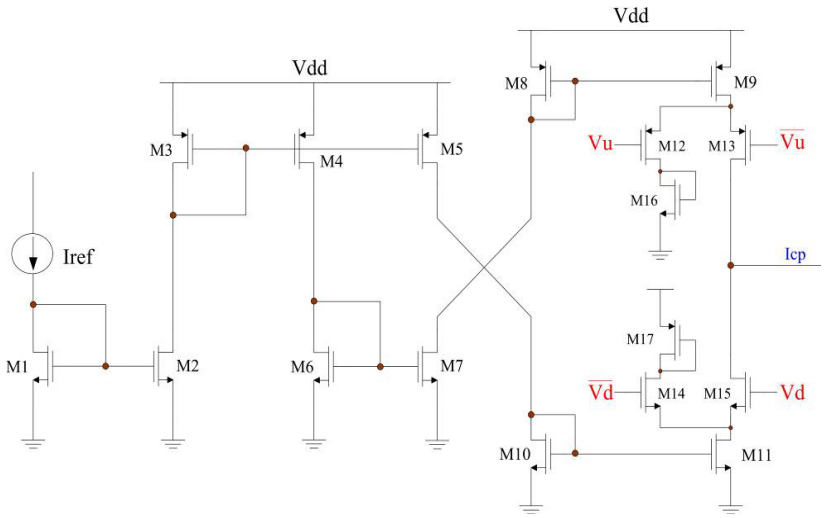


Figure 9. Schematic of charge pump.

positive and negative currents to reduce undesired spectral emission in RF transmitter.

6. LOOP FILTER

Since it is an extremely critical key point in designing a frequency synthesizer, a 3rd order RC loop filter used in this work is shown in Fig. 10. Output of a loop filter is a dc voltage and directly connected to VCO, so a well considered circuit not only can degrade high frequency noise but also can prevent the disturbance produced while PFD and charge pump switching states from influencing VCO, while the synthesizer stabilizes. The loop bandwidth of the filter affects the synthesizer settling time, so the filter was excluded from the chip to modulate the response of the circuit.

7. SIMULATION AND LAYOUT CONSIDERATION

It is important to simulate the entire circuit and make sure the function of it is correct before and after layout. Matlab is used in the beginning to ensure that the detail design concepts and the circuit parameters are accurate, and electromagnetic simulating tools used in post-layout to guarantee the critical signal paths are not influenced by parasitic effects. By doing so, a higher performance of the design can be achieved.

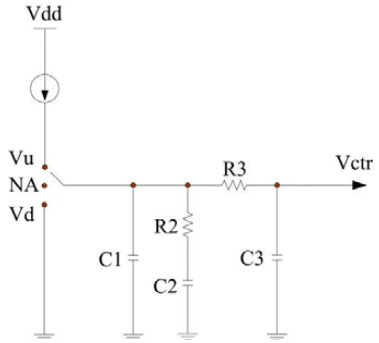
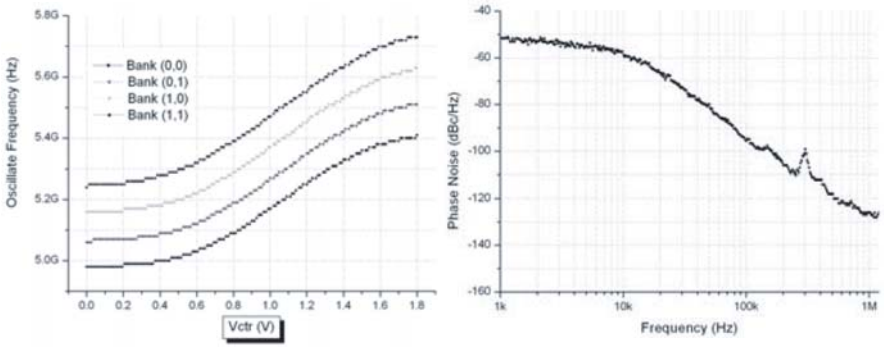


Figure 10. A 3rd order loop filter.



(a) (b)

Figure 11. (a) Measured tuning range under different banks; (b) Phase noise is −126 dBc/Hz@1 MHz offset.

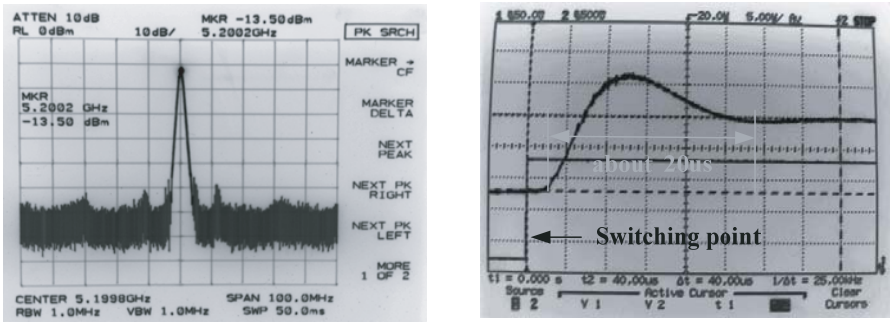
8. MEASUREMENT RESULTS

First the tuning curve and phase noise of the voltage controlled oscillator is discussed. As Fig. 11(a) shows, all the banks (from 00 to 11) include the frequency range needed, namely, as long as picking up the right control bits corresponding to each bank we can make the frequency synthesizer lock successfully.

Next the phase noise is investigated as a critical parameter of a voltage-controlled oscillator. Fig. 12(a) shows that the output power of the voltage-controlled oscillator on spectrum analyzer is −13.5 dBm at 5.2 GHz and thus derives a −126 dBc/Hz phase noise at 1 MHz offset from the carrier signal shown in Fig. 11(b).

Also shown in Fig. 12(b) is the measurement result of the settling time while applying a periodical clock signal to the division control

bit. As can be distinguished, the settling time is just a little bit longer than 20 µs which derived from the simulation. The control voltage is stably locked at about 40 µs. The comparison result between the references and this work is listed in Table 1. Clearly, the work done so far has a shorter settling time and outstanding phase noise among all the designs.



(a) (b)

Figure 12. (a) VCO output power is −13.50 dBm at 5.2 GHz; (b) Settling time of the closed loop.

Table 1. Comparison between references and this work.

Reference	[1]2005	[2]2005	[3]2003	[4] 2003	This work
Frequency band (GHz)	N/A	4.11~4.35	5.15~5.70	5.15~5.82	4.98~5.73
Tuning range	N/A	5.64%	27.2%	N/A	14.42%
Phase noise	−125 dBc/Hz (@3 MHz)	−139 dBc/Hz (@20 MHz)	−116 dBc/Hz (@1 MHz)	−106 dBc/Hz (@1 MHz)	−126 dBc/Hz (@1 MHz)
Divider architecture	Fractional-N	Integer-N	Integer-N	Fractional- N	Integer-N
Ref. frequency	N/A	16 MHz	10 MHz	19 MHz	10 MHz
Settling time	25 µs	N/A	100 µs	520 µs	20 µs
Power consumption	54 mW	9.68 mW	13.5 mW	N/A	26.35 mW
Supply voltage	1.8 V	1.0 V	2.5 V	1.8 V	1.8 V
Fabrication	0.18 µm	0.18 µm	0.25 µm	0.18 µm	0.18 µm

9. CONCLUSIONS

The article presents a design of a 802.11a integer-N frequency synthesizer with 20 µs settling time and −126 dBc/Hz@1 MHz phase noise. The voltage-controlled oscillator is designed to oscillate at 5.2 GHz thus derives a 14.42% tuning range. Swallow counter with five external input signals is adopted to control the two-modulus divider. The supply voltage is 1.8 V and total power consumption of the circuit is 26.35 mW.

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